Onsen Plans for Jan14 DESY Testbeam

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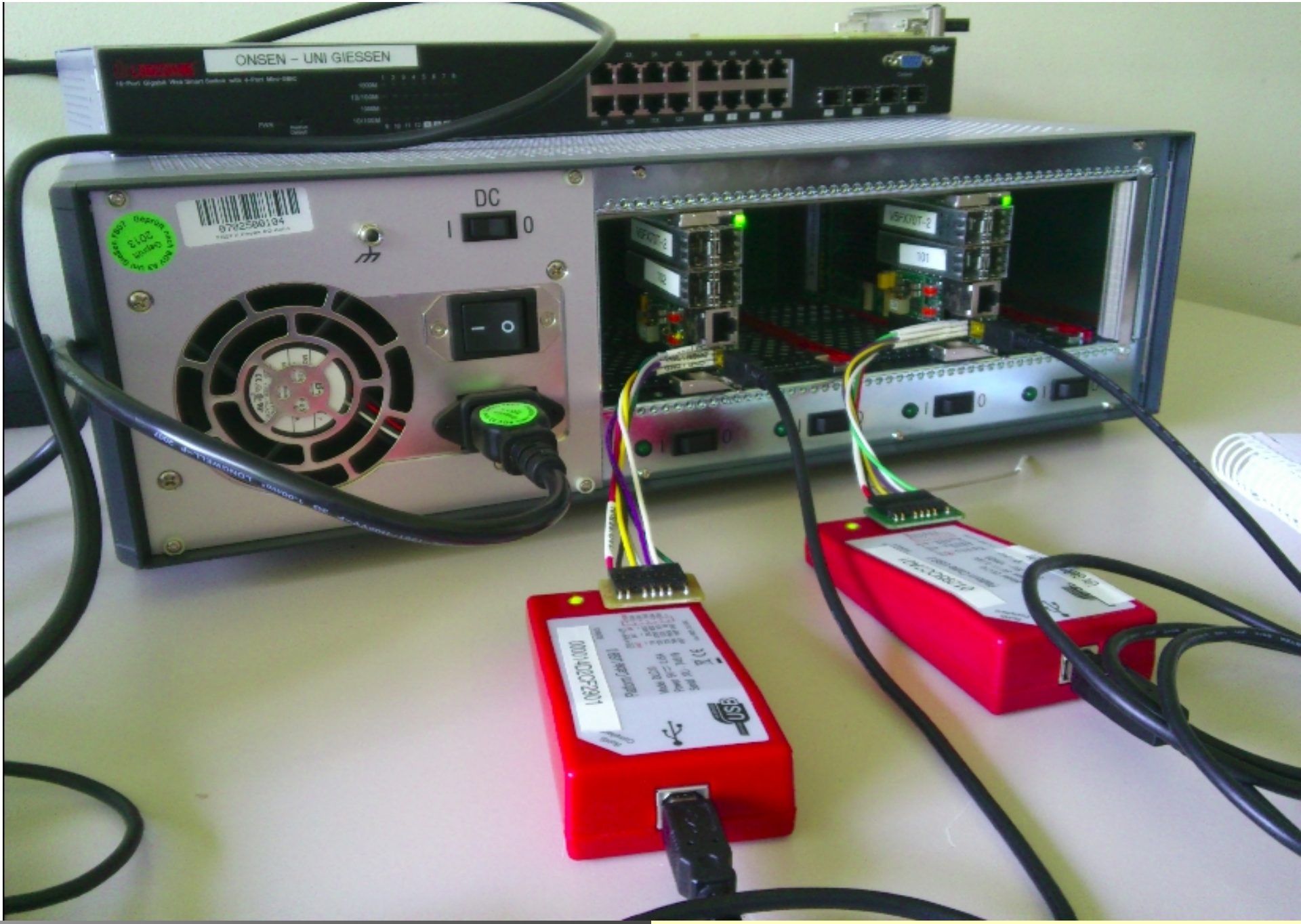
Onsen Preparations for Jan14 DESY Test (I)

1st priority:

- ROI core
- May13 test was only Rx/Tx data, but Jan14 requires unpack/decode on FPGA
- DHH error bit handling (ghost frames, …)
- event handling
  (8 frames per 1 trigger,
  2 frames(halfladders)/event, …)
- high speed optical links (6.25 Gbps)
- 2nd AMC board !
  - as input node for HLT ROI and DATCON ROI, AMC-AMC backplane communication
- fix the data format issues (double headers)

Very tight schedule !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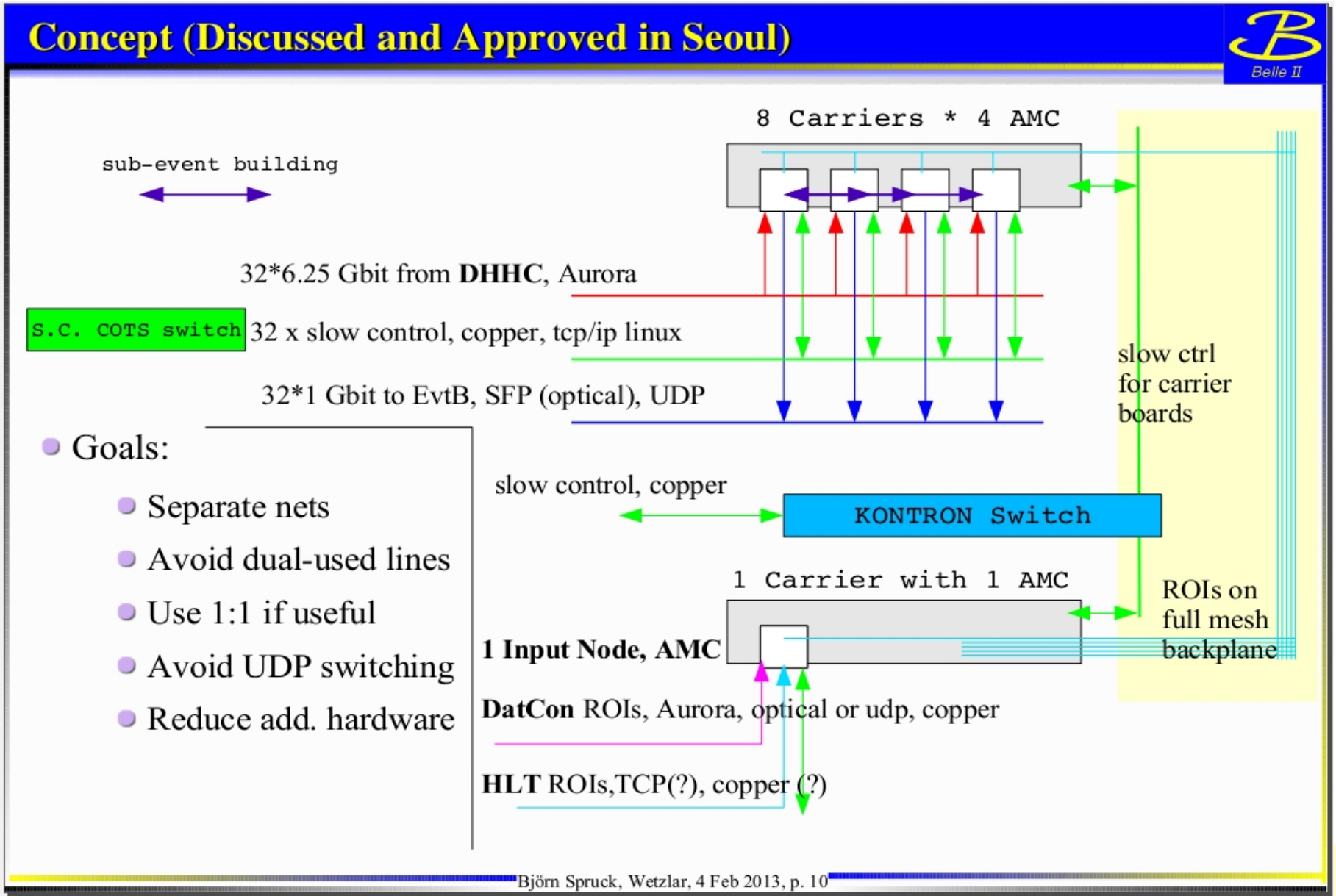
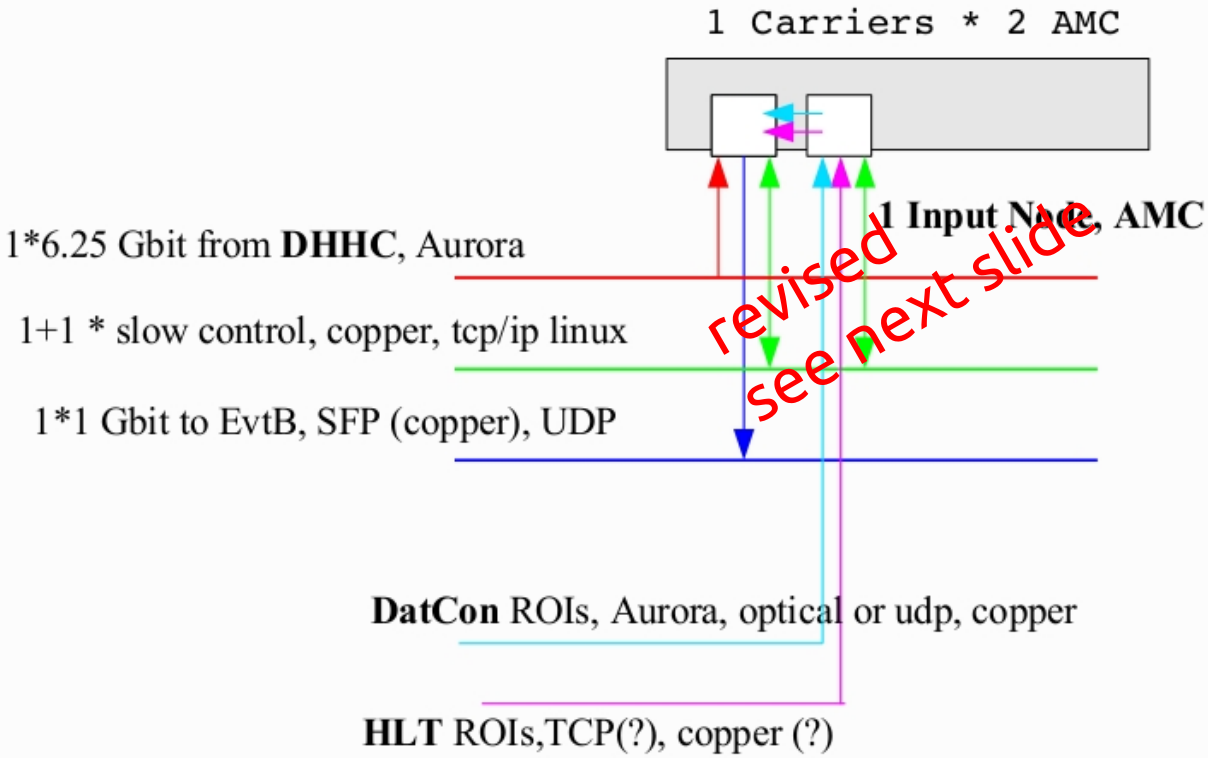
Paradigm change (Korea Workshop Jan13)
ROI distribution is not done by ATCA backplane anymore

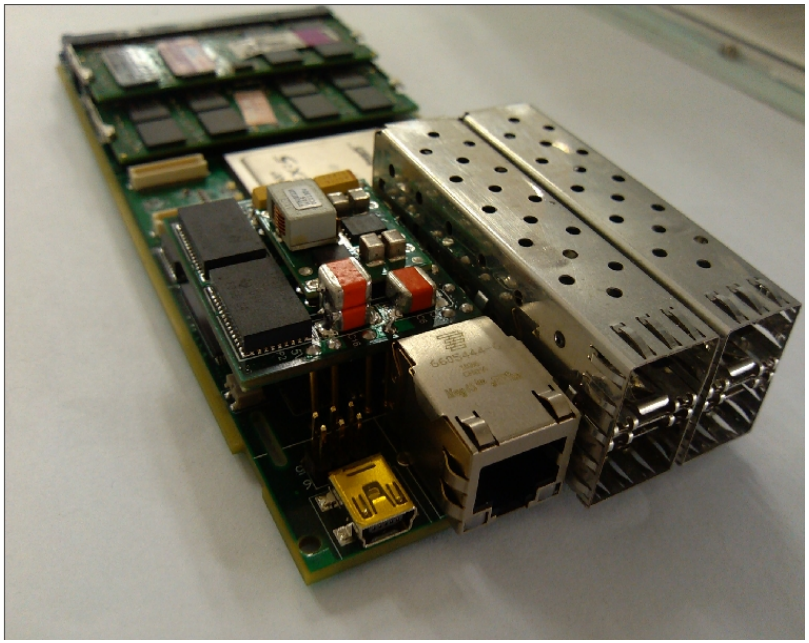


Concept (For 2013/14 DESY Test)

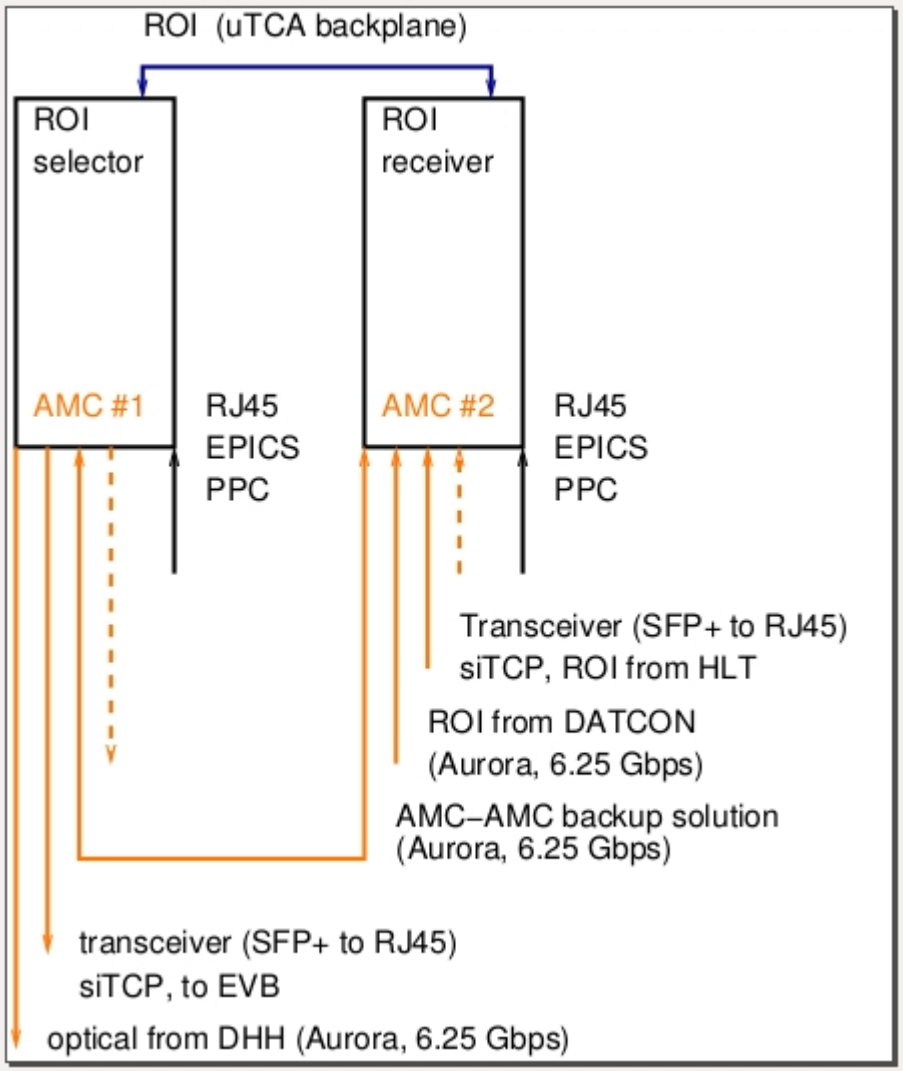
As carrier board is passive, no SC is needed.
Without backplane usage, we can use pizza-shelf.



Planned ONSEN Setup for DESY Jan14



Finisar FCLF-8521-3
SFP+ tp RJ45



Onsen Preparations for Jan14 DESY Test (II)

- EVB interface

  4 tasks:

  a. getting data from ONSEN to EVB

  b. getting data into basf2

  c. decoding in basf2

  d. monitoring similar to BonnDAQ

  a,b,c → new bachelor student: Klemens Lautenbach

  schedule: thesis by August 2013

  b,d → new summer student DESY/Prague: Tadeusz Bilka

Very tight schedule !

2nd priority: EPICS
(reading some registers on PowerPC is o.k. ,
but GUI etc. may not be ready)

Subsystem „Dry Tests“ before Jan14 DESY Test

Test of FTSW+DHH+Onsen
→ check data format (trigger word, measure latency)
→ check of [PXD+SVD]:[Mimosa] matching based upon trigger #

Test DATCON+Onsen
→ DATCON ROI must be sorted
→ receive ROI data (straight forward, Aurora)
→ check data format (extra headers, checksum, 48 bit alignment? Etc.)

Test Onsen+HLT
depends on timescale of HLT track finder,
maybe test with random ROIs at first
→ check data format (extra headers, checksum, 48 bit alignment? etc.)

Test DATCON+HLT+Onsen
→ mixer for DATCON ROI (from optical) and HLT ROI (from siTCP)
→ DATCON ROI must always arrive earlier
→ check timeout schemes for ROI non-arrival

Test with new ATCA-DHH+Onsen
(anytime when available, already before September?)

Important question (for Onsen firmware preparation):

Can we fix 1 frame per 1 trigger ?

It means: fixing and understanding
Trigger latency of TLU and FTSW

Milesstones (updated 12.06.2013)

Preparation of formware for DESY Beamtest Jan14

-> 30.09.2013

Design/Layout of new ATCA carrier board (bug fixing)

-> 31.12.2013

ONSEN mass production (8 carrier boards, 32 AMC cards)

-> 31.12.2014

Onsen and BEAST

BEAST DHH+Onsen could be very similar to DESY setups
(1-2 halfladders, small uTCA readout system, PocketDAQ)

But: all travel budget for work at KEK in 2015
in BMBF application was rejected.

David is following BEAST activity (on BEAST EVO meetings)
but in the moment no possibility to participate in BEAST

New funding application: December 2014
(funding would start in July 2015)

Priority: cosmic test of complete Belle II DAQ
w/ SVD and PXD.