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DHPT 1.0 Status

H. Krüger, Uni Bonn

DHP Development

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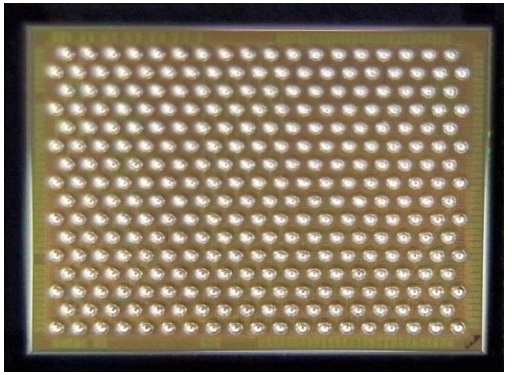
Current prototype: **DHP 0.2**

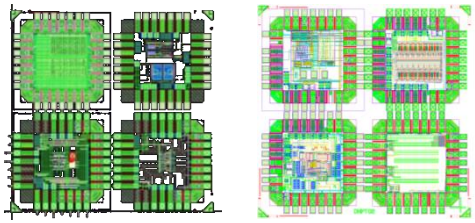
- Full size chip, IBM 90nm technology
- Used on Hybrid 5 prototype modules
  (future: large PXD6 matrices and E-MCM)
- Fully functional but a few limitations (i.e. no gated mode support)



DHP 0.2 full size prototype chip with bumps

Test chips: **DHPT 0.1** and **DHPT 0.2**

- TSMC 65nm technology
- Full custom analog block verification



DHPT 0.1 and DHPT 0.2 test chips

Next full size chip: **DHPT 1.0**

- TSMC 65nm technology
- **Footprint & electrical compatible to DHP 0.2**
- New features: Gated Mode support, enhanced trigger modes etc.

Design Review, April 11th

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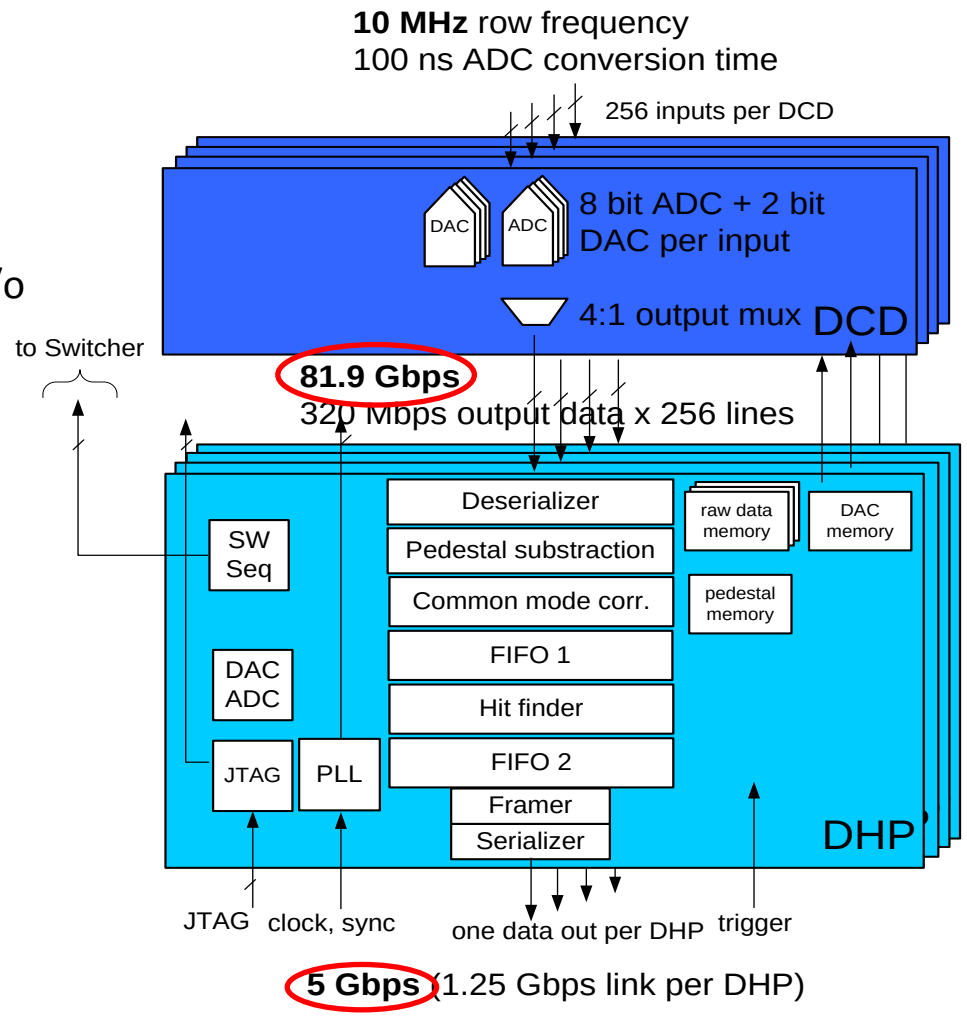
- Participants: R. Casanova, C. Kiesling, I. Konorv, A. Campbell, I. Peric, C. Kreidl, T. Hemperek, I.Kisisita, T. Kleinohl, H. Krüger, M. Lemarenko, F.Lütticke, C. Marinas, R. Richter (phone), A. Wassatsch (phone)
- Material: http://twiki.hll.mpg.de/twiki/bin/view/DepfetInternal/DesignResourcesDHP#DHPT_1_0_Design_Review_11_4_2013

➔ List of proposed/discussed changes implemented (some still need verification)

DHP Functional Overview

- Functionality
  - Module controller
    - JTAG bus to DCDB and SWITCHER chips
    - Clock & timing generation & distribution
  - Data reduction (1/20): 0-suppression, triggered r/o

- Data processing details
  - Raw data buffer
  - Common mode (two pass)
  - Fixed pattern noise correction (static pedestals)
  - Hit finder (FIFO1 + FIFO2)
  - Framing (AURORA)
  - Serializer + Gbit link driver



Major Changes wrt. DHP 0.2

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- Increased buffer sizes
- Fully programmable Switcher Sequencer
- Capability to exclude individual channels from common mode processing
- Trigger line → Manchester encoded commands (4 bits @ 80MHz)
- Minor bug fixes

DHPT 1.0 Data Buffer Resources

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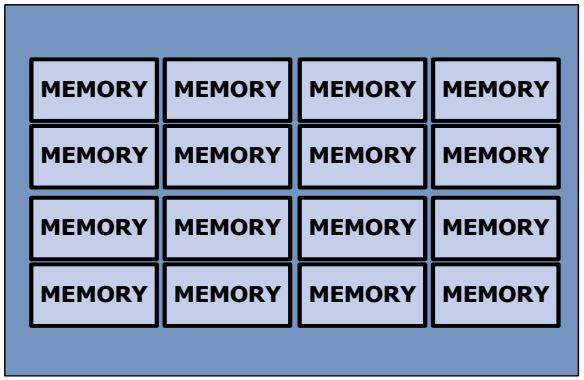
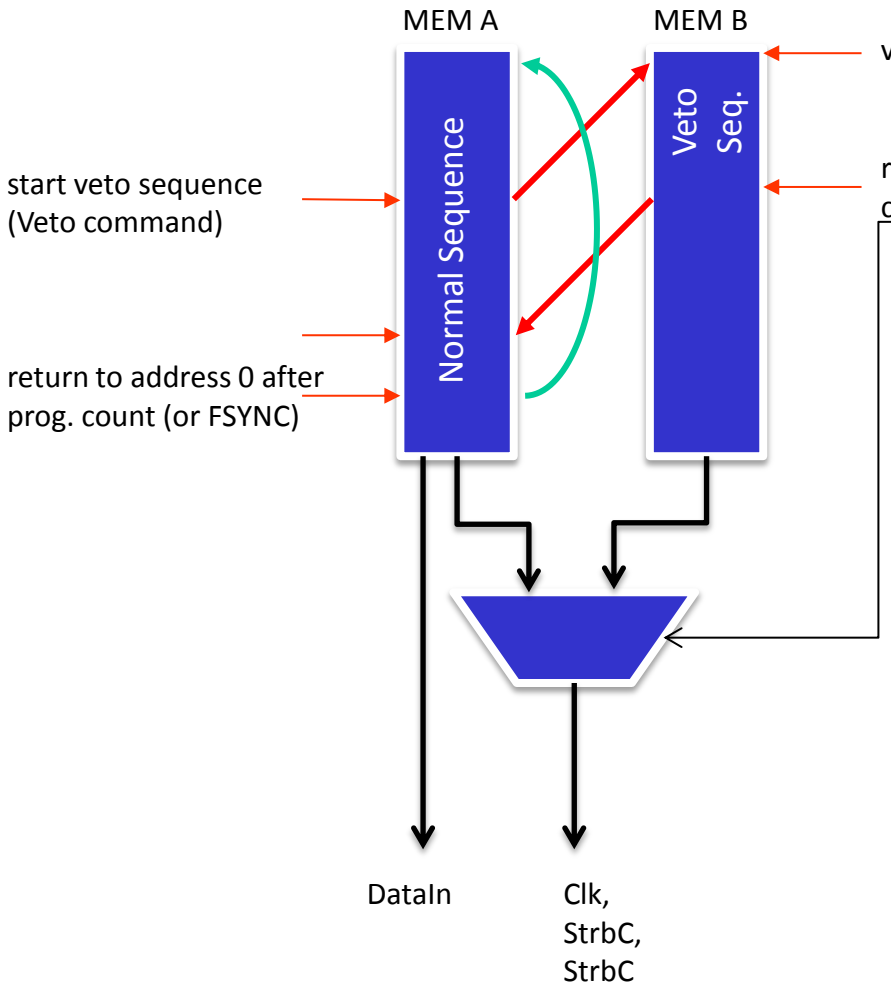
- Overall memory size is 4 full frames (1024 rows each)
  - 2 raw data frames
  - 2 pedestal frames
- Double buffer for pedestals:
  - One is active while the other one gets updated in the background (JTAG)
  - Toggle memories once update is finished
- Memory protected by Hamming code
- Full memory can be assigned to entirely capture raw data ata full r/o speed (for calibration or TB studies)

DHPT 1.0
16x 1024x128 (4x1024 rows)



DHPT 1.0 Switcher Sequencer



- Two memory blocks
  - MEM A for **standard** sequence
  - MEM B for **Gated Mode** sequence
- Switch form A to B on VETO command
- Switch back from B to A after programmed number of row clock cycles
- Individual row programming
- Timing resolution
  - Coarse: 3ns (320 MHz clock)
  - Fine: ~200ps (tapped delay line, 16x)

Fast Commands

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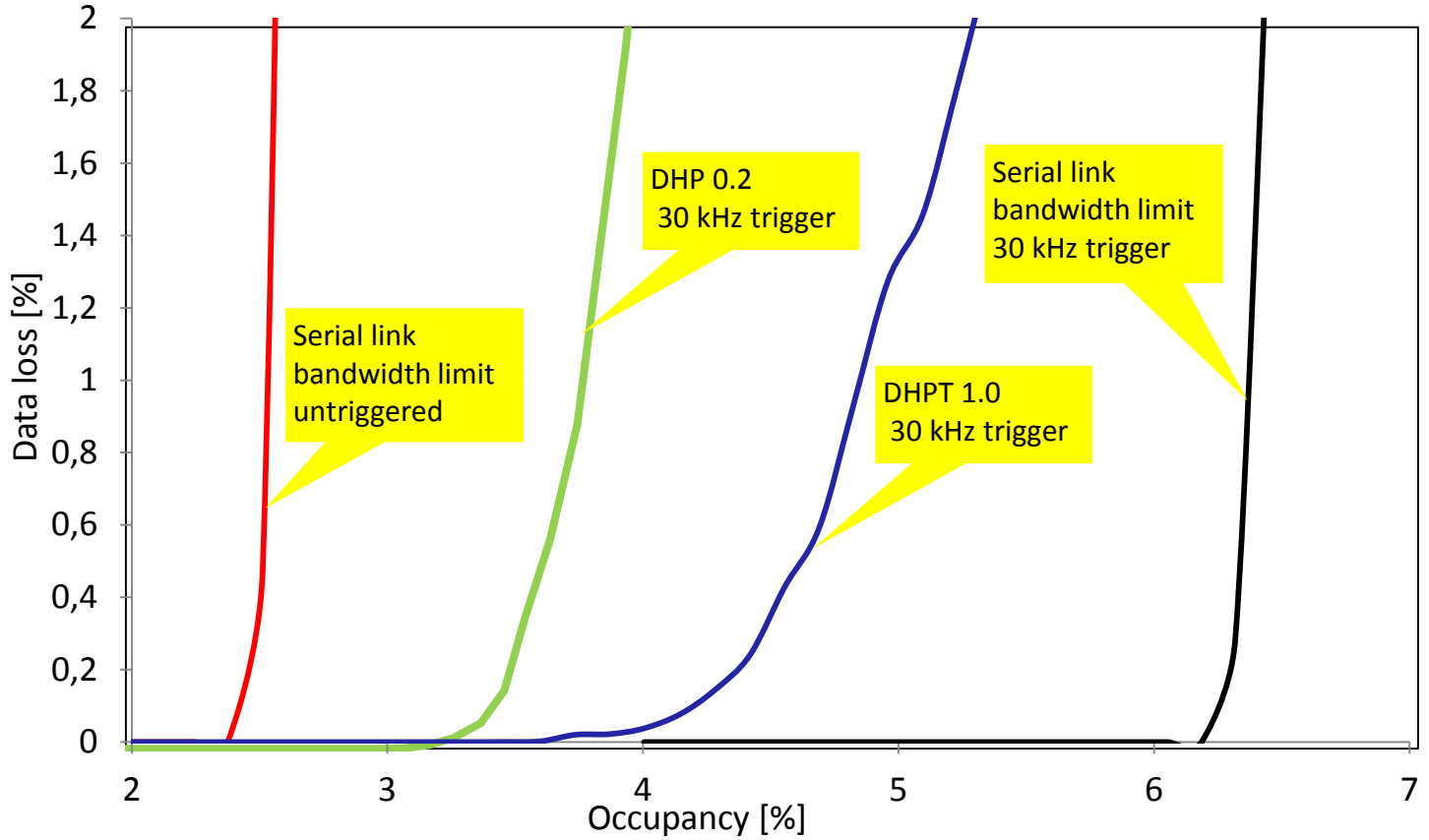
- Use TRG line to encode fast commands (8bits per row period @ 80 MHz)
- Manchester encoding → one 4 bit user symbol per row period
  - 01 → active user bit
  - 10 → not active user bit
  - DC balanced, run length ≤ 2
- Four independent commands possible
  - TRIGGER
  - VETO (start gated mode sequence)
  - FRAME_SYNC (send at the beginning of frame)
  - RESET

  Example (trigger command send): <reset><veto><trigger><frame> = 10 10 01 10

- Symbol synchronization (broken Manchester)
  - 000111<frame>, send as default
  - 111000xx → MEMORY DUMP command
- The FRAME_SYNC and RESET commands are still ORed internally with external RST and FCK lines

Expected DHPT 1.0 Data Losses

- FIFO 1: 64 FIFOs in front of the hit finder ➔ 256 words deep (DHP 0.2 → 16)
- FIFO 2: between hit finder and serializer ➔ 4096 word deep (DHP 0.2 → 512)



Interface to DHH

- LVDS inputs for timing and command
  - GCK: DHP Clock (76.35 MHz)
  - TRG: level sensitive trigger, defines timing and length of the read-out frame data
    ➔ will be changed to become a Manchester encoded command line (see Tomasz talk)
  - FCK: Frame sync: defines the frame size, resets internal counters periodically
    ➔ internal behavior may change
  - RST: Reset line: resets global counters
- JTAG
  - no changes
- Gbit Link
  - no functional changes ➔ optimize bias settings
  - PRBS-7 sync pattern for link testing with FPGA resources on DHH

Interface to DCD

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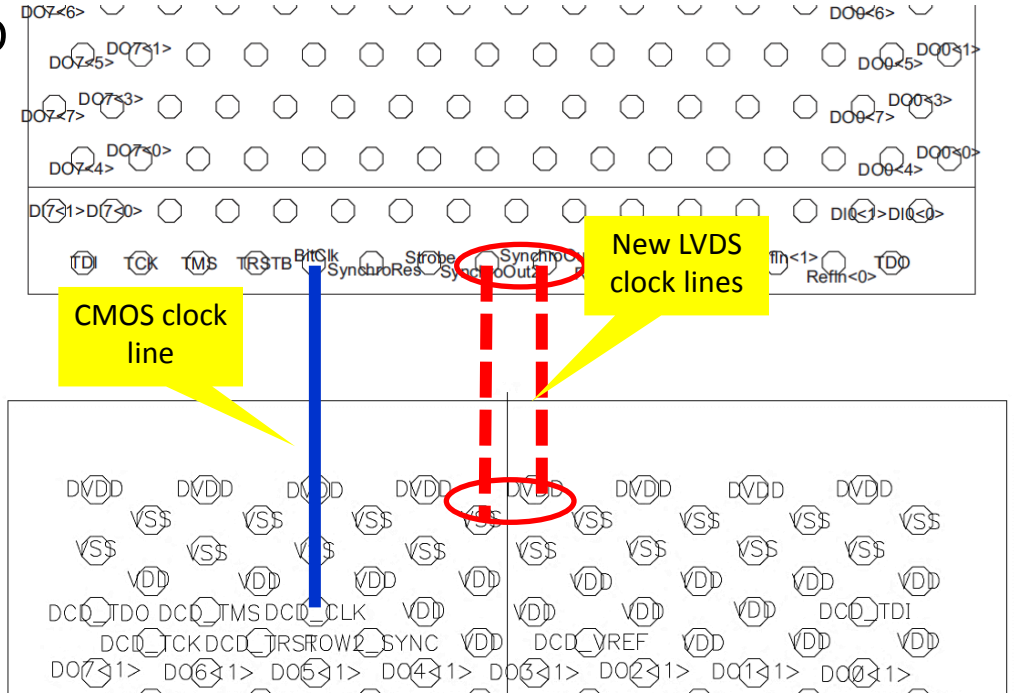
- JTAG
  - 1.8V CMOS
  - active **low** reset (TRSTB) ➔ DCDBv2
- Data_In (64x)
  - low swing single ended receivers
  - Vthr generated by DCD
  - **Data format as with current DCDBv2 / DHP 0.2**
    - 8bit parallel on DOx[7:0], signed integer (two's complement) [-127 .. 127]
    - higher I_{DEPFET} ➔ higher #ADC
- Data_Out (16x DAC bits, DCDclk, Row2Sync)
  - 1.8V CMOS
  - add LVDS version of DCDclk (pads to be defined ➔ DONE)
    - DCD side: unused strobe or sync pads
    - DHP side: redundant power pads

DCD – DHP Interface: Data Lines

- CMOS output of 320 MHz clock to DCD is critical (already seen on DHP 0.1)
  - ➔ Full custom CMOS driver
  - ➔ Add LVDS version of DCD_CLK
    - SynchroOut (P input)
    - SynchroOut2 (N input)
    - 200 Ohm termination on DCD



- Synchronization of data lines (DCD data and DHP Offset DAC data)
  - ➔Programmable delay lines on all in- and output signals (~200ps resolution, 16 taps)

DHP – DCD Interface: JTAG

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- The DCDB has a bug in the JTAG interface (does not comply to the JTAG standard)
- This is not fixed in the new DCD versions submitted in Mai
- JTAG standard:
  - Sample TDI data on rising TCK edge
  - Update TDO on falling TCK edge
- In some modes the DCD does the opposite (sample data on falling edge and output on rising edge)
- Can only partially compensated by a **programmable DCD_TCK inversion**

1. The DHP will still see the DCD_TDO on the wrong clock edge

➔ readback of the DCD has a risk to be compromised

2. The last DCD DHP pair sees the SwitcherB JTAG chain in-between ➔ SwitcherB

➔ This is potentially critical and needs verification of **DCDB to SwitcherB** JTAG communication

Known Minor Issues with DHP 0.2

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- Programmable delay elements
  - duty cycle distortion
  - control bit order
- Common mode block
  - bug in pedestal and common mode offset registers
- Frame sync
  - not correctly generated by internal counter
- Last row counter
- Fix behavior for short frames (< 32 rows)
- Pedestal memory gets corrupted after a reset in ACQUISITION mode
- AURORA desynchronizes at very high data rates (→ check if not a test system issue)
- Optimize bias current range for Gbit driver

Critical Issues for DHP Verification

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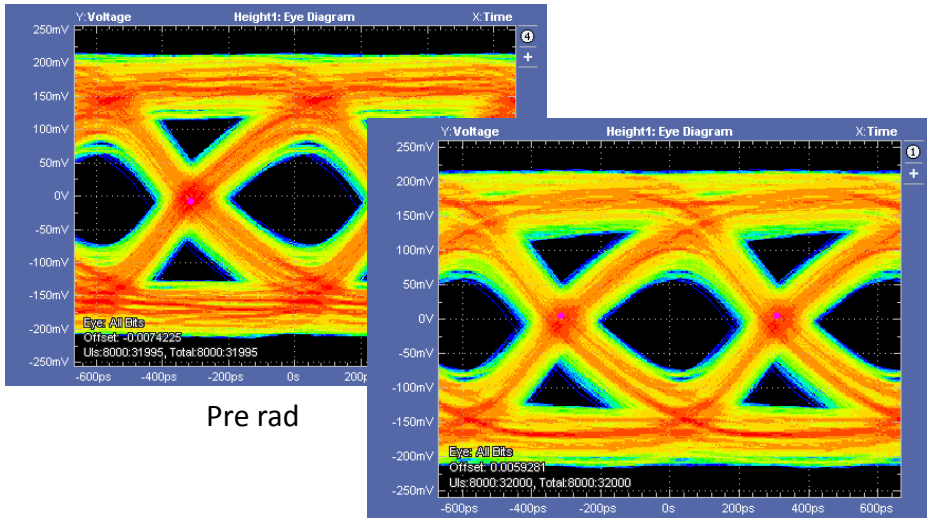
- SEU tolerance
  - ➔ Implement/revise mitigation strategies based on DHPT 0.1 measurements ➔ **DONE**
- TID tolerance
  - ➔ Measurements still pending ➔ **DONE (see next slide)**
  - ➔ Should be ok for digital core, add timing contingency for critical blocks (serializer, PLL, CML driver) ➔ **DONE**
- Behavior during switching of trigger (read-out) modes
  - ➔ Needs detailed verification ➔ **ongoing**
- Handling of buffer overflow
  - ➔ Add flags to frame header (or add frame footer) ➔ **ongoing**
- Gated mode operation (switcher sequencer)
  - ➔ Verify foreseen implementation with Switcher logic ➔ **ongoing**

Status wrt. DHPT 1.0 design review

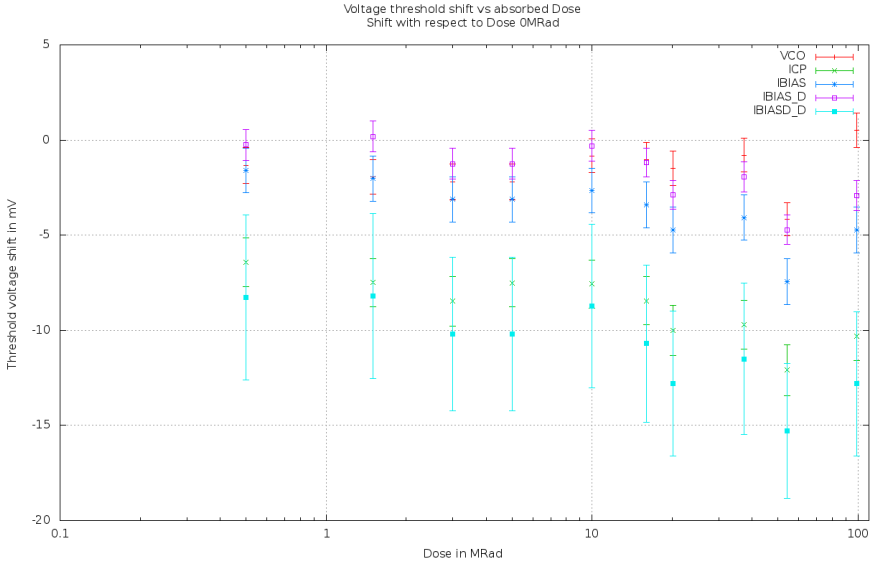
DHPT 0.1 X-ray Irradiation

- TSMC 65nm TID tolerance:
  - V_{THR} shift (wide pMOS and nMOS only)
  - PLL + Gbit link performance
- Up to 100 Mrad (60keV X-ray tube, Karlsruhe)
- Dose rates: ~300 kRad/h (initial) → ~2Mrad/h (end)
- Annealing after each step: 80°C for 100 mir



Pre rad

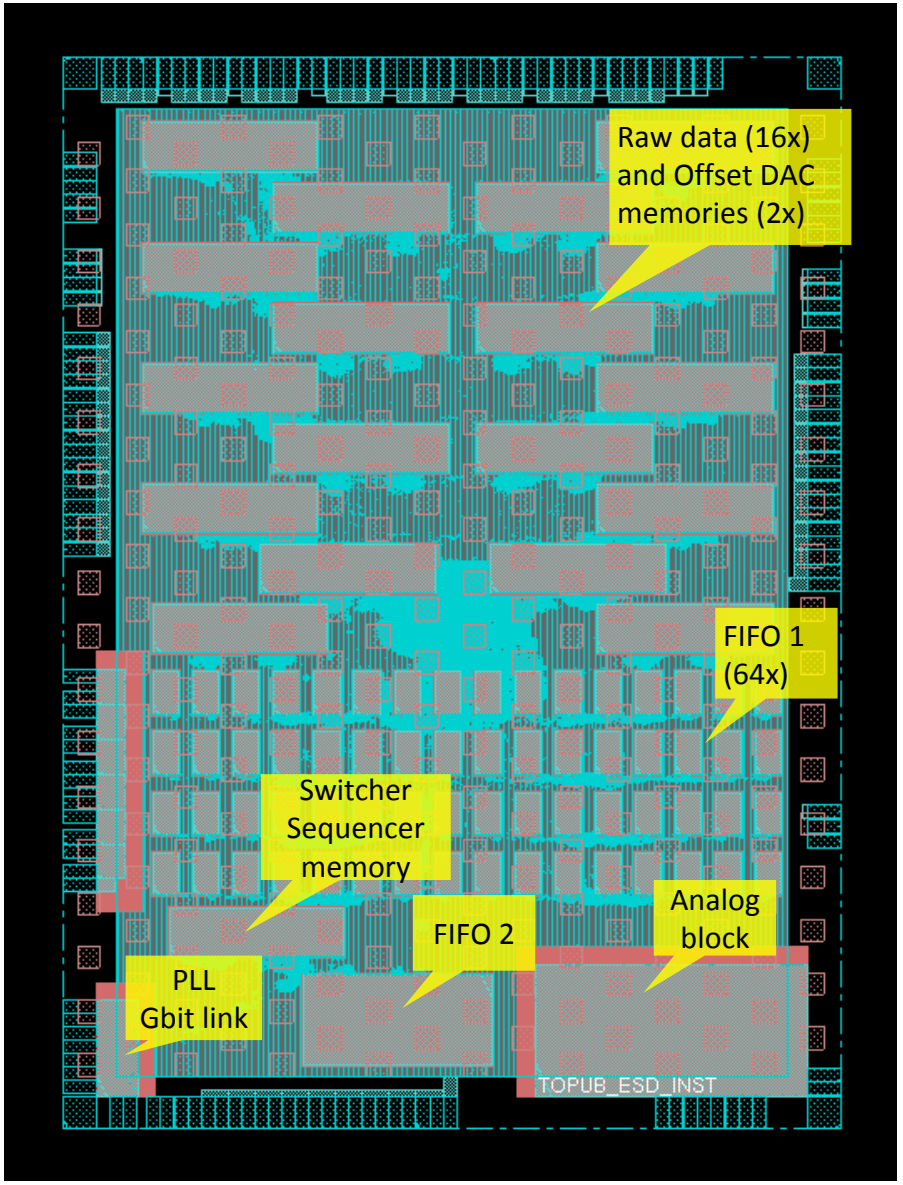
100 Mrad



No TID induced degradiation observed up to 100 Mrad

DHPT 1.0 Implementation Status

- All IP blocks placed
  - Analog block (U Barcelona)
  - PLL + Serializer + Gbit link
  - IO (cores & bump pads)
  - Compiled memories
- Routing ongoing



DHPT 1.0 Planning

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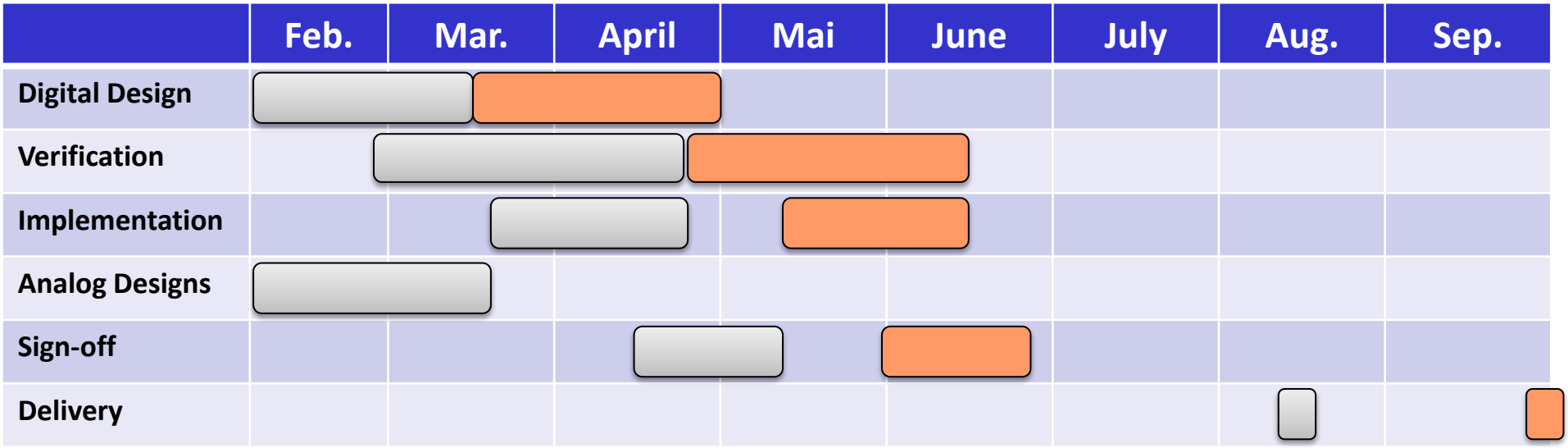

- Changes wrt. to time line shown on B2GM in March 2013
- TSMC 65nm submission schedule (via chip broker): two times a month
- Usually ~12 weeks turnaround (might get a bit delayed due to bumping)

Status

- DHPT 1.0 design almost done
  - All major changes implemented
  - Verification ongoing (!!!)
- Submission planned for beginning of July
  - 12 weeks turn around (➔ Sep/Oct)
  - Cost: 50 kEUR + bumping (~5-10 kEUR)
  - MPW run: 100 chips
  - Extra wafer: 7 kEUR (➔ additional 100 chips)
  - Max. 20 wafers from MPW run

➔ Need to check when the order for extra wafers need to be placed at the latest

- Test system preparation: New wirebond adapter for DHPT 1.0 testing
  - Footprint same as DHP 0.2
  - Add lines for LVDS DCD clock

Backup

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Neutron dose evaluation

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Neutron levels

18

Number of Neutrons **per second per cm²**
Unfortunately, **low statistics**

		Switcher		DCD		DHP	
		-Z	+Z	-Z	+Z	-Z	+Z
Touschek	LER	829	2724	2232	2009	2605	2158
Touschek	HER	473	473	744	371	0	148
Beam-Gas Coulomb	LER	2133	473	744	0	1786	297
Beam-Gas Coulomb	HER	0	0	0	0	0	0
Radiative Bhabha	LER	473	711	297	1488	1488	1786
Radiative Bhabha	HER	947	5687	3572	1334	3572	4019
KoralW		1049	1023	1543	1730	1859	2100
Total (Neutrons per s per cm²)		**5904**	**10068**	**9132**	**6932**	**11310**	**10508**

About 10^4 Neutrons per second per cm² from background

SEU Tolerance

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- Cross section measured 24 GeV pion beam line
- SUE rate extrapolated by assuming 10^4 neutrons s^{-1} cm^{-2}

Memory type	Size	Cross section	Mean time between SEU per one chip	Mean time between SEU for whole detector	Refresh rate	Mitigation	Critical?
Raw data buffer	0.5 Mbit	σ_{SRAM}	~30 min	13 sec	20 us		
Pedestals	0.5 Mbit	σ_{SRAM}	~30 min	13 sec	~15 min	Humming code protection. Single SEU corrected every 20 us, Double SEUs are detected.	yes
Configuration Register	368 bit	σ_{FF}	490 day	3 day	No	Triple redundancy, protects against single SEU.	yes
Data processing logic	45 kbit	σ_{FF}	4 day	36min	20 us		

SuperKEKB timing & DHP Clock Frequencies

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- SuperKEKB **RF frequency** f0 = **509 MHz** (508.89 MHz precisely)
- Number of slots per cycle: 5120
- Circulation time: 10.059 µs
- System clock f0/12 = 42.3 MHz (or f0/4, f0/8, f0/16, f0/256)
- Abort gap: 200 ns (~100 bunches)

- DEPFET read-out **synchronous** with **two beam circulations** (192 rows):
  Frame clock (FCK) = ½ x 509 MHz / 5120 = 49.7 kHz
  Row clock = ½ x 509 MHz / (5120/192) = 9.5 MHz
  DCD clock = row clock x 8 x 4 = 305.4 MHz
  DHP clock (GCK) = row clock x 8 = 76.35 MHz (= 0.15 x f0)

Switcher Standard Operation

For non-overlapping gate signals it is essential that the *rising* edge of StrG has to be *after* the falling edge of CLK. The Gate output is switched off as soon as the next Gate is switched on. See figure 3.3.

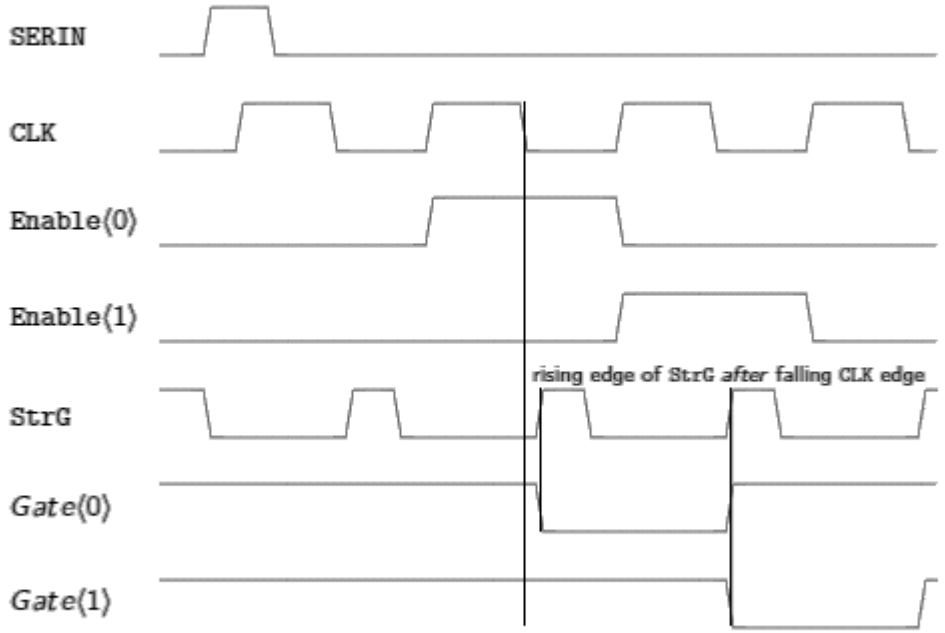

Figure 3.3: Non-overlapping gate strobe timing.

Switcher Gated Mode Operation without Read

The gated mode without read-out is enabled by stopping CLK while StrC is high and StrG is running. It is disabled by switching StrC to low and sampled by the falling edge of StrG. A minimum length of 8 falling StrG is required for a gated mode cycle.

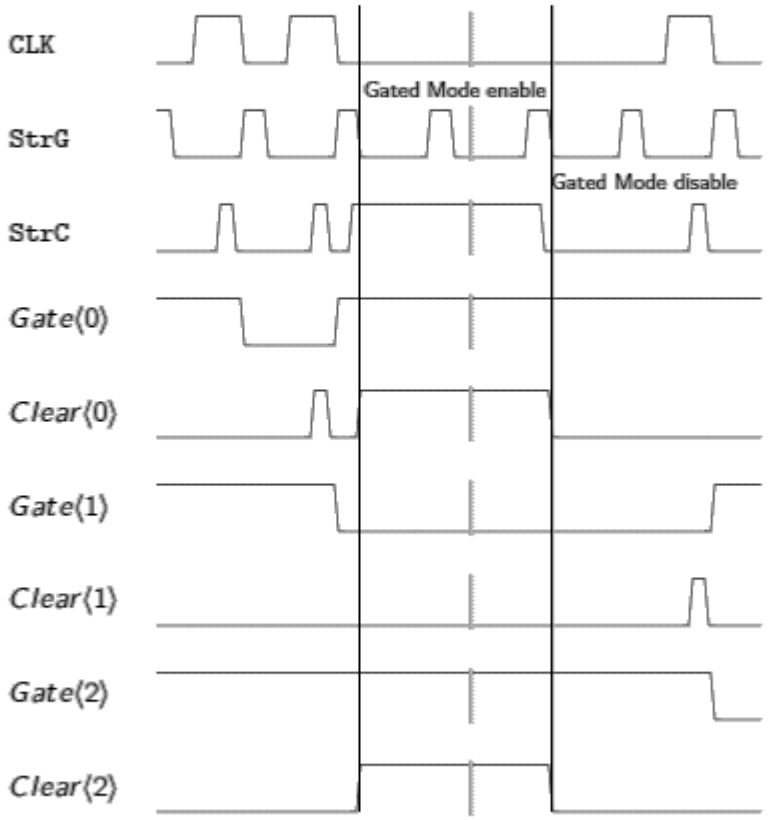

Figure 3.8: Gated mode timing without read-out

- Enter veto mode
  - Stop Switcher clock
  - Keep Gate strobe running
  - Keep Clear strobe high
- Veto length at least 8 Gate strobes
- Leave veto mode
  - Set Clear strobe low
  - Resume Clock operation

Switcher Gated Mode Operation with Read

Gated mode with read-out is trigger by a high level on CLK or StrC at the falling edge of StrG. The clock continues to run.

The clear changes to high level immediately on non-active channels (see Clear<0>). Channels currently enabled (low gate voltage) will be switched to gated mode when they are disabled (see Clear<1>). No clear pulse is applied!

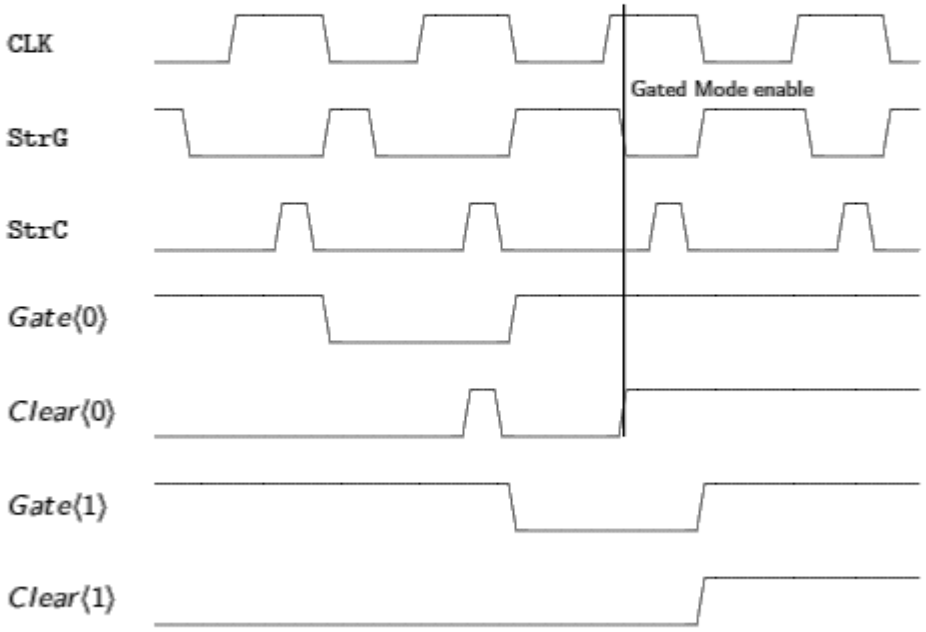

Figure 3.9: Gated mode timing with read-out

- Enter veto mode
  - Extend Gate strobe width across rising clock edge or Clear strobe edge
  - Keep clock running
- Veto length requirements?
- Leave veto mode
  - Remove Gate strobe overlap?

➔ No clear during veto mode

Address Naming Convention

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- Electronic channels:
  - 8 bit Switcher channel address: 0..191 (6 x 32 ch. Switcher)
  - 8 bit DCD channel address: 0..255 (one DCD → one DHP→ one Link)
- Physical (pixel) addresses:
  - 10 bit pixel row address: 0..767
  - 6 bit pixel column address: 0..63
  - this format is used for the hit data words inside the DHP

DHP Data Format Options

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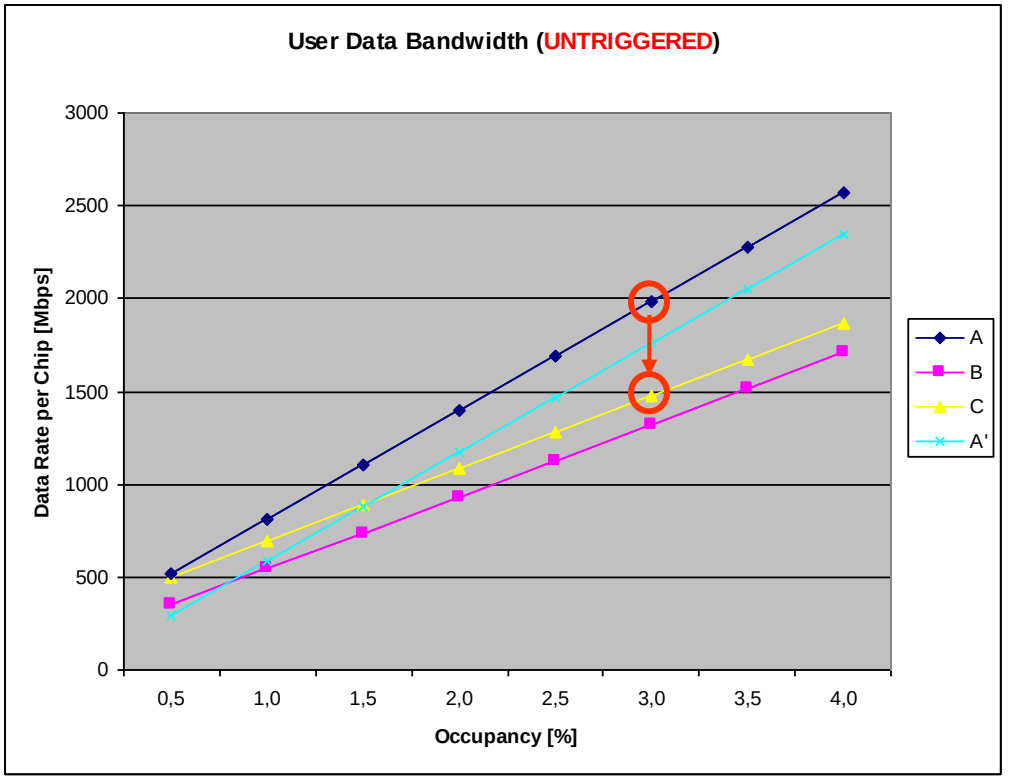
- Generic 24 bit hit data format: <10b row><6b col><8b ADC>
  - 10 bit row address: 768 pixels
  - 6 bit column address: 64 pixels
  - 8 bit ADC range: 0..255
- “Row Header” format
  - send row address only once and send data words with column address and ADC value
  - 16 bit length for both words
  - row header (including c.m.): < 10b row><6b cm>
  - data word: <6b col><8b ADC><2b reserved>
  - disadvantage: one cannot distinguish row headers form data words by their structure (maybe heuristics can do)

DHP Data Format Options

- Re-order addresses bits to define flags for bits row headers and data words
  - row header: <row flag = 0><9b row><6b cm>
  - data word: <data flag = 1><7b col><8b ADC>
  - send row header every 128 (and not 256) pixels (adds some overhead)

- Data formats shown in the plot
  - A: generic 24b data (+ 24b c.m. word per row)
  - A': A without c.m. word
  - B: 10b/6b row/col addresses
  - C: reordered 9b/7b row/col addresses

➔ data reduction of 26% @ 3% occ. for a change from A to C



DHP 0.2 Data Format

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- Frame Header (32 bit): <data type><res.><chip ID><frame ID> ➔ will be revised
  - data type (3 bit): [raw data, processed data]
  - reserved (5 bit)
  - chip ID (8 bit)
  - frame ID (16 bit)

  ➔ will always be send at start of a new frame, independent of trigger
- Row Header (16 bit): <flag><row address><common mode>
  - flag (1 bit): 0 → row header
  - row address (9 bit)
  - common mode (6 bit)

  ➔ will only be send if hit data for the active row is available
- Data Word (16 bit): <flag><column address><ADC>
  - flag (1 bit): 1 → hit data
  - column address (7 bit)
  - ADC (8 bit)