PXD6 long matrix status and testing preparations

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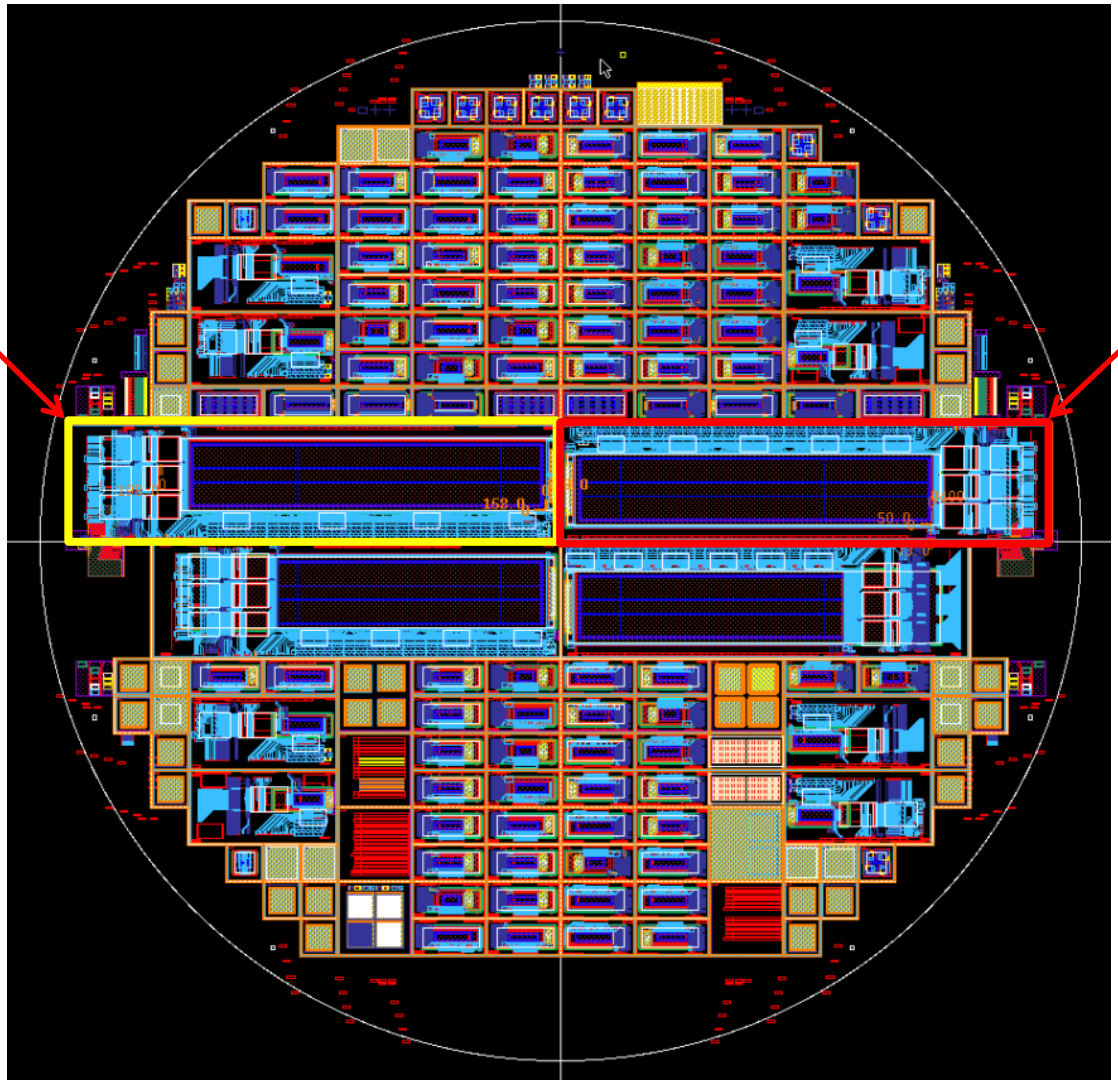
Outline

- PXD6 status: batch II & III
- PXD6 large matrices layout
- Testing plans
- Test Systems, in particular Hybrid 6.0
- Summary and Outlook

PXD6 batch III

2 SOI wafers with DHP0.2 footprint waiting for Cu deposition (will be deposited soon).



PXD6 batch II & III

Differences between batch II and batch III

Batch II:

- 4 wafers (3 SOI + 1 ref)
- no DHP footprint
- shorts in the large PXD6 matrices
- none working large PXD6

Batch III:

- 2 wafers (SOI) à 4 large PXD6
- DHP footprint
- changed Aluminium 2 layer in order to deposit copper
- Copper pads are included (in order to solder the ASICs)

Current status:

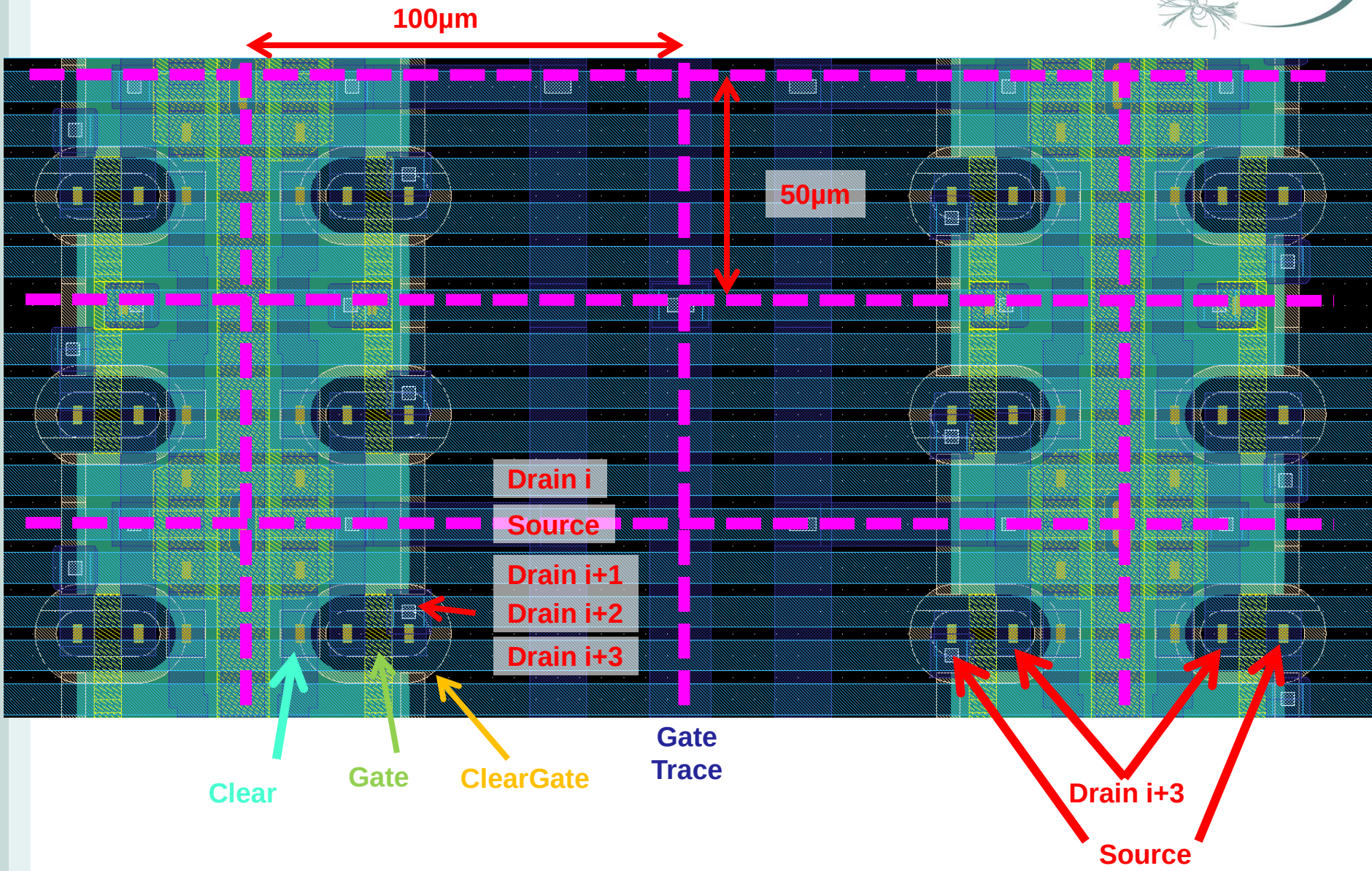
2 PXD6 matrices are tested and work properly

Copper layer is still missing => will be done soon

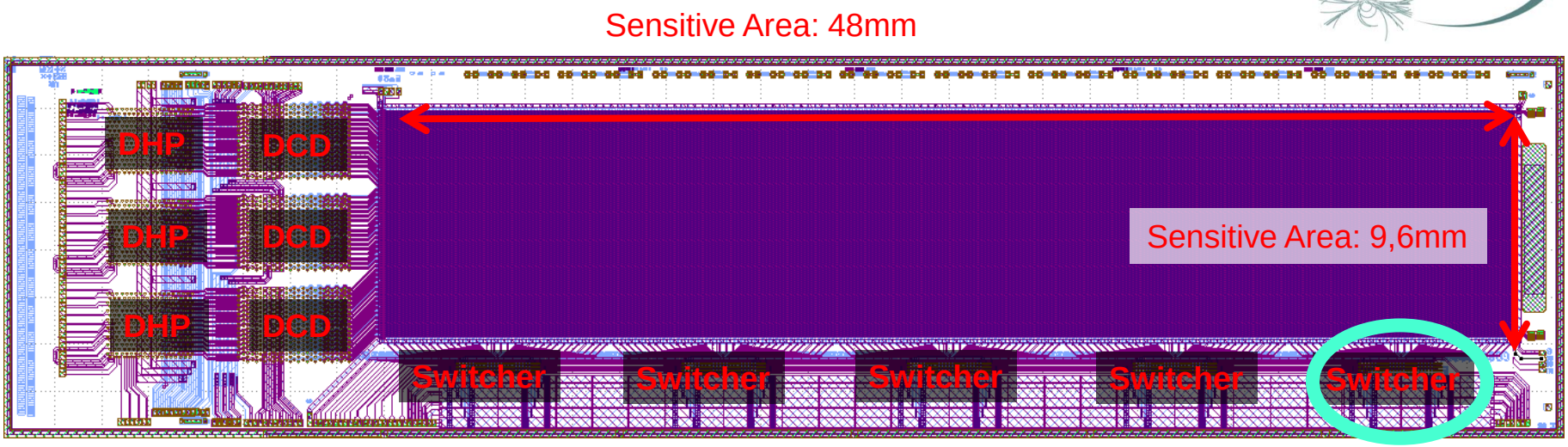
PXD6 – I00

- Capacitive coupled clear-gate (provides Clear mechanism but harms Gated-Mode Operation)
- Enhanced drift field
- 50 x 100 μm^2 pixel size
- 192 x 480 pixels
  - 768 drain lines → 3 DCDs & 3 DHPs
  - 120 gate/clear lines → **4 SWITCHERs**

PXD6 – I00


100µm
50µm
Drain i
Source
Drain i+1
Drain i+2
Drain i+3
Clear
Gate
ClearGate
Gate
Trace
Drain i+3
Source

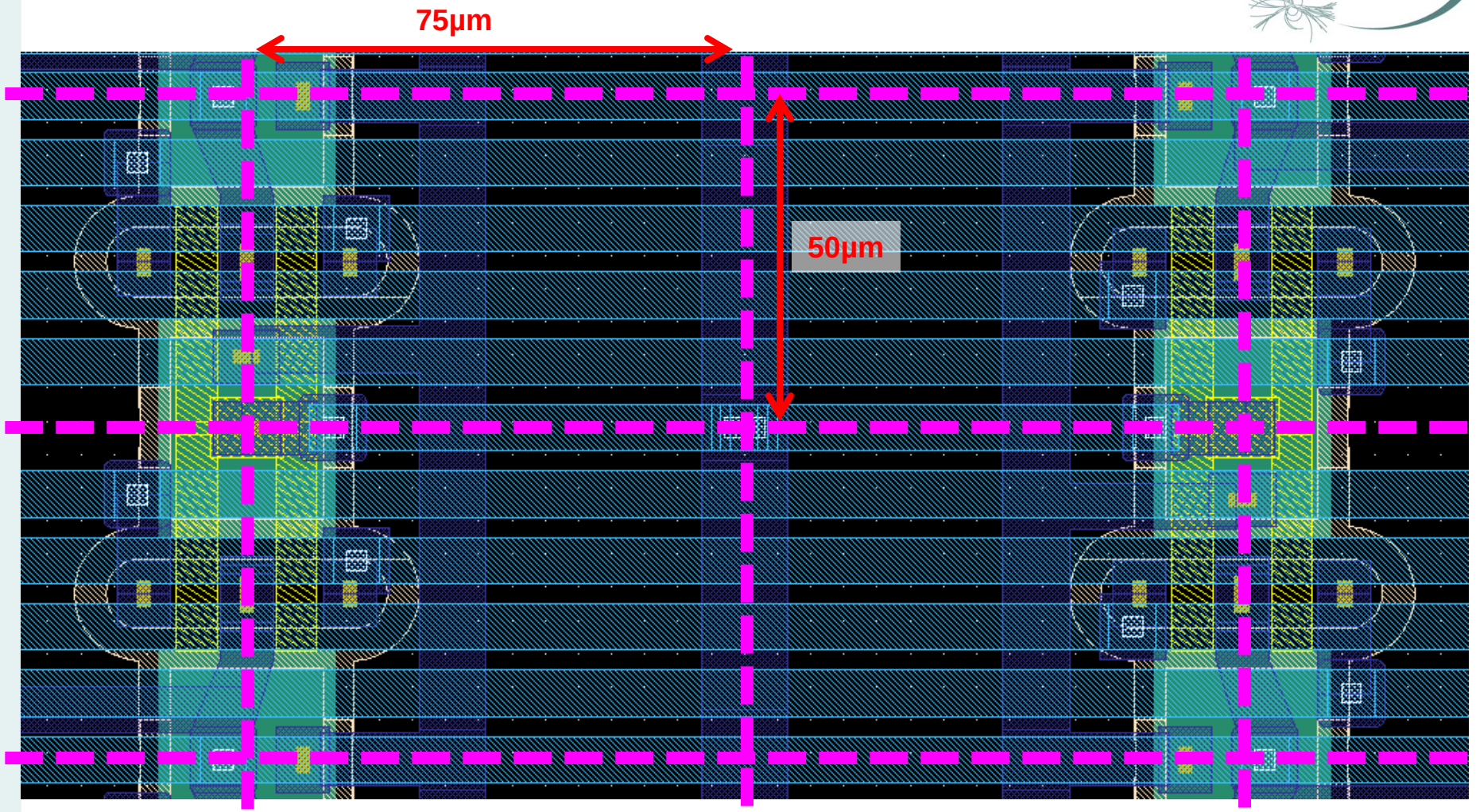
PXD6 – I06



- **Standard Belle II design**
- 50 x 75 μm^2 pixel size
- 192 x 640 pixels
  - 768 drain lines → 3 DCDs & 3 DHPs
  - 160 gate/clear lines → **5 SWITCHERs**

Both matrices have the same sensitive area

PXD6 – I06



PXD6 Status Verification Tests

PXD6 long matrices testing plans

1. Verify the status of the matrices on the wafers (pretested after Al2)

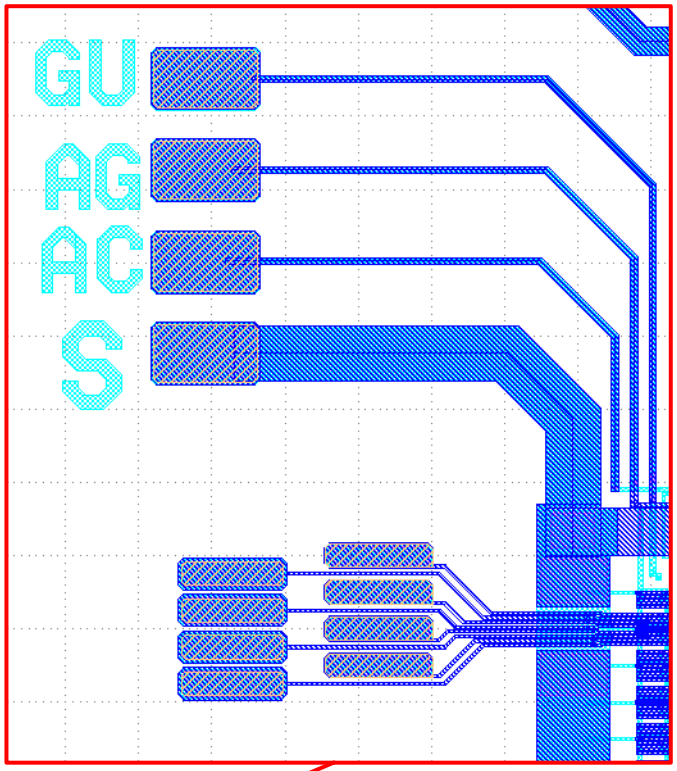
2. Measure the output characteristics for all the (768) DEPFETs on one electrical row

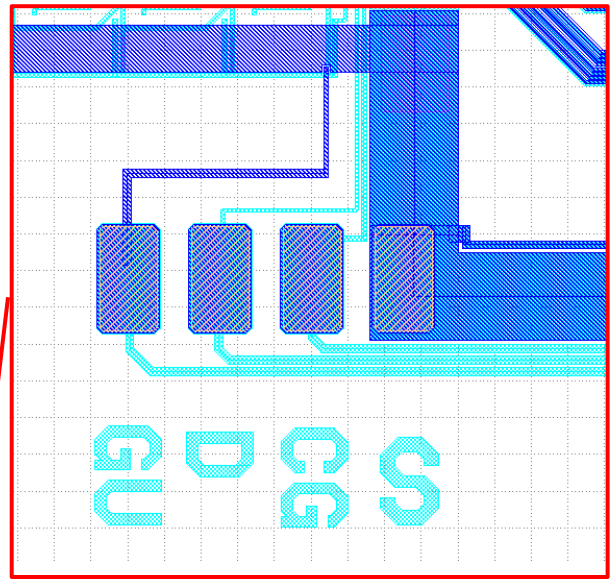
3. Check for shorts/opens in the two metal layers in the peripheral region – to be performed at ATG, as in the case of the EMCM

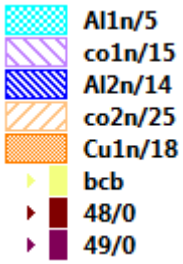
- Instrumentation for tests no. 1. and 2.:
  - Probe station PA200 equipped with two flying needles and four static needles
  - Keithley 4200 SCS measurement system

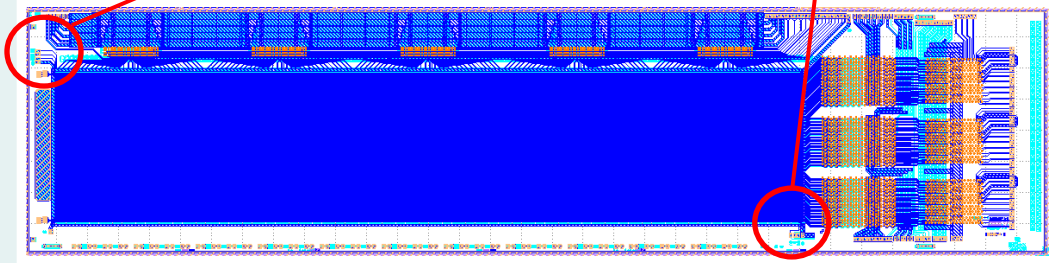
- Instrumentation for test no. 3.:
  - ATG Flying probe system (S2 machine – ref. to C. Koffmane's talk)

Verification of the PXD6-batch III matrices' status [I]





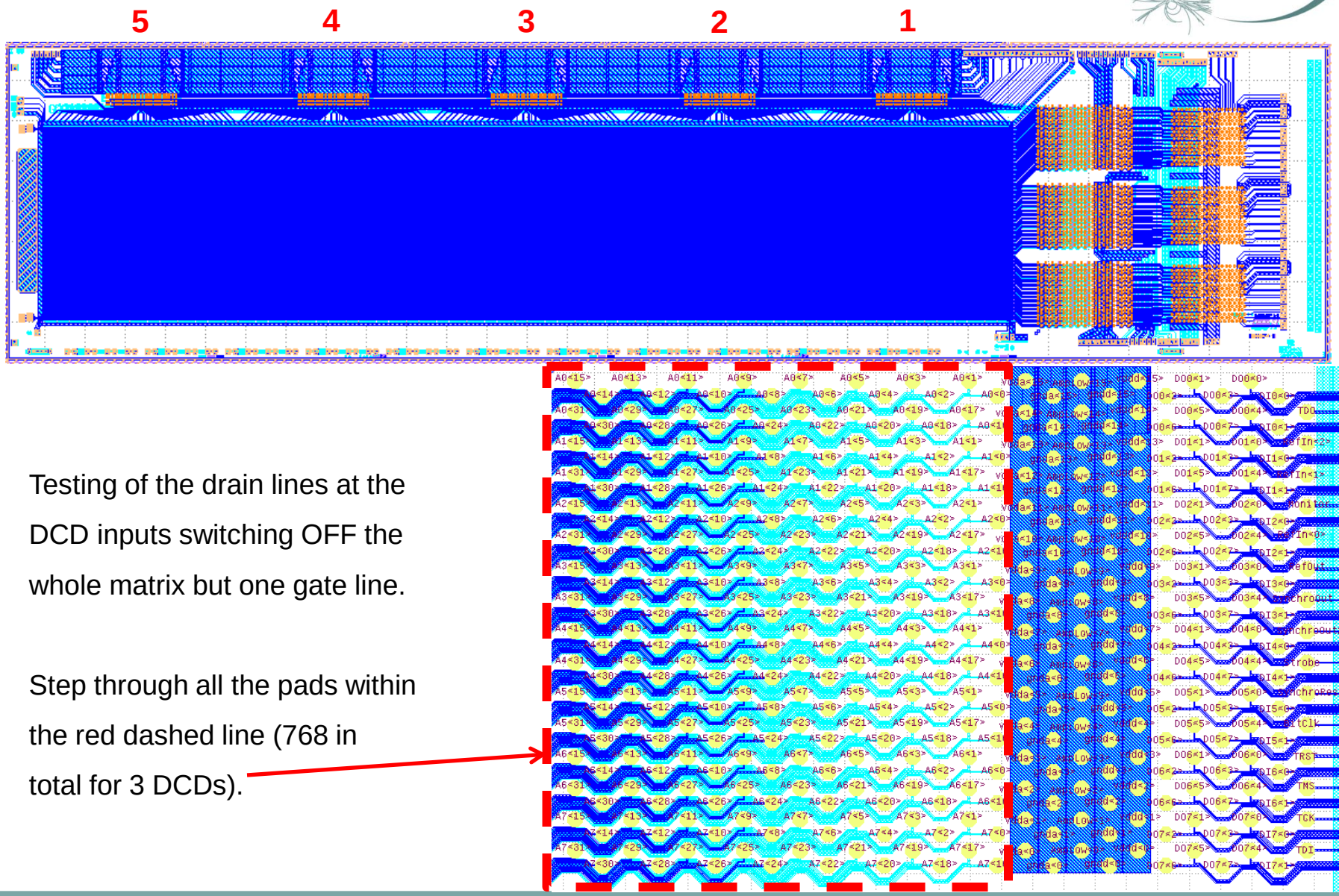




Verify the status of the matrices on the wafers measuring the characteristics of:

- All Gates vs All Clear (bulk)
- All Gates vs Clear Gate
- All Clears vs Source
- All Clears vs Clear Gate

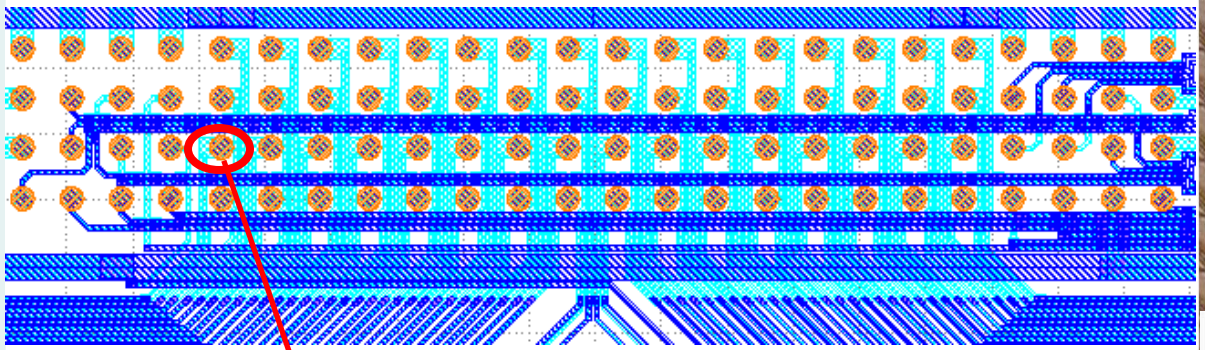
Verification of the PXD6-batch III matrices' status [II]

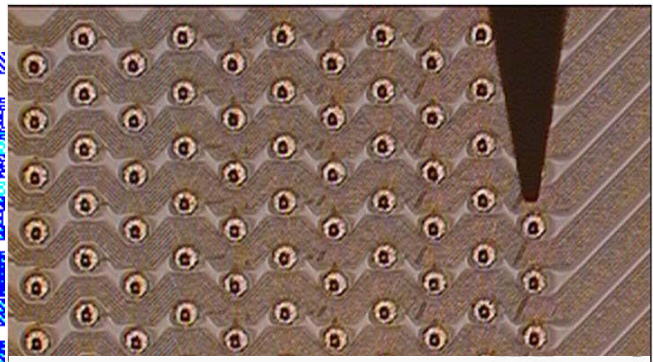


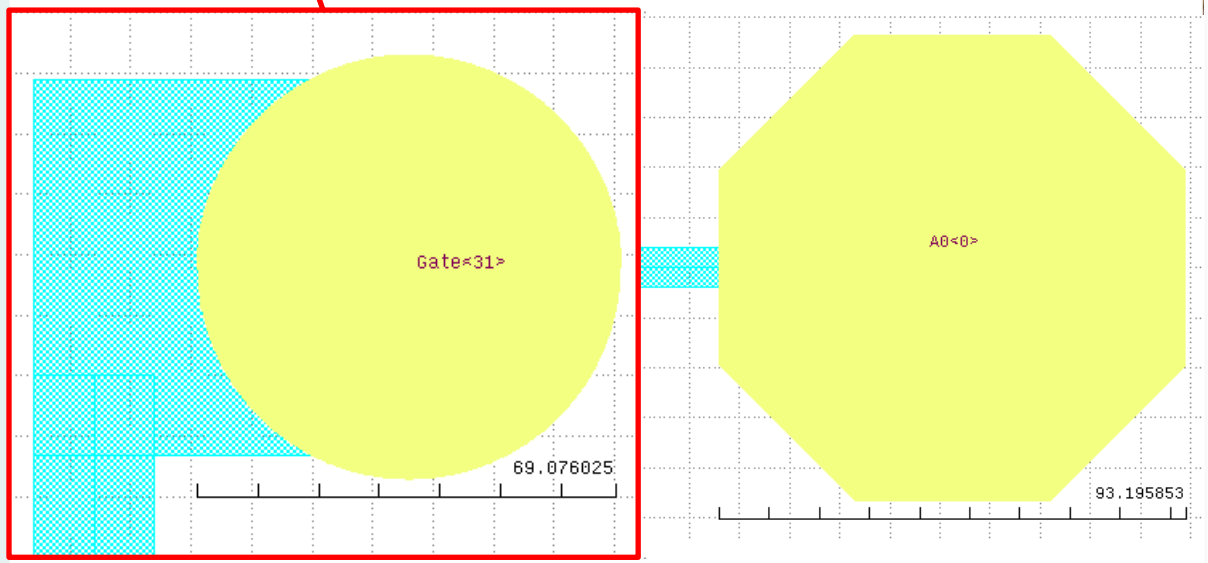
Testing of the drain lines at the DCD inputs switching OFF the whole matrix but one gate line.

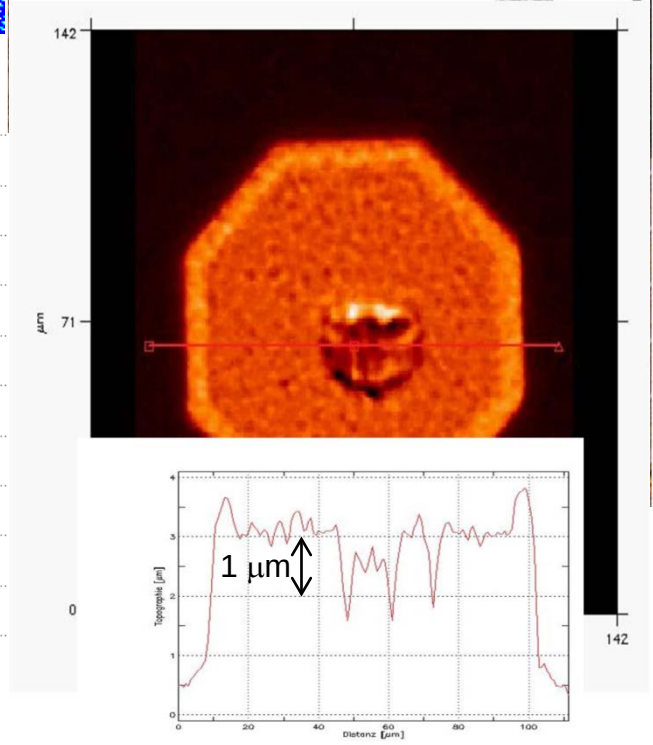
Step through all the pads within the red dashed line (768 in total for 3 DCDs).

Challenges of the testing









SWITCHERB pad

DCDB pad

Test Systems

- EMCM
- Hybrid 5
- Hybrid 6

EMCM, Hybrid 5, Hybrid 6

	EMCM	Hybrid 5	Hybrid 6
Matrix	Small	Small	Large
DCD	1 (4) (128 of 256 channels)	1 (128 of 256 channels)	3
DHP	1 (4) (128 of 256 channels)	1 (128 of 256 channels)	3
Switcher	1 (6) (16 of 32 channels)	1 (16 of 32 channels)	4 OR 5
Connector	Kapton DataPatchPanel (DPP) – 2Infiniband PowerPatchPanel(PPP) – MircoDSub	2 Infiniband (data) Samtec IPD1 (Power)	4 Infiniband (data) MicroDSub (Power)
DHH	✔	✔	✔
DHH Emulator	✔	✔	NO (3 DCDs, DHPs)

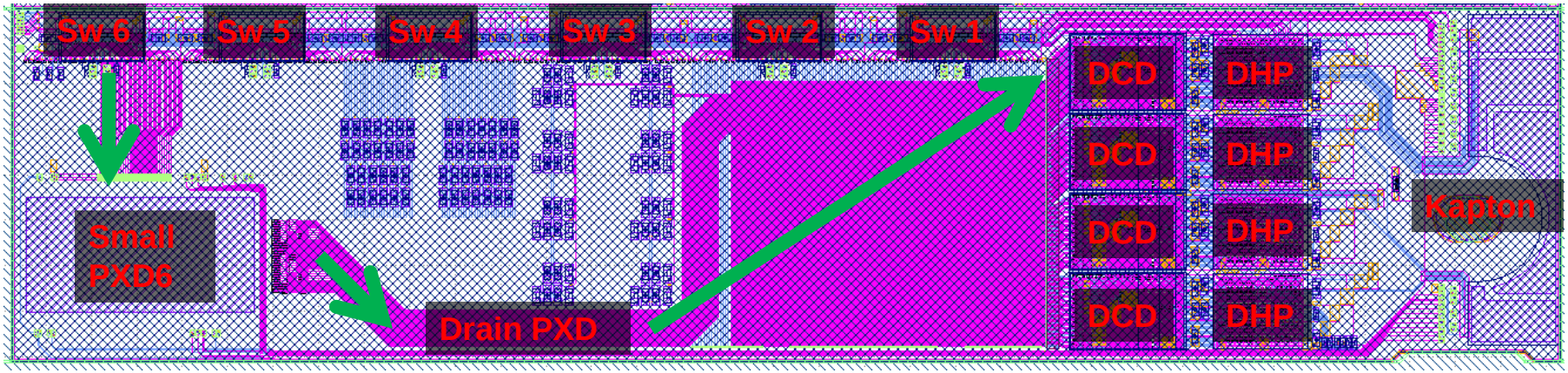
Almost same setup : 128 drains, 1 Switcher, small PXD6
Difference: Kapton

Same power cable as for EMCM PPP

Same Infiniband cable as for hybrid 5

EMCM

See Christian Koffmane‘s & Laci Andricek‘s talk



1 Switcher (only 16 of 32 channels)

1 small PXD6

1 DCD (only 128 of 256 channels)

1 DHP (only 128 of 256 channels)

Kapton (Power & Data)

DHH / DHH Emulator

Operation similar to hybrid 5

Possibilities to solder:

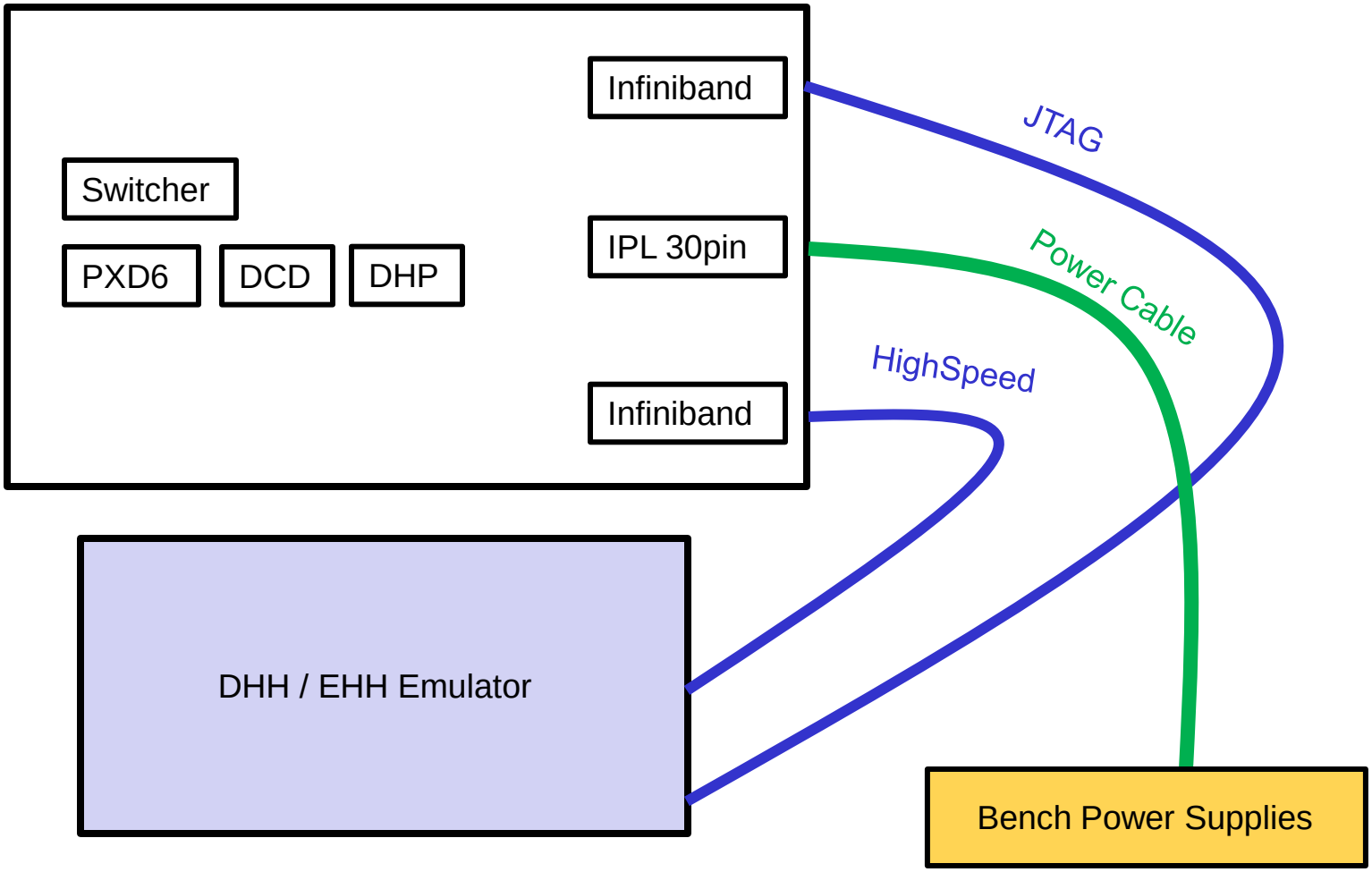
6 Switchers (check outputs by external PCB (wirebonds)

4 DCDs

4 DHPs

Hybrid 5

See Florian Lütticke‘s talk



Hybrid 6

There are two large PXD matrices working (75µm x 50µm & 100µm x 50µm (CC))
(I06 & I00)

=> For the DESY testbeam (2014) 2 PCBs are required (mirrored)

- 4 Infiniband cables (High Speed DHPs, JTAG DHPs, Switcher Control, Switcher JTAG)
- Power connector
- Cooling (DCDs & DHPs and Switchers)

Plan:

DHP controls Switcher (StrG, StrC, Clk, SerIn, SerOut)

External FPGA provides JTAG for Switcher (TDI, TDO, TMS, TCK, TRST)

Problem:

- DHP does not support GatedMode operation but DHPT does – finished soon enough (Sep 13)?

Is this a serious problem?

JTAG

JTAG for switchers is required for boundary scan and configuring termination resistors …

=> JTAG will be provided by the **DHH** (in consultation with Igor Konorov)

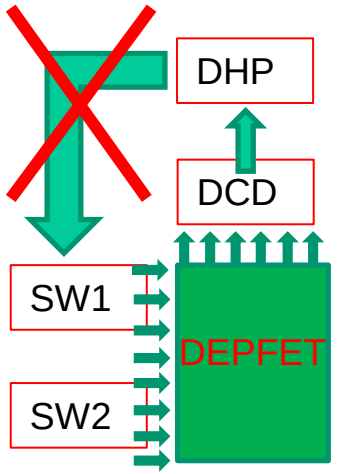
Therefore, an additional Infiniband Connector is required

Switcher Control

DHP does not support GatedMode operation for Switchers

DHPT supports GatedMode Operation => will it be ready (Sep13)?

Control Switcher by **DHH** => Can switch into GatedMode



Switcher Control

Switcher control lines (controlled by DHP or by DHH => discussion was already in the DEPFET-LAB Evo Meeting (March 1))

Both? (either DHP or DHH (online switching)) => Multiplexer needed

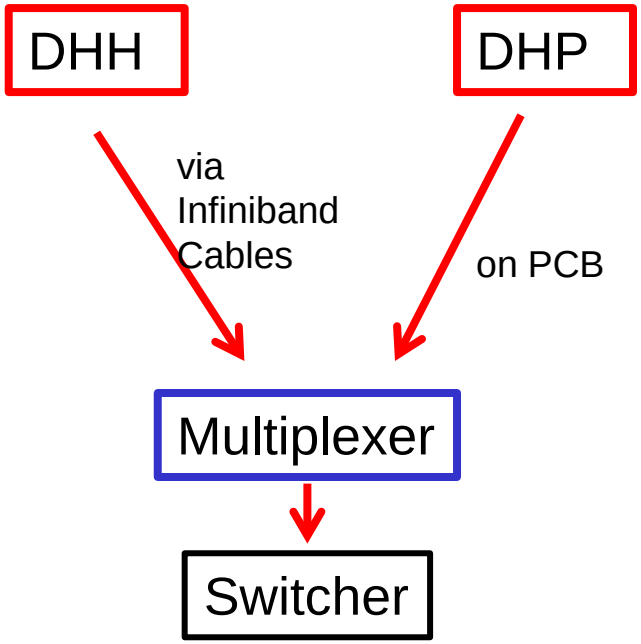
Power provided by the Polycover channel of the LMU Power Supply (also included in PowerCable)

Switcher signals:
SERIN
SEROUT
STRG
STRC
CLK

Need not be provided externally But for GatedMode operation

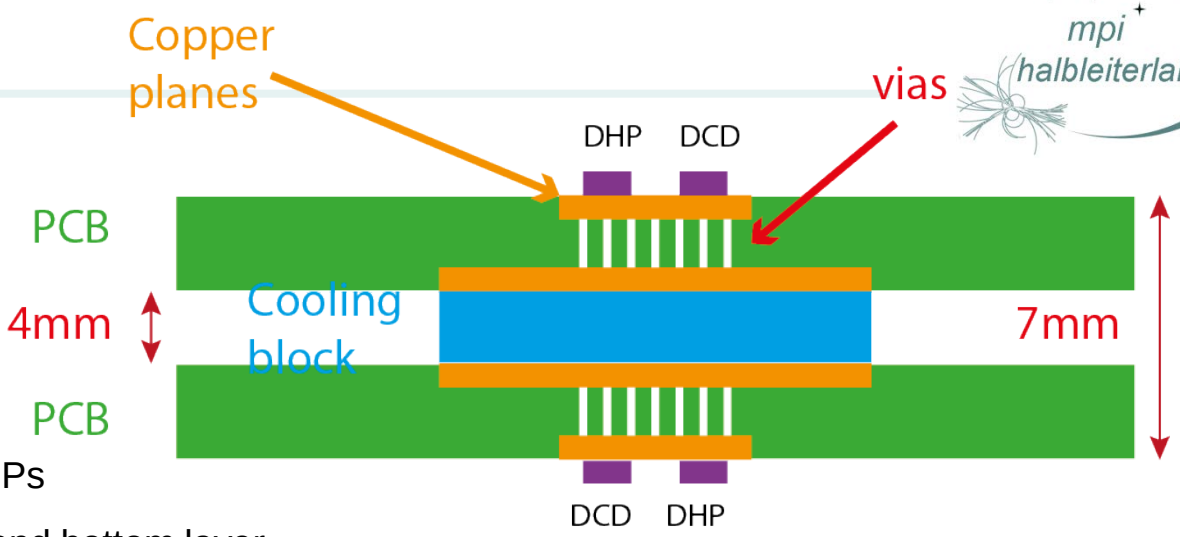
JTAG:
TDI
TDO
TCK
TMS
TRST

Must be provided externally



Hybrid 6

Cooling



Cooling block on backside

Cooling of 3 DCDs and 3 DHPs

Large copper planes on top and bottom layer

Heat transfer between top and bottom layer by Vias

(same as for hybrid 5)

Diameter (pipe) 1mm

Either fluid or CO2

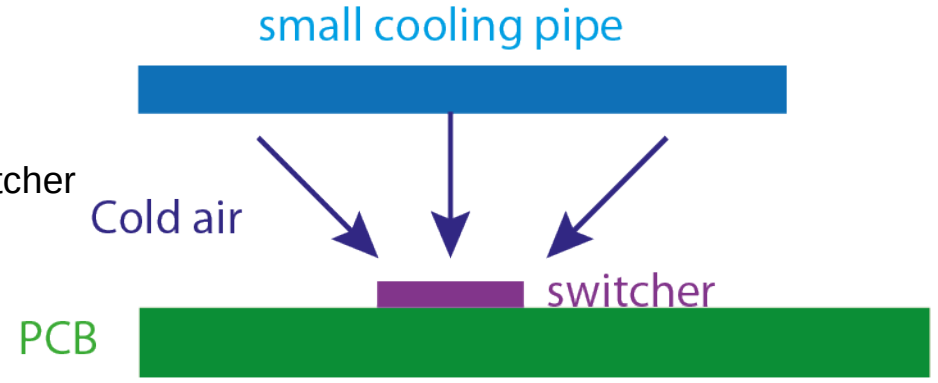
Thickness 4mm (PCB: 1.5mm => distance between PXD detectors: 7mm)

Additional Switcher cooling

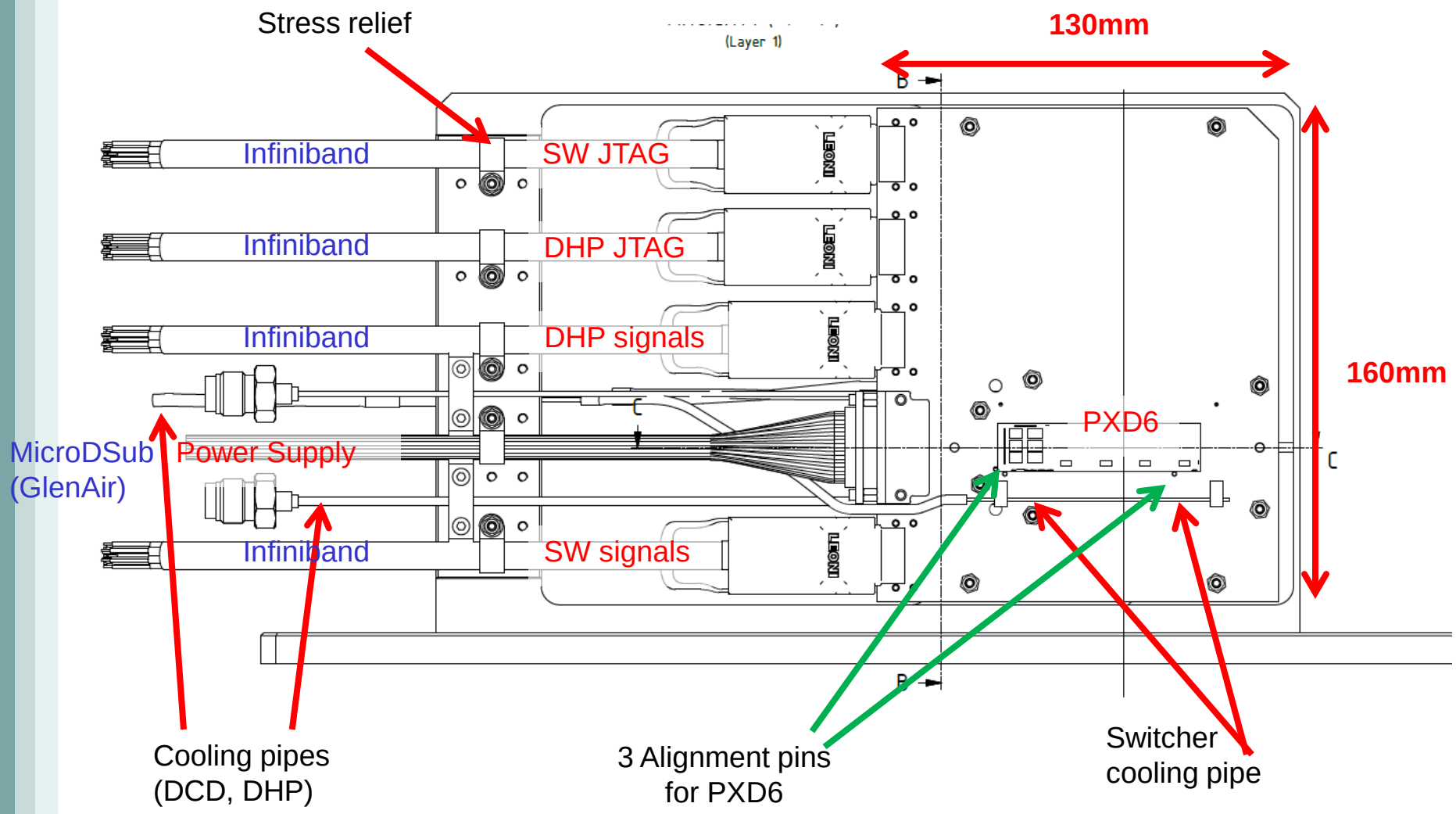
small pipe with ‚holes' installed above the switcher

air flow

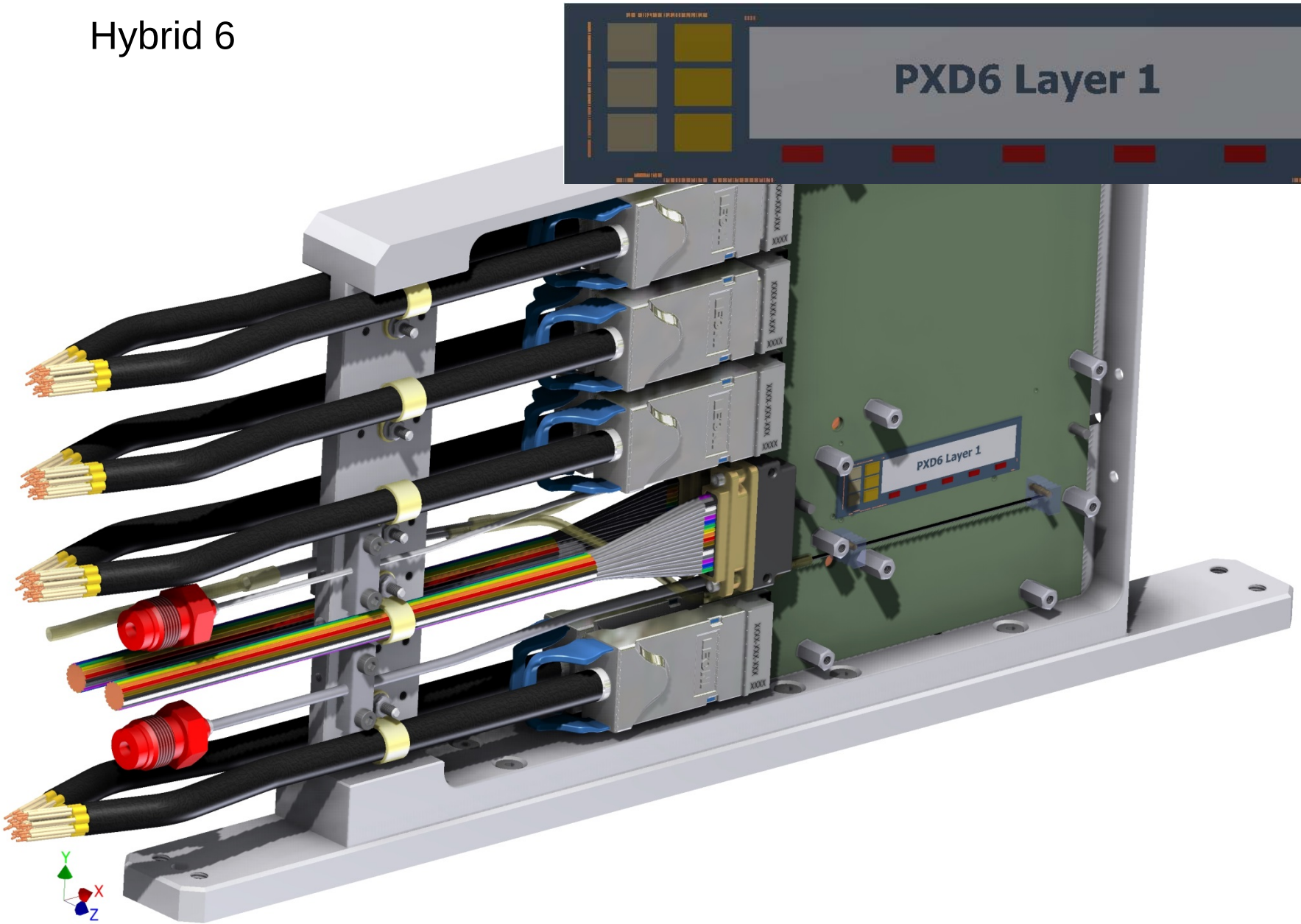
easily removable



Hybrid 6

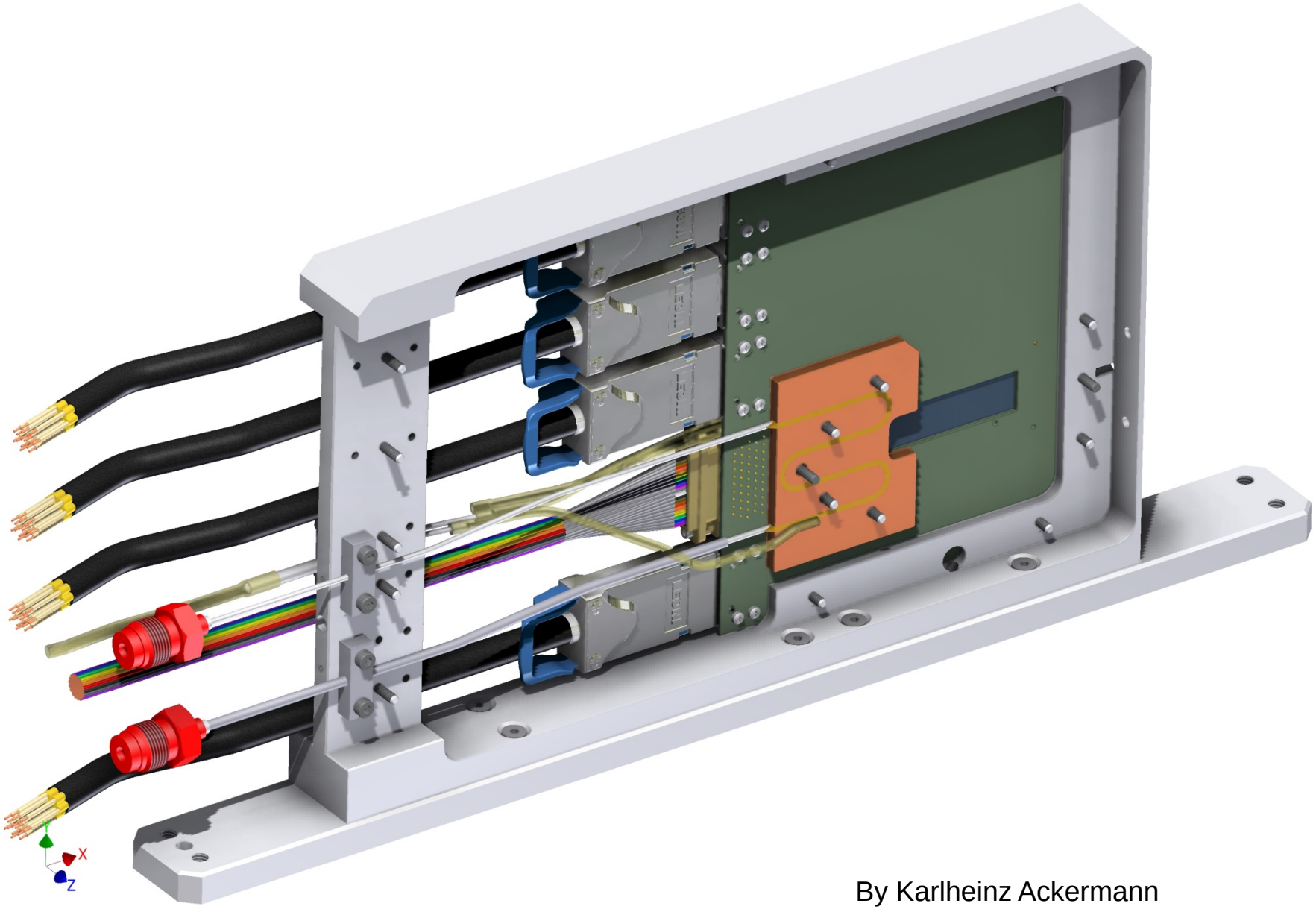

Stress relief
130mm
160mm
Infiniband
SW JTAG
Infiniband
DHP JTAG
Infiniband
DHP signals
MicroDSub
(GlenAir)
Power Supply
Infiniband
SW signals
PXD6
Cooling pipes
(DCD, DHP)
3 Alignment pins
for PXD6
Switcher
cooling pipe

Hybrid 6



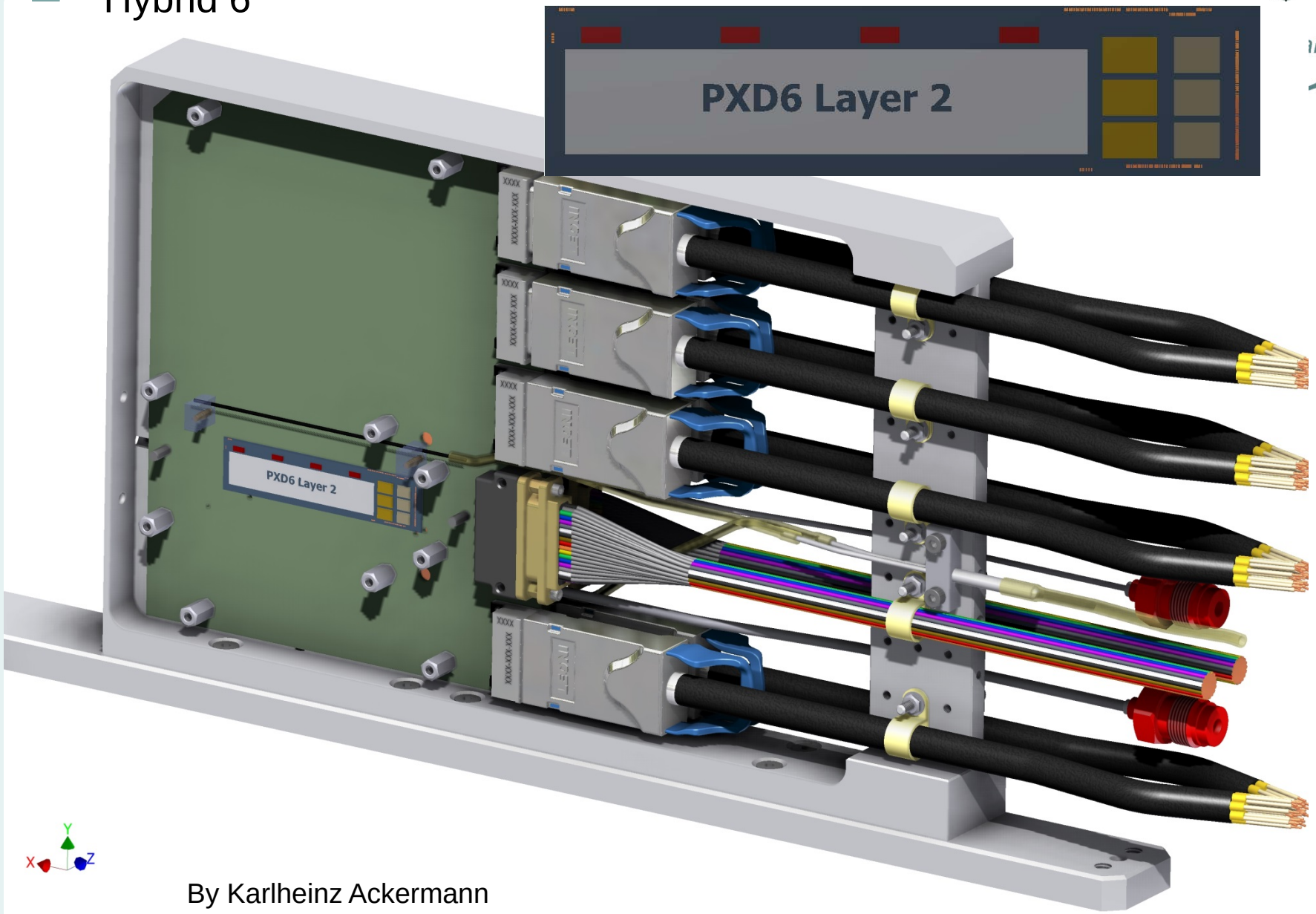
By Karlheinz Ackermann

Hybrid 6



By Karlheinz Ackermann

Hybrid 6



By Karlheinz Ackermann

Hybrid 6, design in progress

- 6 to 8 layers
- Place bottom traces to inner layer(s)
- Back drilling (more complex)

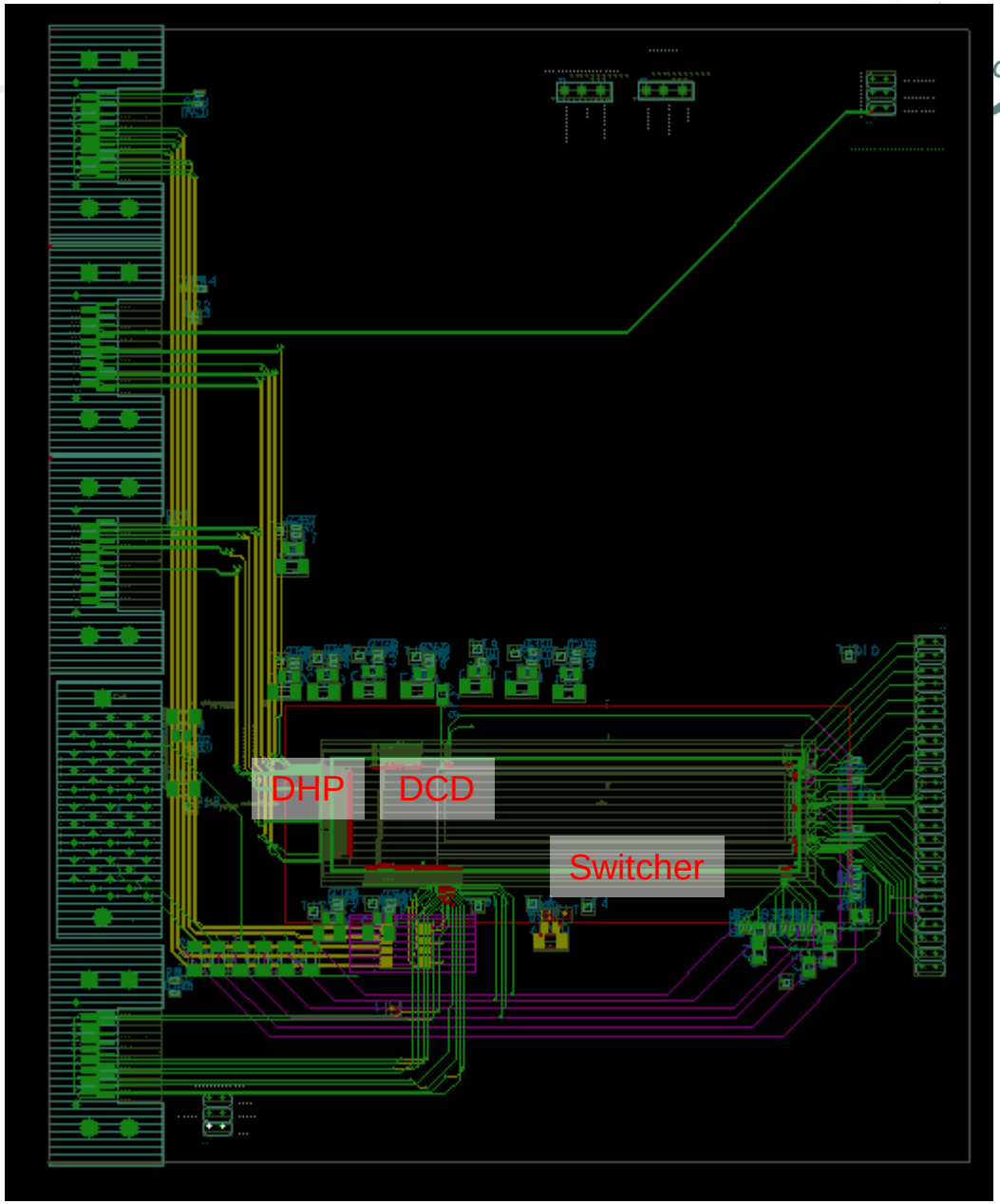
DHH <=> Switcher JTAG

DHH <=> DHP JTAG

DHH <=> DHP control lines

Power Connector

DHH <=> Switcher control lines



Conclusions and Outlook

- 2 long working PXD6 matrices waiting copper deposition
- Testing strategy planned
- PCB design of hybrid 6 in progress
- Open questions: Switcher control – Multiplexer in the case that DHPT is not ready

  => Must be tested on a extra board (needs a few weeks)

Thank you!

Pretests of large PXD6 matrices

- Keep all transistors OFF select only ONE gate (192x4 pixels) and measure I_d vs. V_{gs}
- Measure the characteristics of individual transistors along the ladder
- Check pedestal spread
- Check threshold voltage spread
- Check g_q spread

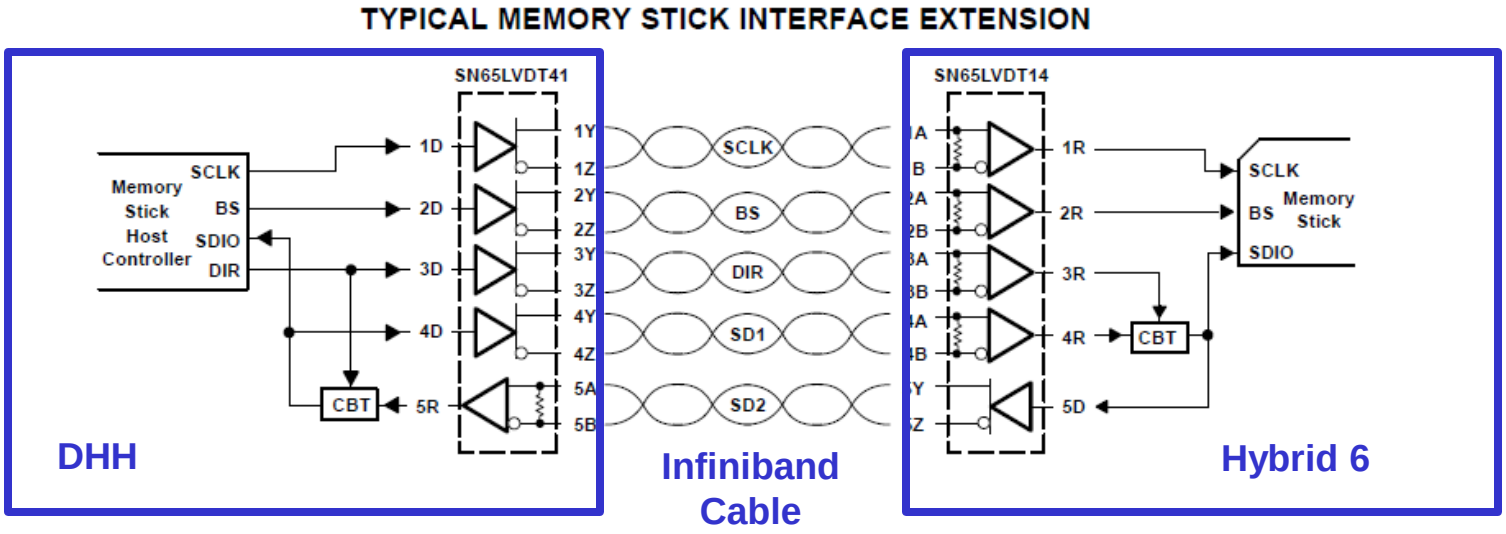
Hybrid 6 – JTAG (single ended & differential signals)

JTAG is provided by the DHH

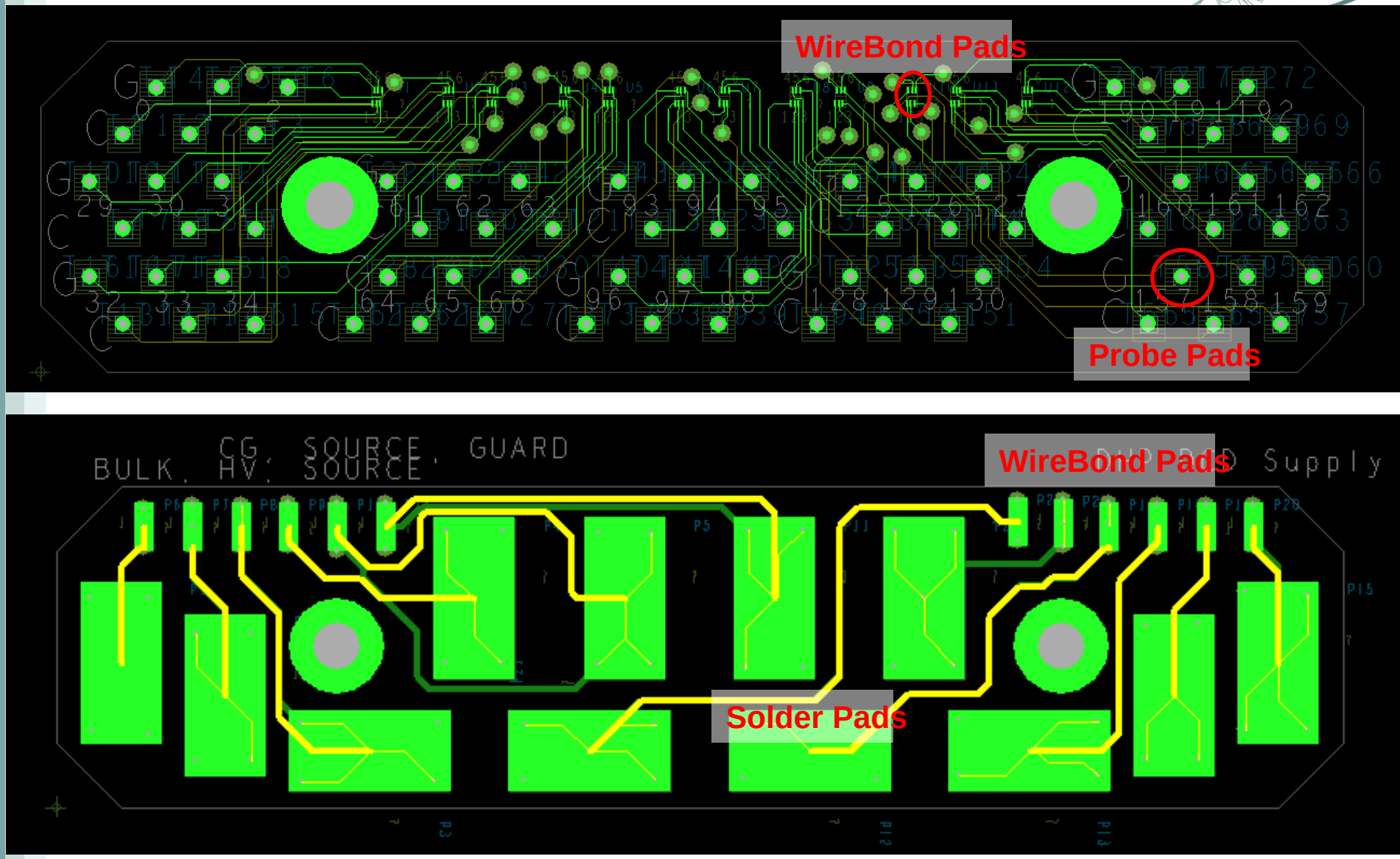
=> differential signals are favorized + converter (differential -> single ended)

=> SN65LVDT14 (in consultation with Igor Konorov)

VDD (3.3V) provided by LMU power supply (Polycover channel) (in consultation with Stefan Rummel)



Backup, EMCM


WireBond Pads
Probe Pads
BULK
CG
SOURCE
HV
SOURCE
GUARD
WireBond Pads
Solder Pads

Backup, EMCM