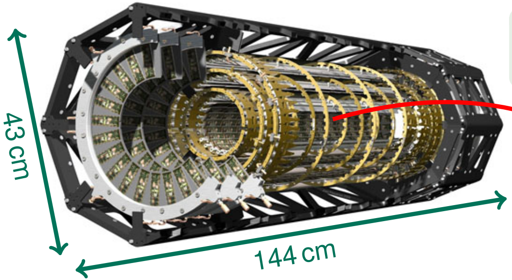
The upgrades of the ATLAS pixel detector

Stefano Terzo

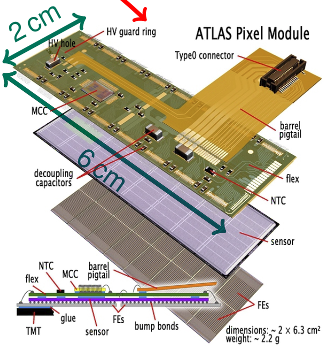
Max-Planck-Institut für Physik
München

Young Scientist Workshop
Ringberg Castle
17th July 2014

The original inner tracker of ATLAS



3 barrel layers
2×3 end cap disks

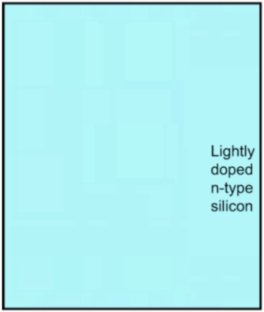


Composed of hybrid planar pixel detectors:

- 1744 modules
- 46080 pixel channels per module:
  - $50\,\mu\text{m} \times 400\,\mu\text{m}$ cell pitch
- n-in-n silicon sensors: 250μm thick

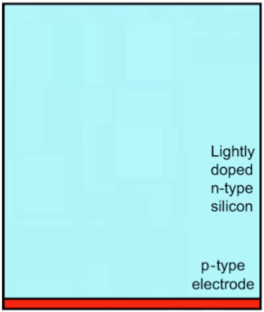
Hybrid silicon pixel detectors

- Lightly n-doped silicon:
  - n-doped ($-$ charge) pixels
  - p-doped ($+$ charge) backside
- A reverse bias voltage is applied:
  - silicon depletion from the backside (pn junction)
  - $\Delta V_{\text{bias}} > V_{\text{dep}} \rightarrow$ full depletion
  - depleted region = sensitive volume
- A particle passing through the depleted region creates electron-hole pairs which drift to the electrodes



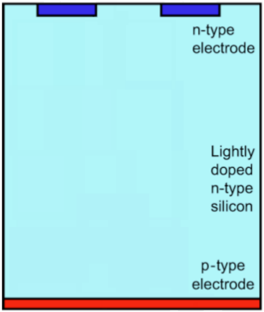
Hybrid silicon pixel detectors

- Lightly n-doped silicon:
  - n-doped (– charge) pixels
  - p-doped (+ charge) backside
- A reverse bias voltage is applied:
  - silicon depletion from the backside (pn junction)
  - $\Delta V_{\mathrm{bias}} > V_{\mathrm{dep}} \rightarrow$ full depletion
  - depleted region = sensitive volume
- A particle passing through the depleted region creates electron-hole pairs which drift to the electrodes



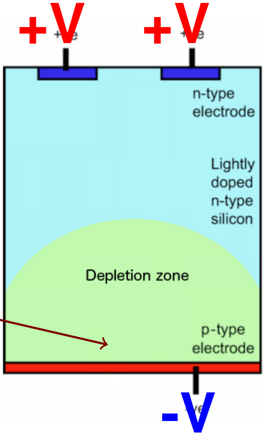
Hybrid silicon pixel detectors

- Lightly n-doped silicon:
  - n-doped ($-$ charge) pixels
  - p-doped ($+$ charge) backside
- A reverse bias voltage is applied:
  - silicon depletion from the backside (pn junction)
  - $\Delta V_{\mathrm{bias}} > V_{\mathrm{dep}} \rightarrow$ full depletion
  - depleted region = sensitive volume
- A particle passing through the depleted region creates electron-hole pairs which drift to the electrodes



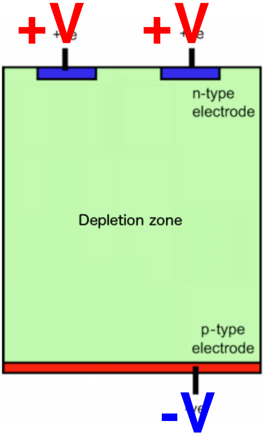
Hybrid silicon pixel detectors

- Lightly n-doped silicon:
    - n-doped (– charge) pixels
    - p-doped (+ charge) backside
- A reverse bias voltage is applied:
    - silicon depletion from the backside (pn junction)
    - $\Delta V_{\mathrm{bias}} > V_{\mathrm{dep}} \rightarrow$ full depletion
    - depleted region = sensitive volume
- A particle passing through the depleted region creates electron-hole pairs which drift to the electrodes



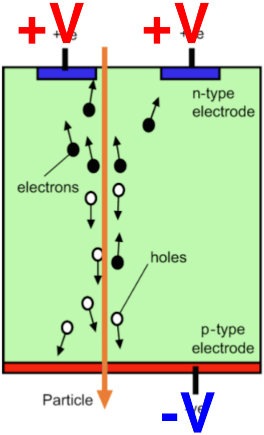
Hybrid silicon pixel detectors

- Lightly n-doped silicon:
  - n-doped ($-$ charge) pixels
  - p-doped ($+$ charge) backside
- A reverse bias voltage is applied:
  - silicon depletion from the backside (pn junction)
  - $\Delta V_{\mathrm{bias}} > V_{\mathrm{dep}} \rightarrow$ full depletion
  - depleted region = sensitive volume
- A particle passing through the depleted region creates electron-hole pairs which drift to the electrodes



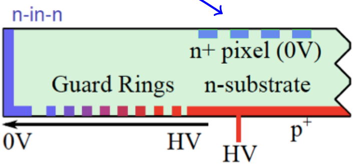
Hybrid silicon pixel detectors

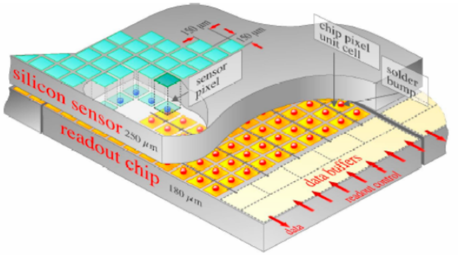
- Lightly n-doped silicon:
  - n-doped ($-$ charge) pixels
  - p-doped ($+$ charge) backside
- A reverse bias voltage is applied:
  - silicon depletion from the backside (pn junction)
  - $\Delta V_{\text{bias}} > V_{\text{dep}} \rightarrow$ full depletion
  - depleted region = sensitive volume
- A particle passing through the depleted region creates electron-hole pairs which drift to the electrodes

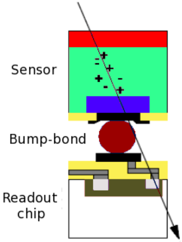


Hybrid silicon pixel detectors

- Pixel surface segmentation:
  - precise two dimensional spatial information
- Guard ring structures to smoothly drop the potential at the edge of the sensor
- Readout chip coupling (bump bonding)

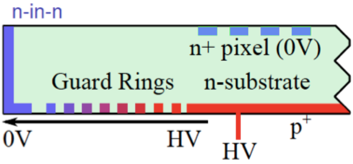


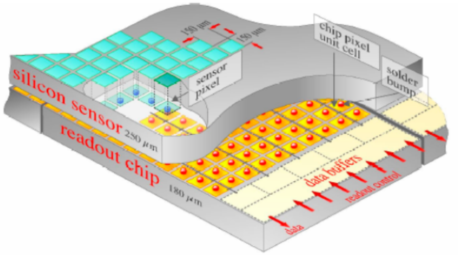


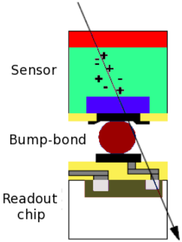


Hybrid silicon pixel detectors

- Pixel surface segmentation:
  - precise two dimensional spatial information
- Guard ring structures to smoothly drop the potential at the edge of the sensor
- Readout chip coupling (bump bonding)

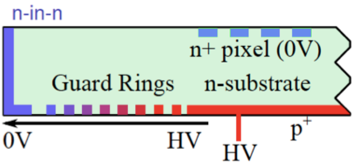


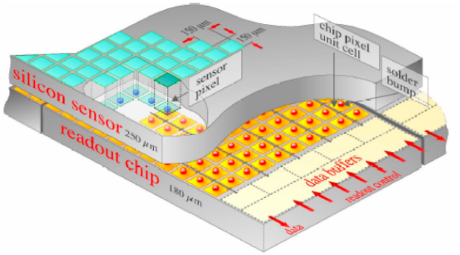


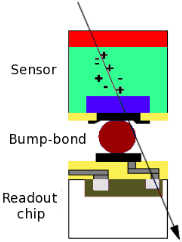


Hybrid silicon pixel detectors

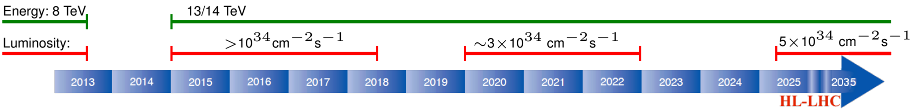
- Pixel surface segmentation:
  - precise two dimensional spatial information
- Guard ring structures to smoothly drop the potential at the edge of the sensor
- Readout chip coupling (bump bonding)







The inner tracker upgrade plan



Energy: 8 TeV

13/14 TeV

Luminosity:

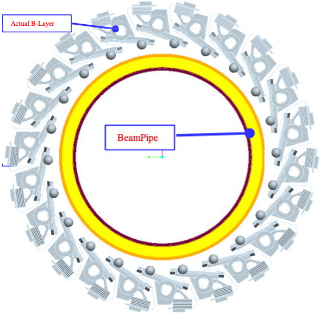
$>10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$

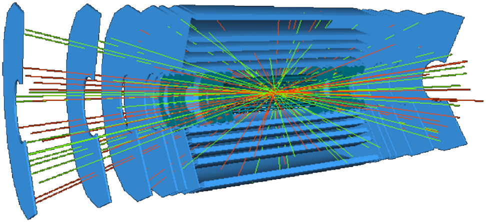
$\sim 3\times10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$

$5\times10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$

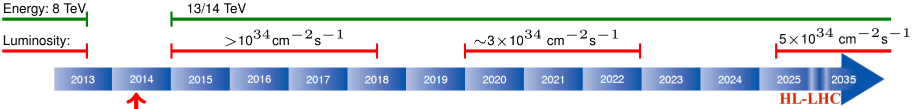
2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2035

HL-LHC





The inner tracker upgrade plan



Energy: 8 TeV

13/14 TeV

Luminosity:

$>10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$

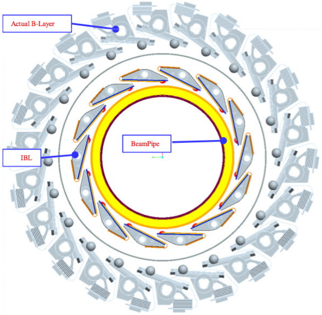
$\sim 3\times10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$

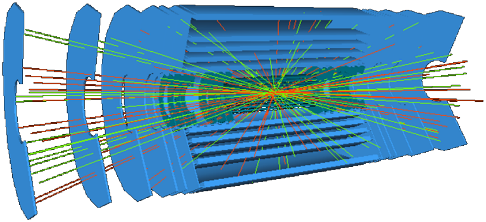
$5\times10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$

2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2035

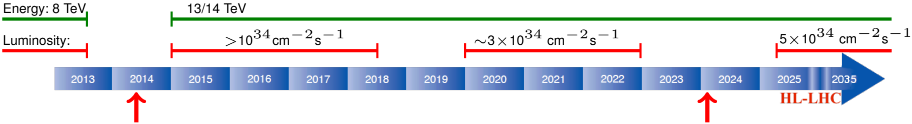
HL-LHC

Insertable B-Layer (IBL): new pixel layer at 3.2 cm from the pp interaction





The inner tracker upgrade plan



Energy: 8 TeV

13/14 TeV

Luminosity:

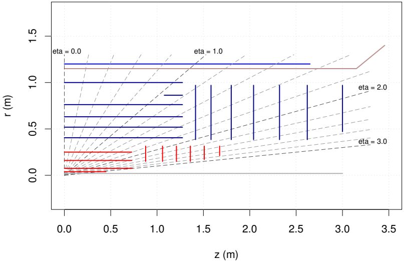
$>10^{34}$ cm^{-2}s^{-1}

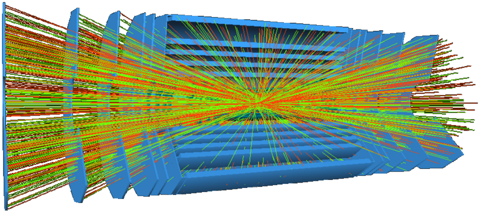
$\sim 3\times10^{34}$ cm^{-2}s^{-1}

5×10^{34} cm^{-2}s^{-1}

Insertable B-Layer (IBL): new pixel layer at 3.2 cm from the pp interaction

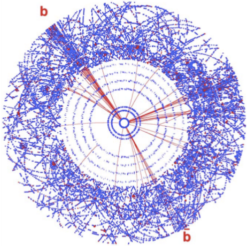
"Phase II": full inner detector replacement (4 layers)

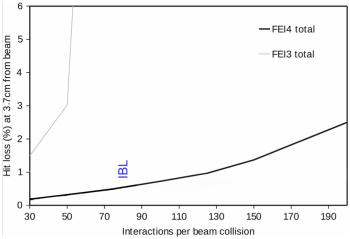




Why a fourth layer?

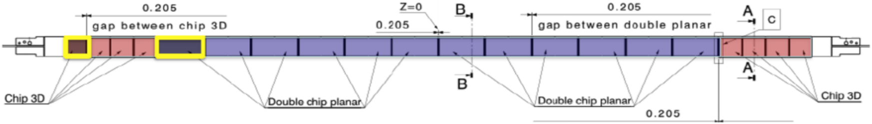
- Mantain and improve performances lost due to current detector degradation:
  - radiation damage
  - module failure
- Improve tracking, vertexing and b-tagging:
  - proximity to the interaction point
  - larger extension along the beam line
  - improve track measurement
- Cope with pile-up at high luminosity
  - The new IBL will be tolerant to higher occupancy without saturation



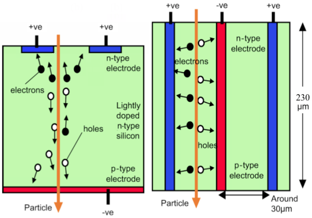


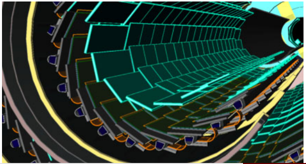
The Insertable B-Layer (IBL)

14 support structures (staves) to hold 32 new front-end chips each



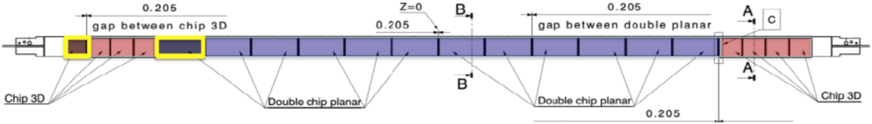
- Mixed sensor technology:
  - 200 μm thick planar n-in-n silicon sensors
  - 230 μm thick 3D n-in-p silicon sensors
- Full ϕ coverage by tilting staves by 14°
  - Overlap of the inactive regions
- Coverage in $|\eta| < 2.8$
- No overlap possible due to limited space
  - Recover z coverage with slim edge sensors



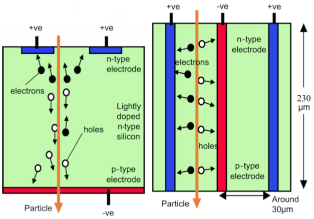


The Insertable B-Layer (IBL)

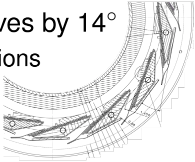
14 support structures (staves) to hold 32 new front-end chips each



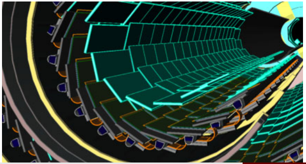
- Mixed sensor technology:
  - 200 μm thick planar n-in-n silicon sensors
  - 230 μm thick 3D n-in-p silicon sensors



- Full ϕ coverage by tilting staves by 14°
  - Overlap of the inactive regions

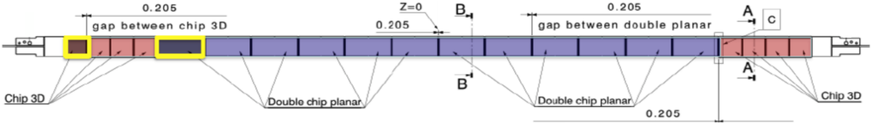


- Coverage in $|\eta| < 2.8$
- No overlap possible due to limited space
  - Recover z coverage with slim edge sensors

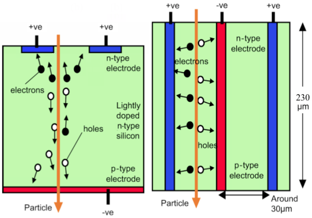


The Insertable B-Layer (IBL)

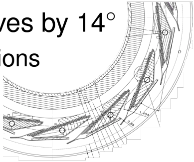
14 support structures (staves) to hold 32 new front-end chips each



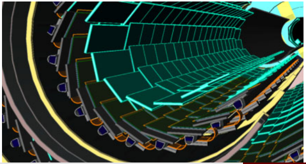
- Mixed sensor technology:
  - 200 μm thick planar n-in-n silicon sensors
  - 230 μm thick 3D n-in-p silicon sensors



- Full ϕ coverage by tilting staves by 14°
  - Overlap of the inactive regions

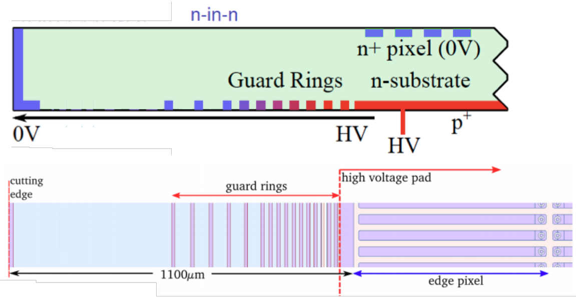


- Coverage in $|\eta| < 2.8$
- No overlap possible due to limited space
  - Recover z coverage with slim edge sensors



Slim edge planar pixel sensors for IBL

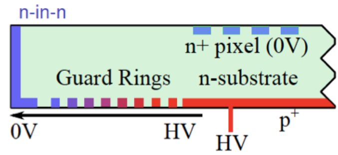
No overlap possible along the beam direction for the inner layer
→ new slim edge design



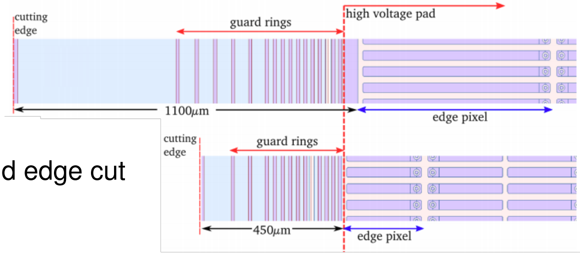
- Initial design
    - 1.1 mm dead area
- Reduced guard rings and edge cut
    - 450 μm dead area
- Pixels shifted behind the guard rings
    - Dead area is reduced to 200 μm

Slim edge planar pixel sensors for IBL

No overlap possible
along the beam direction
for the inner layer
→ new slim edge design

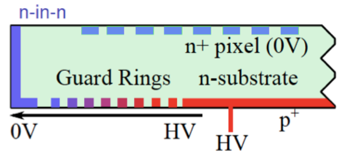


- Initial design
  - 1.1 mm dead area
- Reduced guard rings and edge cut
  - 450 μm dead area
- Pixels shifted behind the guard rings
  - Dead area is reduced to 200 μm

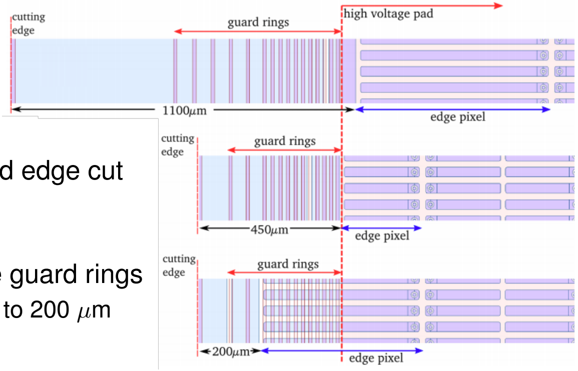


Slim edge planar pixel sensors for IBL

No overlap possible along the beam direction for the inner layer → new slim edge design

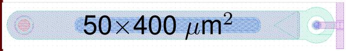


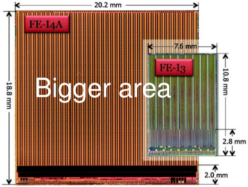
- Initial design
  - 1.1 mm dead area
- Reduced guard rings and edge cut
  - 450 μm dead area
- Pixels shifted behind the guard rings
  - Dead area is reduced to 200 μm

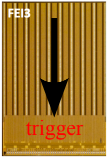


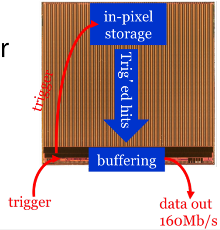
The new readout chip

FE-I3	vs	FE-I4
$50\times400\ \mu m^2$	Smaller pixel pitch	$50\times250\ \mu m^2$
1×1 cm^2	Bigger area	2×2 cm^2
160 row × 18 columns		336 row × 80 columns
$1\times10^{15}\mathrm{n_{eq}/cm^2}$	Radiation hardness	$5\times10^{15}\mathrm{n_{eq}/cm^2}$
column drain architecture	higher hit rate	local in pixel storage





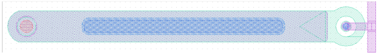




From IBL to the inner layers of Phase II

A smaller pixel cell to reduce the occupancy

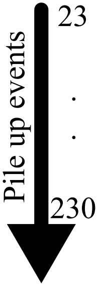
Now: FE-I3 chip $50\times400\ \mu\mathrm{m}^2$

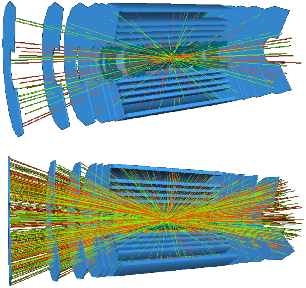


IBL: FE-I4 chip $50\times250\ \mu\mathrm{m}^2$

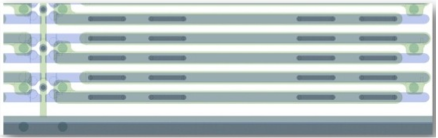
Ph. II: new chip $25\times100\ \mu\mathrm{m}^2$

or $50\times50\ \mu\mathrm{m}^2$



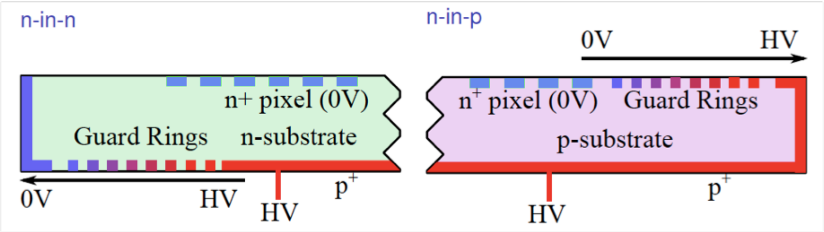


preliminary studies using the FE-I4 chip and $25\times500\ \mu\mathrm{m}^2$ pixel shape



From “n-in-n” to “n-in-p” sensors

Present pixel detector + IBL → Phase II (HL-LHC)



N-in-n

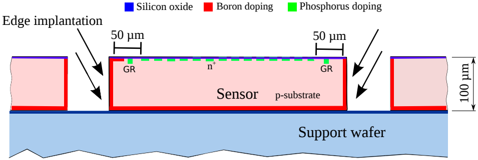
- Depletion from the backside
- Guard rings on the backside
- Double sided process
  - → Pixel can be shifted below the guard rings

N-in-p

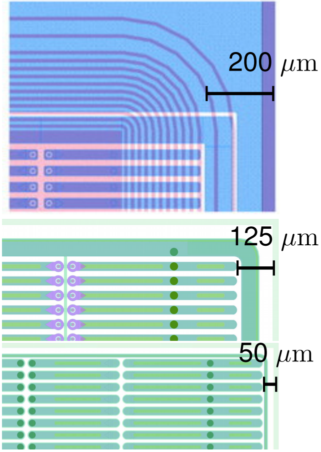
- Depletion from the pixel side
- Guard rings on the pixel side
- Single sided process
  - → Cost effective to cover large areas

A new solution is necessary to reduce the dead area

Planar active edge sensors for HL-LHC



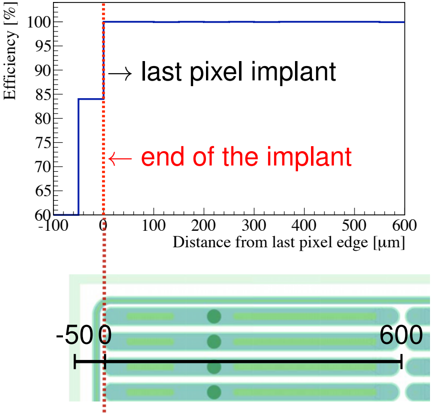
Backside implantation extended to the edges



- Present IBL design:
  - n-in-n sensor with 200 μm edge (pixel shifted under the guard rings)
- Phase II alternatives:
  - n-in-p sensor with 125 μm active edge (only one Bias Ring)
  - n-in-p sensor with 50 μm active edge (Floating Guard Ring)

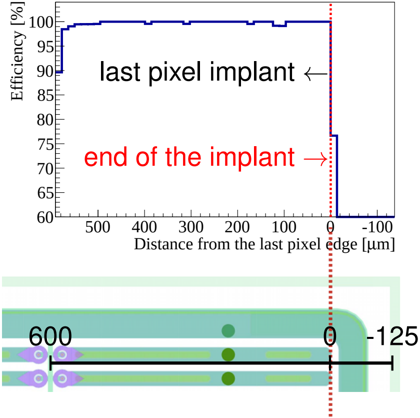
Edge efficiency

FE-I3, 50 μm active edge



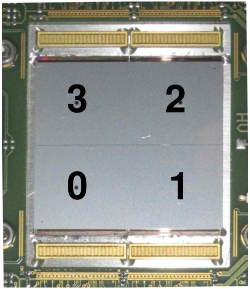
Active area extends outside the last pixel implant up to the active edge

FE-I3, 125 μm slim edge



Active area only until the bias ring structure

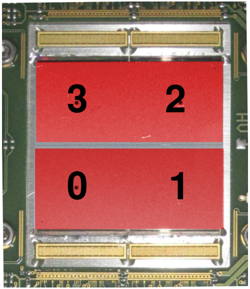
N-in-p quad modules for the outer layers



Quad module:
4 × readout chips connected to a bigger sensors

- Planned full module geometry for phase II
  - No guard ring structures between the 4 chips
  - Fully active area between the 4 chips

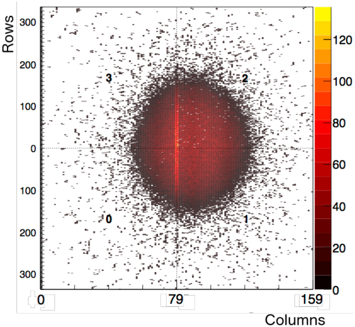
N-in-p quad modules for the outer layers



Quad module:
4× readout chips connected to a bigger sensors

- Planned full module geometry for phase II
  - No guard ring structures between the 4 chips
  - Fully active area between the 4 chips

First tests performed on pseudo quad module interconnected to IBL FE-I4 chips



Summary and outlook

- IBL, the 4th pixel layer in ATLAS has been successfully inserted:
    - closer to the interaction point
    - featuring the new FE-I4 chip
    - improved radiation hardness
- New module designs are necessary to cope with the HL-LHC environment:
    - reduced occupancy
    - radiation hardness
    - increased active area (for the innermost layers)
- N-in-p active/slim edge sensor are under investigation for the HL-LHC upgrade:
    - 50 $\mu\mathrm{m}$ active edge sensors show efficiency even outside the pixel area
- First pseudo quad modules have been assembled and characterized