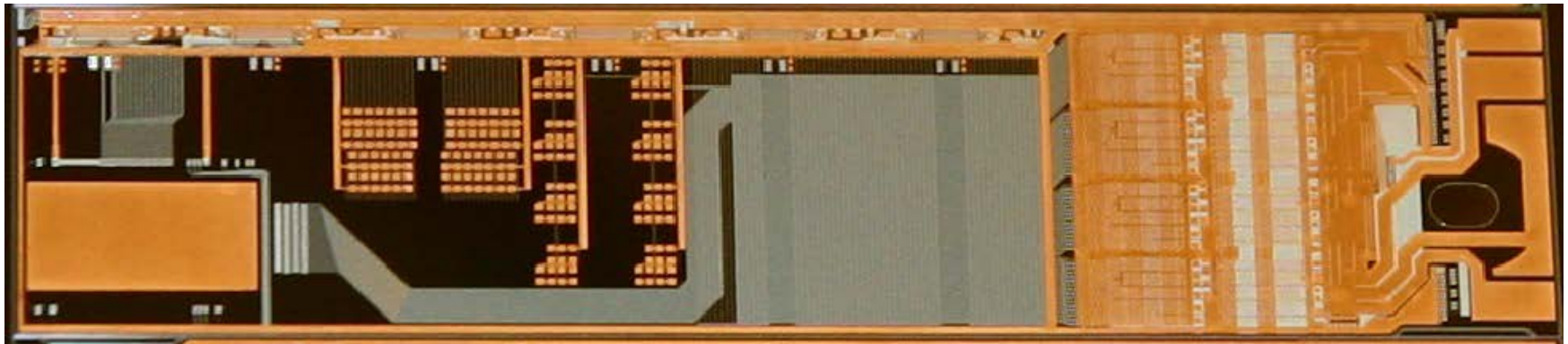


# EMCM testing summary

C. Koffmane, P. Avella, J. Ninkovic

# Electrical Multi-Chip Module

- 3 metal layers on silicon substrate
- 4055 test pads (size down to  $70\mu\text{m} \times 70\mu\text{m}$  and  $50\mu\text{m} \times 100\mu\text{m}$ )
- 2149 different electrical nets
- Open and short test necessary



- Adjacency test contains  $>100\text{k}$  test per EMCM
- With up to  $2\text{k}$  test for individual pads

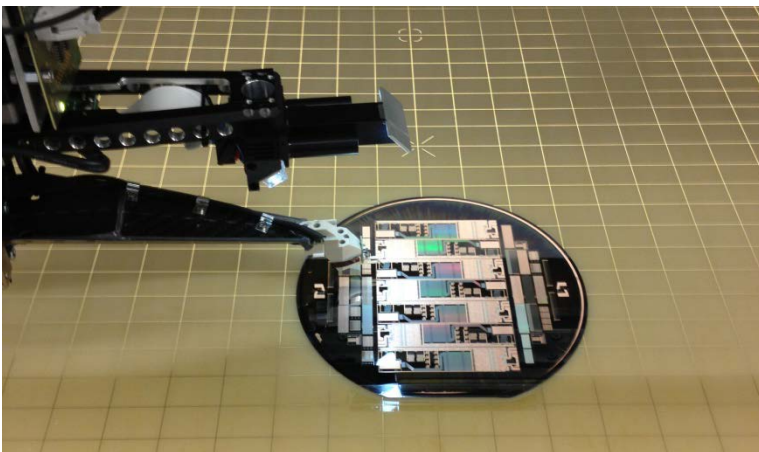
# Test ZMI 5

- Wafers from Test ZMI5 – produced to optimize metal systems
- P1, P2, P3, P4, P5, P6
- P5 had problems in 2 metal layer system
- Other wafers had different variations but showed good performance in tests performed before Cu but EOS was not tested
- Change in the Cu layout to accommodate bigger caps required change in the test program

# ATG testing



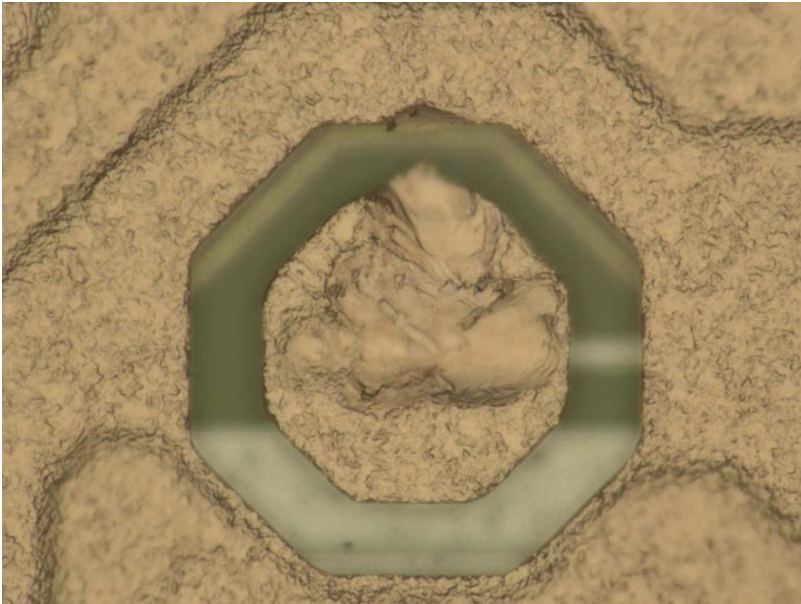
- A7 machine
- 4 flying needles
- Placed in not temperature controlled room and not in the clean room conditions.
- This brought some initial problems with alignment and some “not real” shorts due to the dirt falling on the wafers



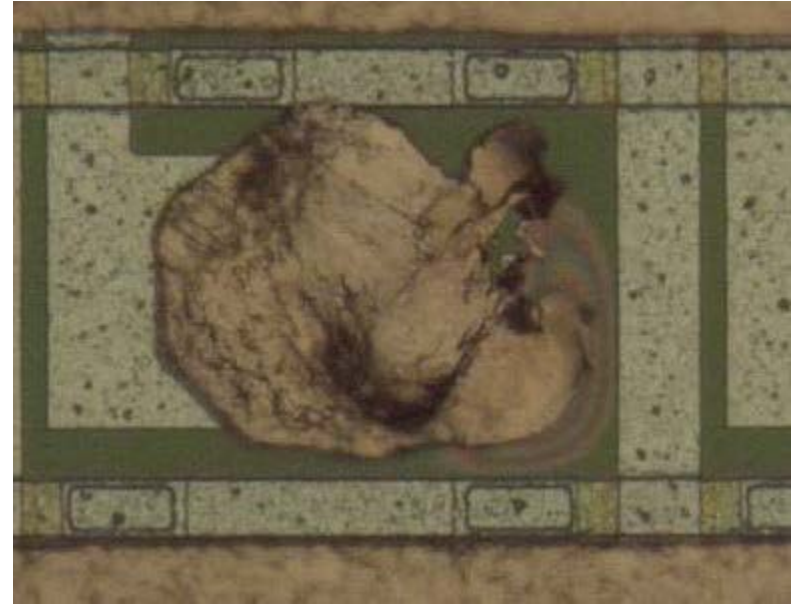
Measurements done by:  
Christian K. (week 19 &20)  
Paola A. (week 20)

# ATG testing - Wafers A1(dummy), P1

- Problems with alignment accuracy in time (week19)



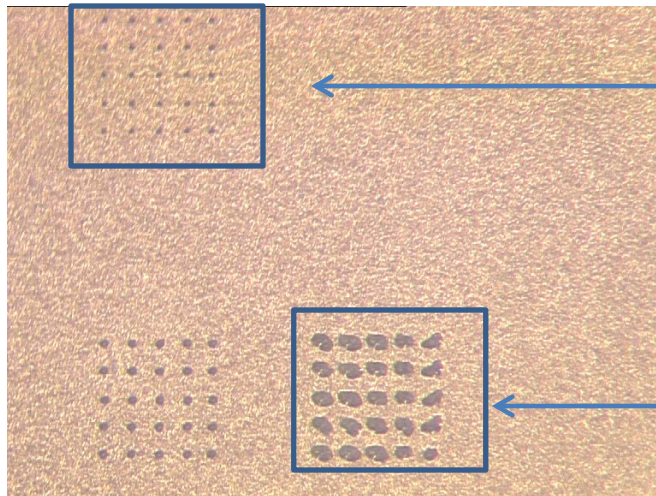
A7 machine has non optimal accuracy  
Drifts due to the temperature changes



Non optimal stopping speed of the  
probe heads

# ATG testing – Wafers P2, P4, P6

- Optimized speed of the probe heads (week20)
- Calibration of the A7 before each run
- Best results in terms of accuracy of the needle position during the night run (wafer P4)



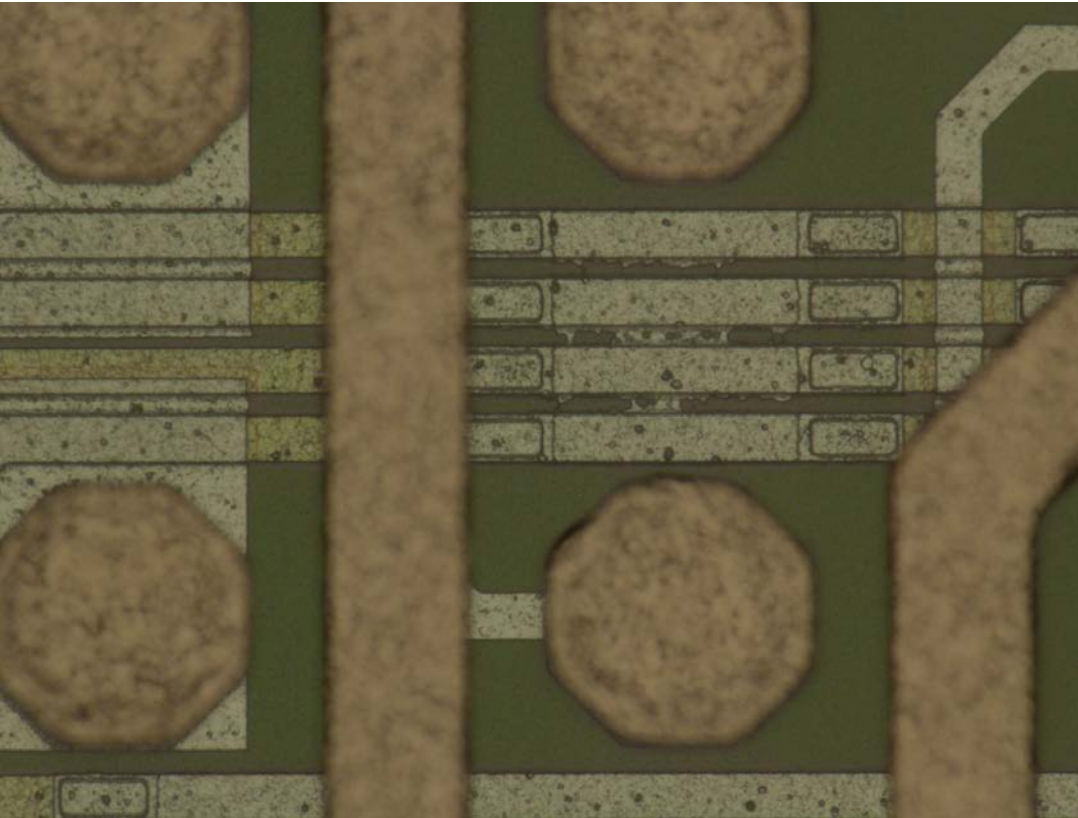
100 x touch down with optimized settings  
(week 20)  
(stroke, pressure and accuracy set to 5)

100 x touch down with non-optimized settings  
from the first week (week19)

# ATG results – P1

- Showed :
  - order of 20 low ohmic shorts on a DUT1 ( $<20 \Omega$ )
  - order of 600 high ohmic shorts on a DUT 1 (few  $M\Omega$ )

# Low ohmic shorts

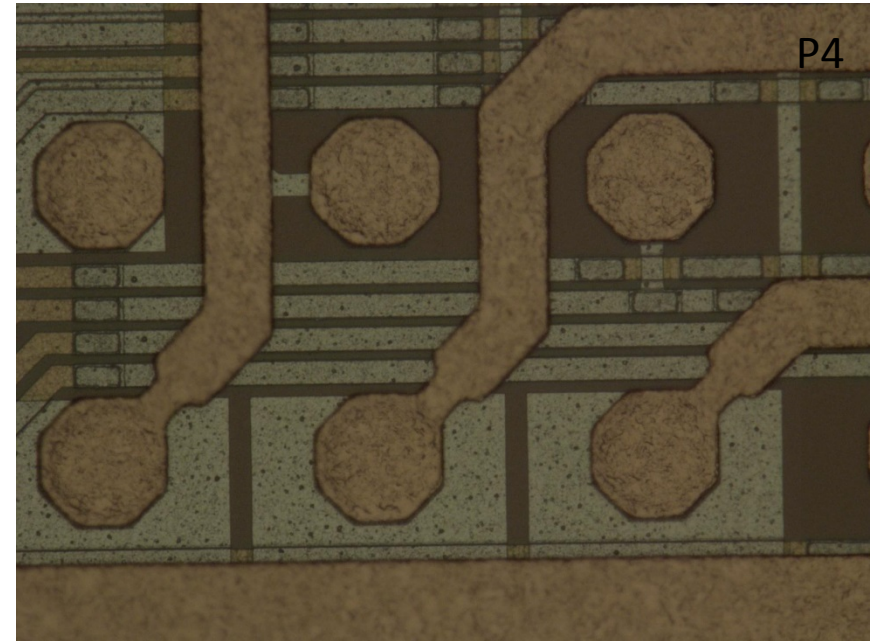
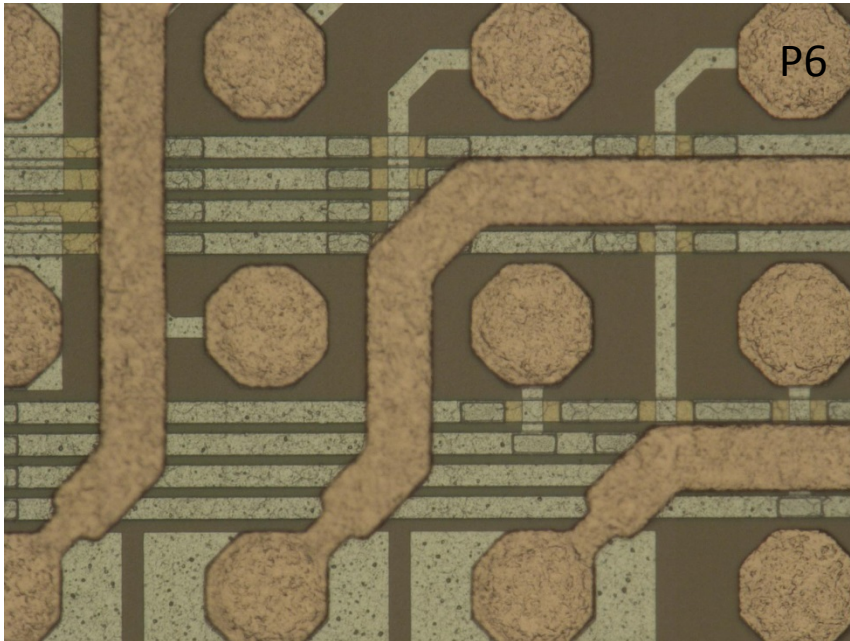


Stack of Al1 +Al2 used to decrease resistance of the control lines of switchers had problems in production  
Differs from wafer to wafer



# Low ohmic shorts – Wafers P4 & P6

- Optical inspection done on all wafers - this problem could not be identified of wafers P4 and P6 - still significant area under Cu



## EMCM (ZMI-5) WaferP6

DUT 1: 1 low ohmic short (??)

DUT 2: no low ohmic shorts

DUT 1 open: 2 x DCD to DHP interconnection in 2<sup>nd</sup> and 4<sup>th</sup>  
pair

DUT 2 open: 1 connection to test switcher pad (2<sup>nd</sup> SW)  
1 drain pad to DCD input

# EMCM (ZMI-5) WaferP6

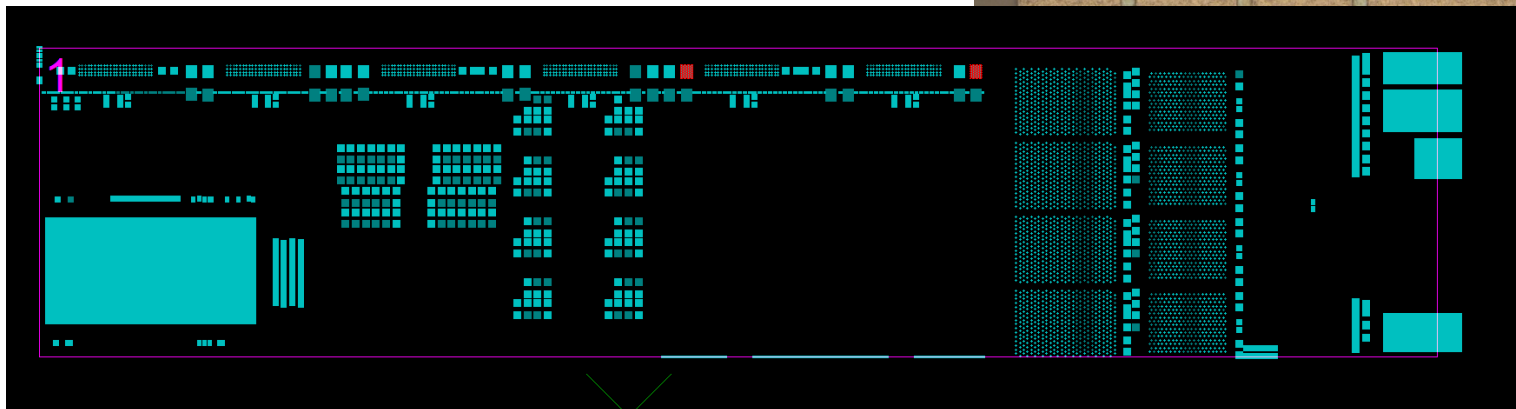
**DUT1 – short GATE ON –GATE OFF**

Nets 1721,1749



Particle or below Cu?

Short measured on pads 3762-3846



# EMCM (ZMI-5) WaferP4

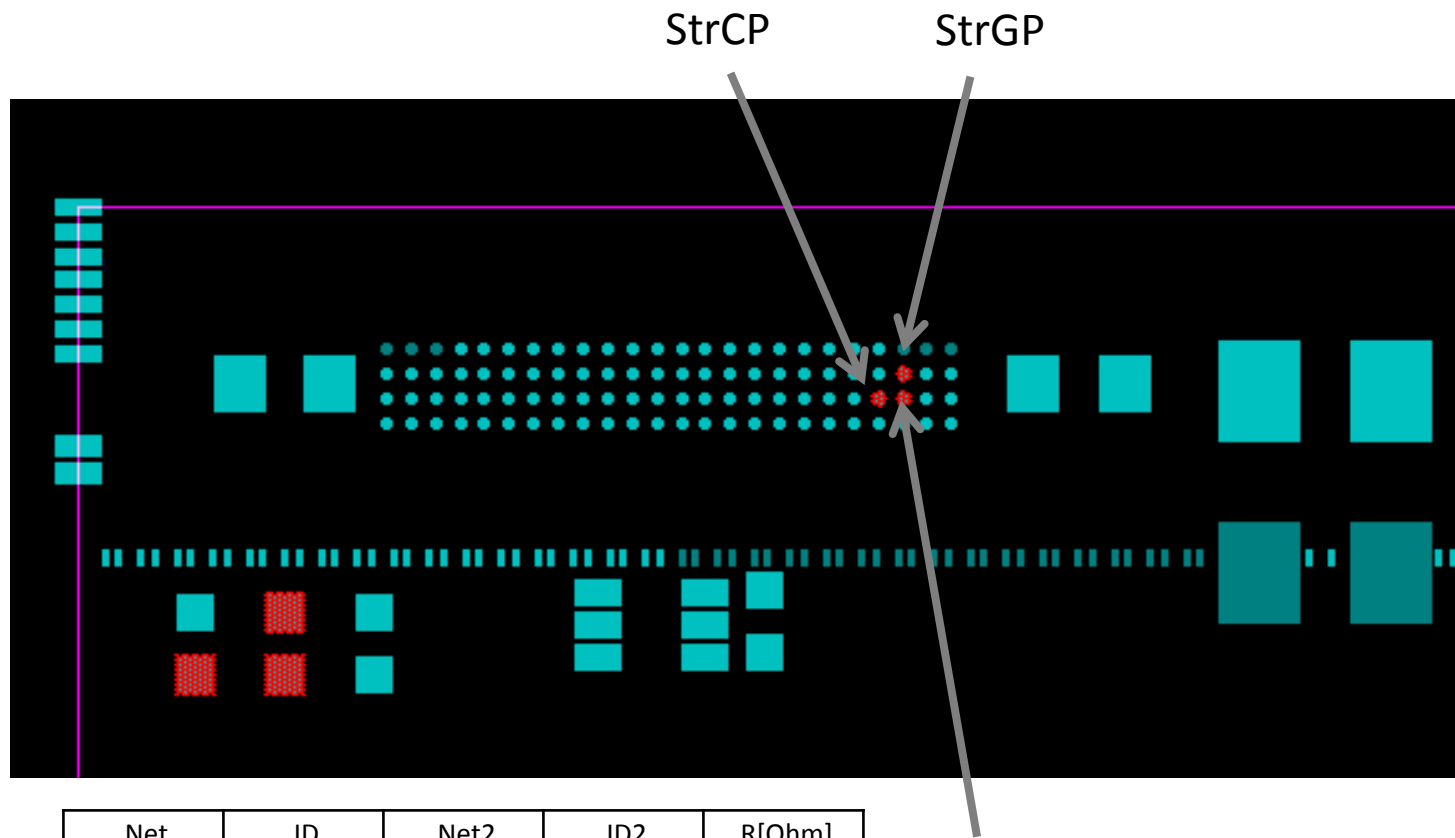
**DUT1 – 400k $\Omega$  shorts - to be remeasured ... on wafer P1 such measurement results were caused by dirt**

**(DHP\_CORE -DCD AmpLow) – should be functional even with this short**

**and in addition several hundred Mohm shorts,  
no open**

# EMCM (ZMI-5) WaferP4

## DUT2 – low ohmic shorts



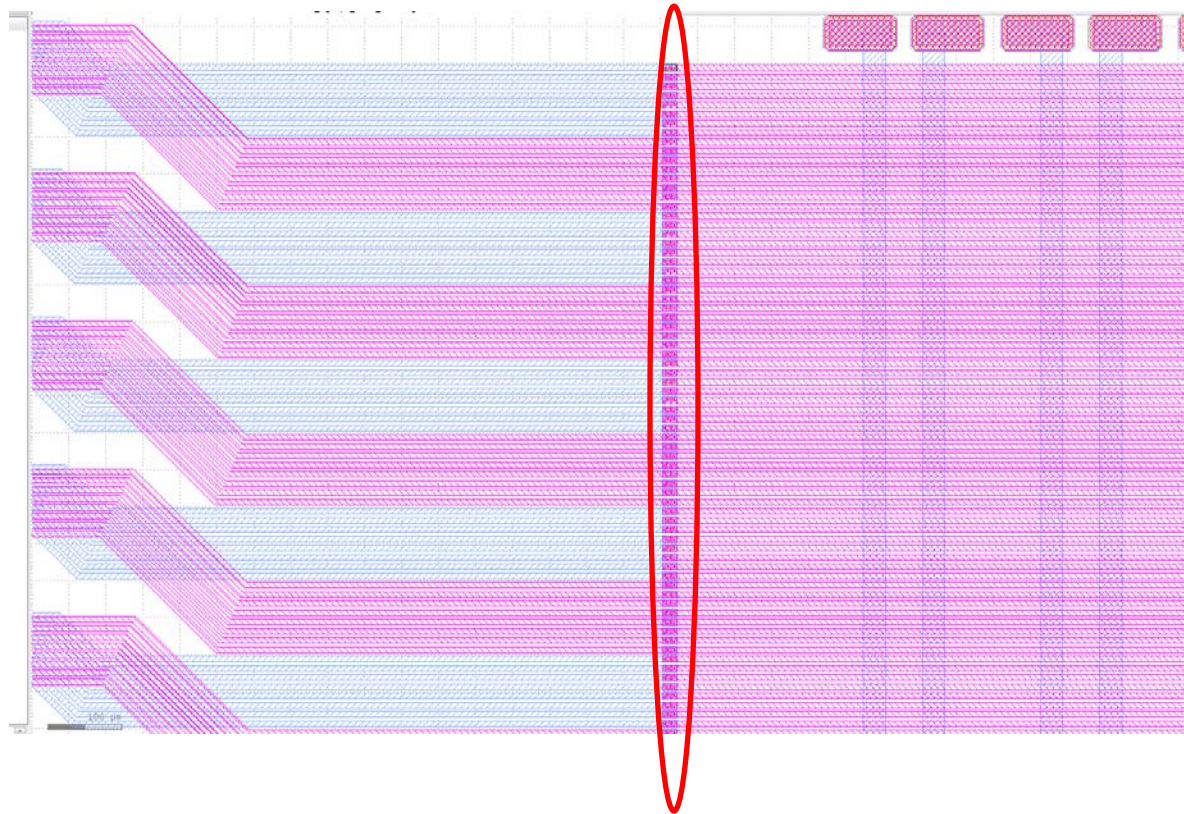
Net	ID	Net2	ID2	R[Ohm]
1731	3786	1780	3928	31.07
1731	3786	1780	3928	36.18
1732	3793	1780	3928	75.53
1732	3793	1731	3786	80.36
1731	3786	1732	3793	81.49

And in addition several hundred Mohm shorts

# High Ohmic shorts

- Present on all tested wafers
- Test ZMI5 project had additional Polysilicon layer and Contact 1 mask to increase topology
- Reason for high ohmic shorts understood.
- During the conversion process to produce mask for photolithography some of the contact 2 openings were transferred into contact1 mask – not really understood how this happened
- Result – all drain lines are connected once to the bulk

# Position of problematic contacts to the bulk



Due to the fact that high ohmic material was used one can use those EMCM (in dark dynamic resistance of about  $20\text{G}\Omega$  measured )

# New EMCMs

- As soon as we got the results we have initiated new fast production run
- Wafers with 7 EMCs/wafers are being processed
- All problems realized up to know fixed
- Structuring of the first Al layers is being done at the moment
- Time estimate 6 more weeks till new EMCs are processed
- ATG is preparing better S machine for the next round of testing - will be ready within the next 3-4 weeks



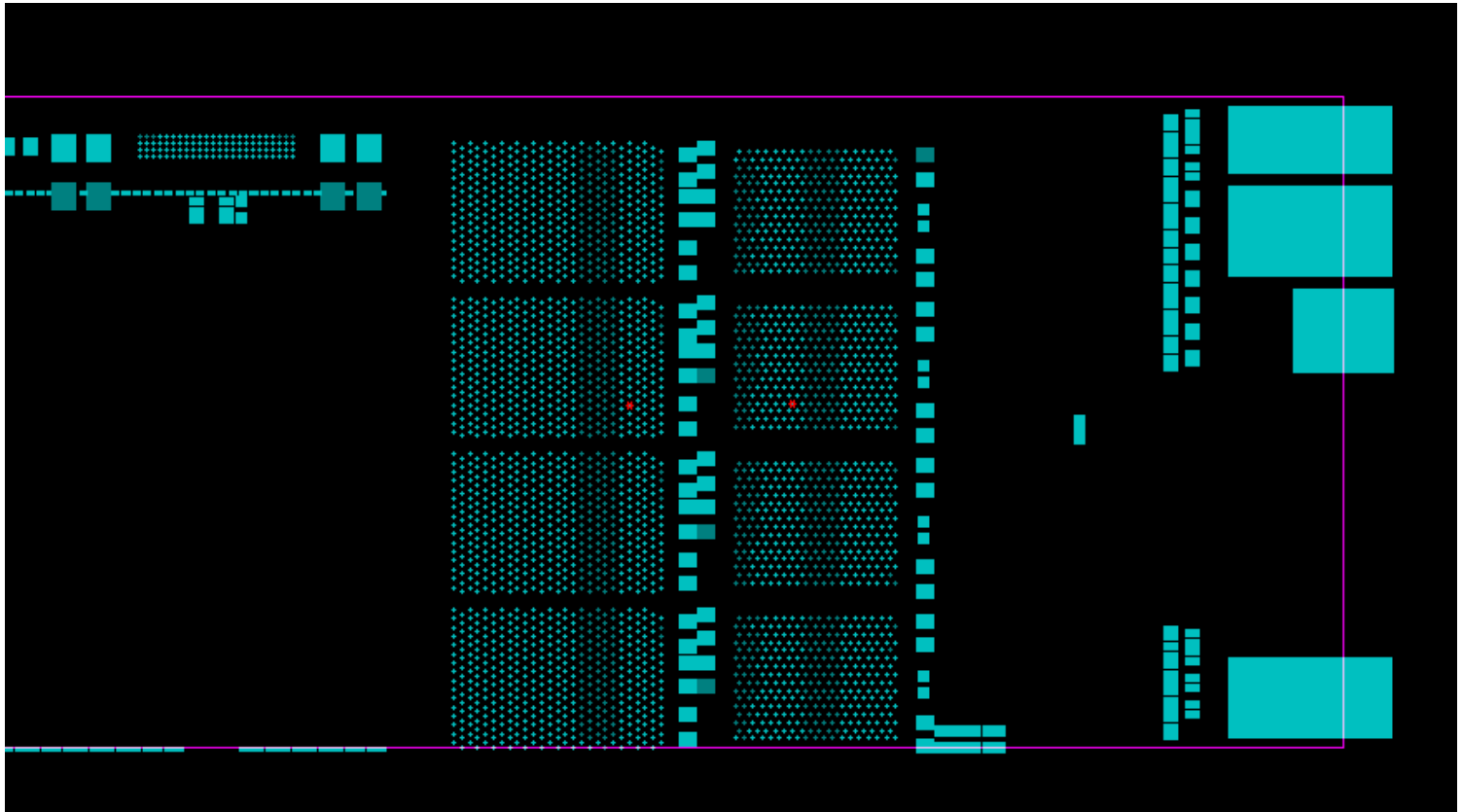
# EMCM testing summary

- We have 3 EMCM that we could use for further assembly.
- Wafers are getting solder stop at the moment and will be cut soon.
- New production run with 7 EMCM/wafer have been started / should be finished in about 6 weeks → Highest priority project!!
- ATG is preparing better machine S machine for the next test

- Backup slides follow ...

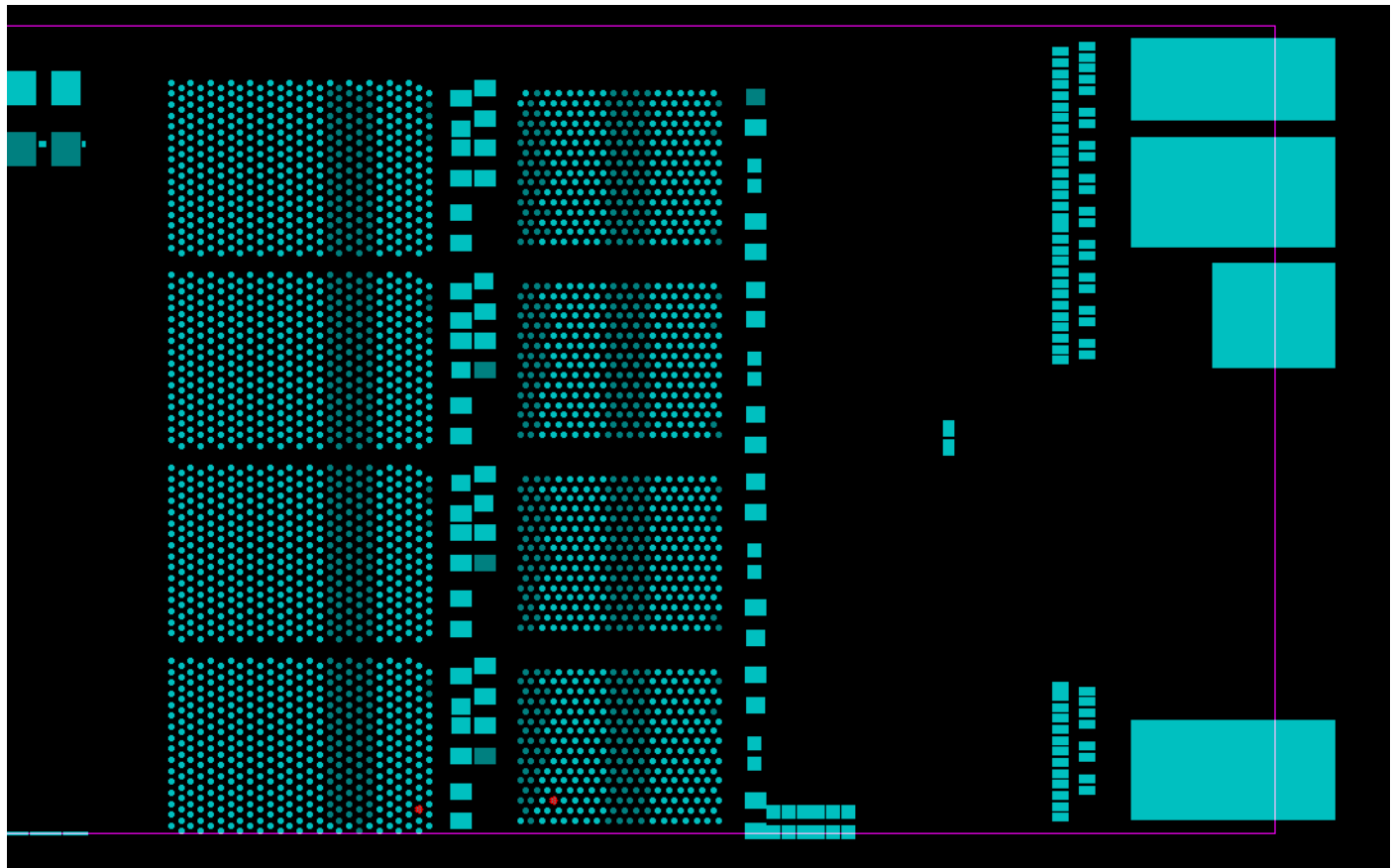
**DUT2 – open**

Pad 3033 - 3032



**DUT2 – open**

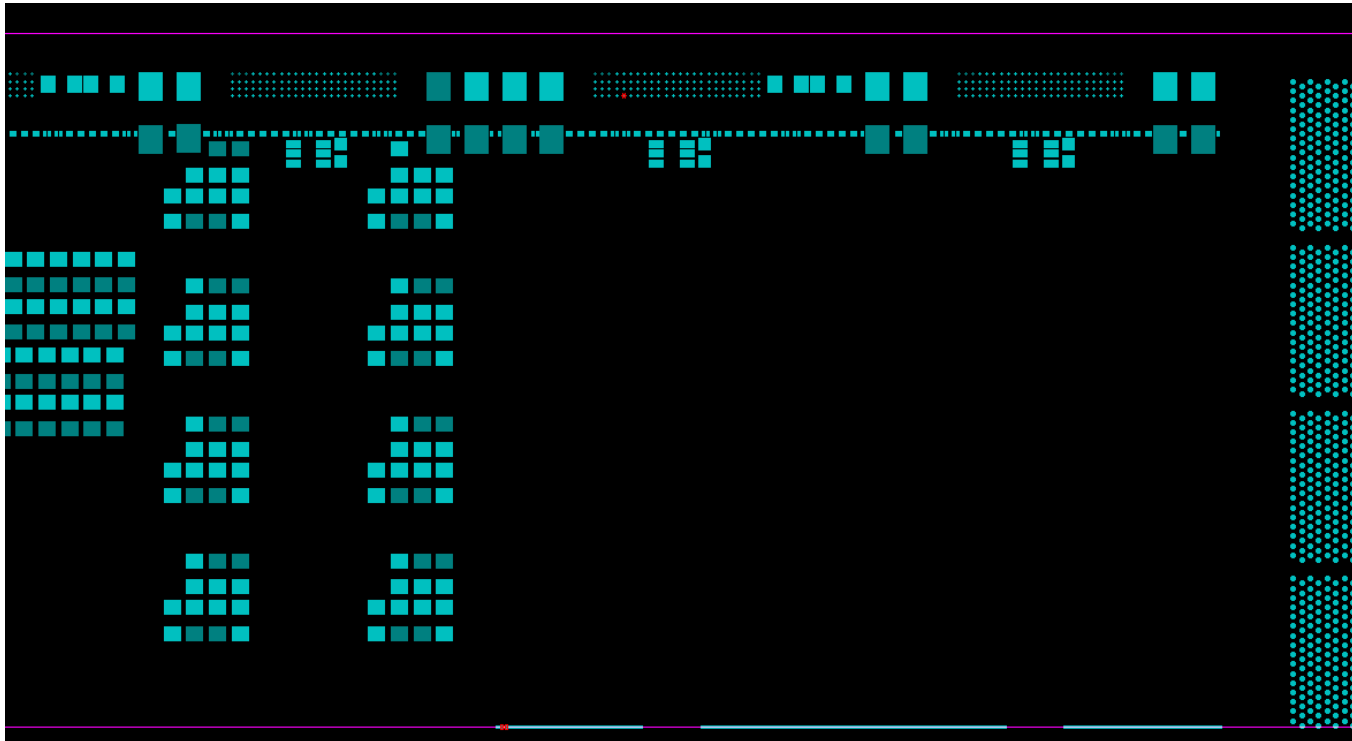
Pad 1290 - 1289



# EMCM (ZMI-5) WaferP6

## DUT1 – open

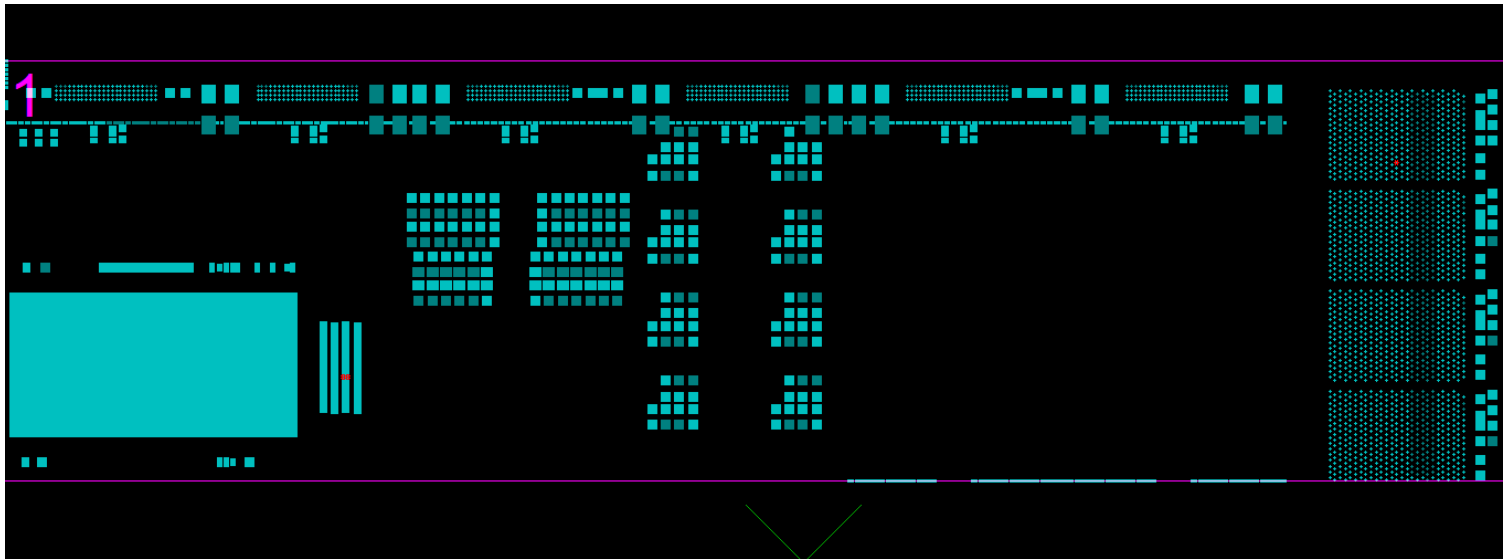
Pad 293 - 294



# EMCM (ZMI-5) WaferP6

## DUT1 – open

Pad 2126 - 2127



# EMCM (ZMI-5) WaferP4

DUT2 – open

SwitcherB Output

