Report of the Electronics Division

Project Review 2014

$$\Delta p \cdot \Delta q \geqslant \tfrac{1}{2}\hbar$$

Max-Planck-Institut für Physik
(Werner-Heisenberg-Institut)

Outline

- Projects in 2014

- Manpower
  - Distribution in 2014

  - Requests for 2015/16

- Status of some selected projects

- Additional activities

Projects in 2014

- Main Projects
  - ATLAS HEC front-end development

  - ATLAS HEC low voltage

  - ATLAS MDT electronics upgrade for HL-LHC

  - ATLAS MDT small tubes and chambers

  - Belle-II

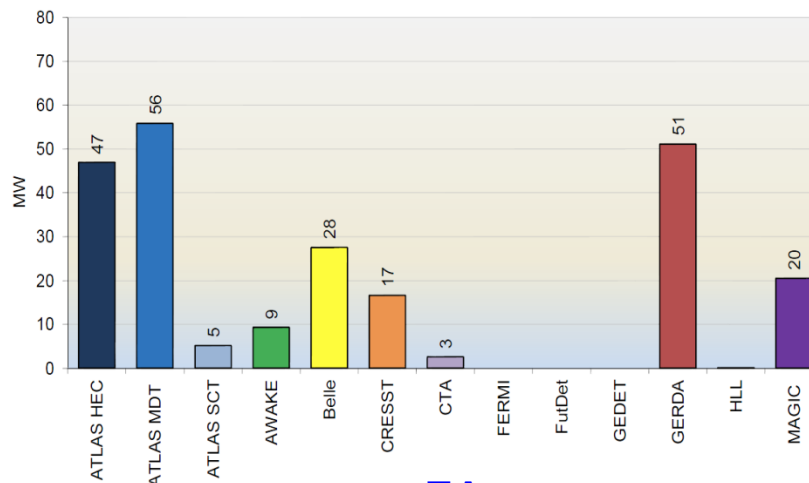 - MAGIC

  - GERDA

  - CRESST
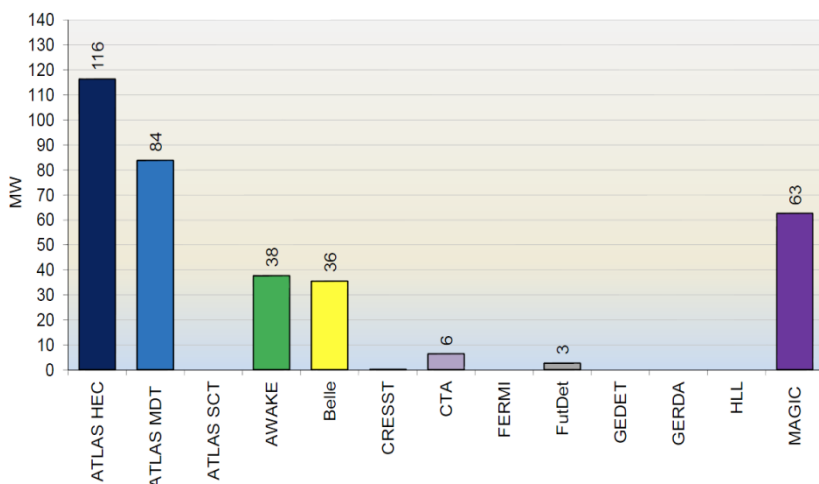
Groups
EA: Elektronik Anlagen
EE: Elektronik Entwicklung
EP: Elektronik Produktion

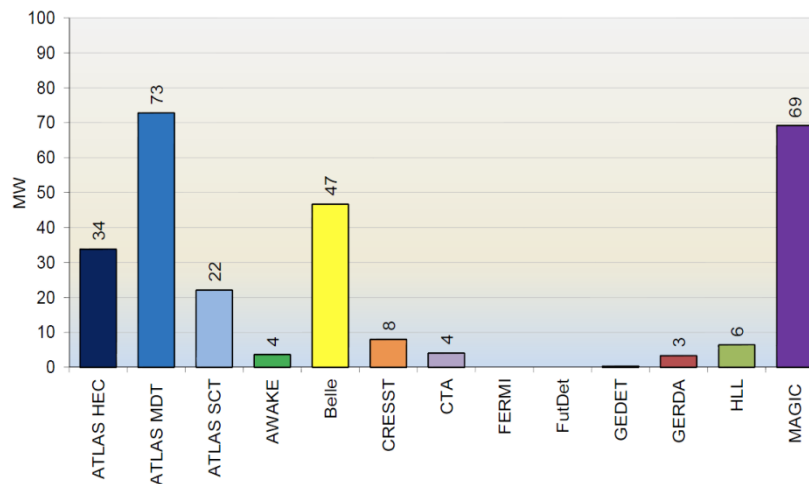# Labor of Individual Groups in 2014

- January – November in MW (man-week)

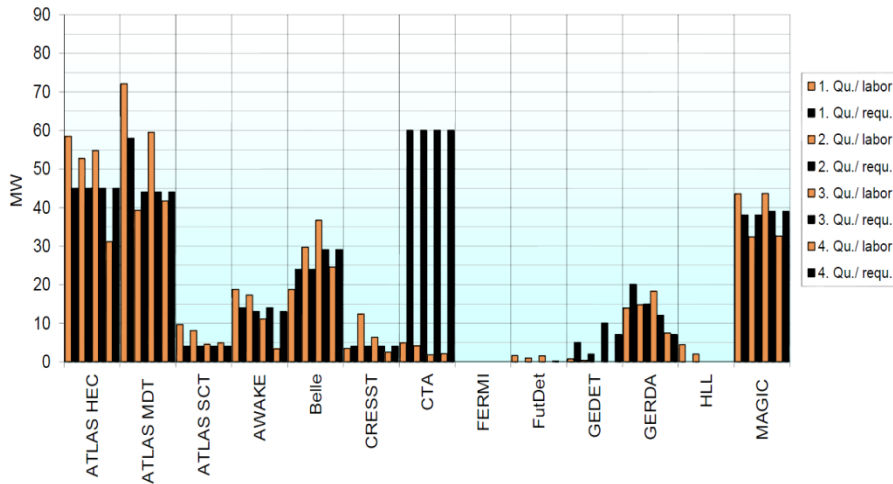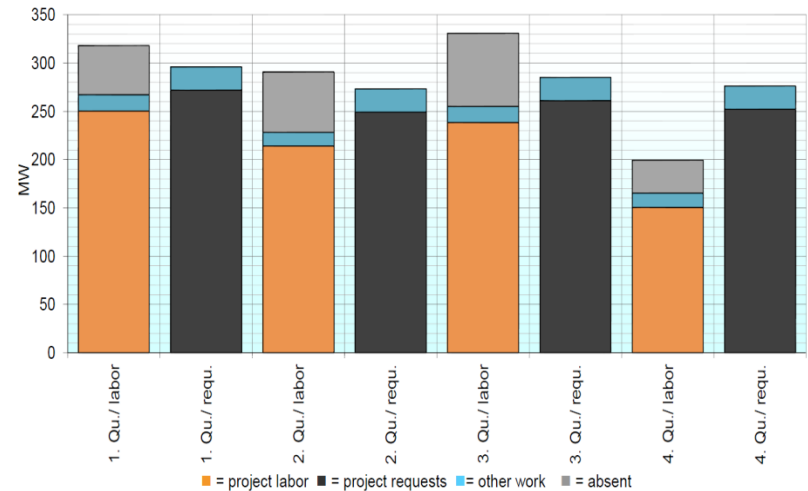- Assumption: 10 MW per quarter and person

EA

EE

EP

Comparison of Labor & Request 2014

- January – November in MW (man-week)

- December is missing
  => lower bars for 4th quarter

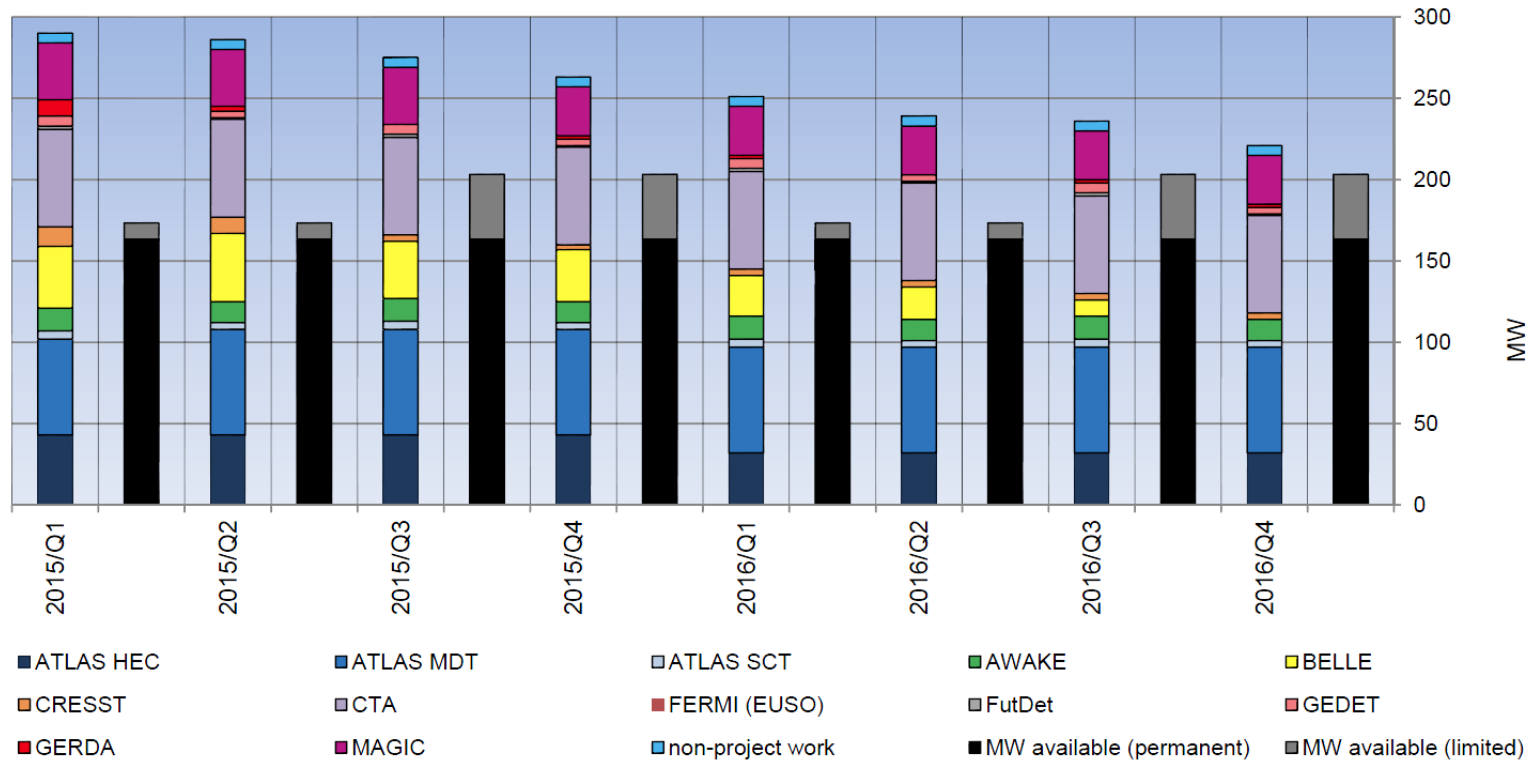- Shift of manpower from MAGIC, ATLAS HEC to Belle-II, ATLAS MDT

Electronics Division labor & requests 2014


Labor vs. requests in total, 2014

Requests for 2015/16

- Main requested projects in 2015/16:
  - MAGIC
  - ATLAS MDT: small chambers, new front-end electronics
  - ATLAS HEC
 - Belle-II: production, Kapton development

Requests for 2015/16

- Demands larger than available resources!
- 2 positions to be filled up for EA in 2015, paid from MDT and Belle's "Zeithilfemittel".

□ Requested
■ Available

EA

EE

EP
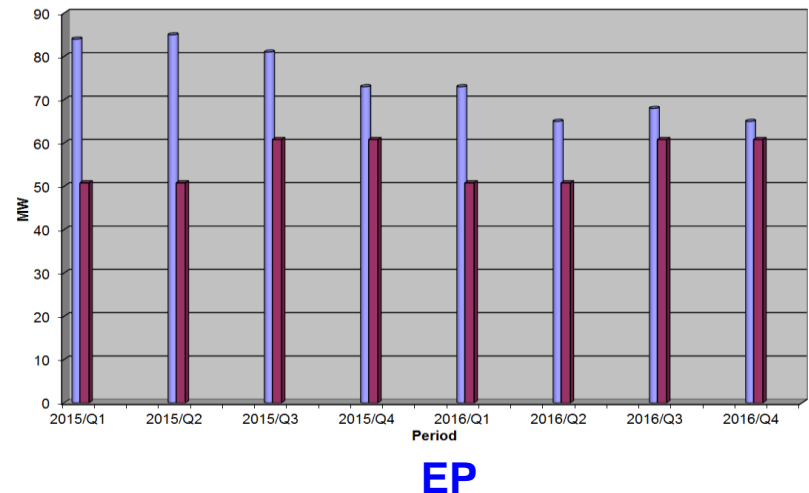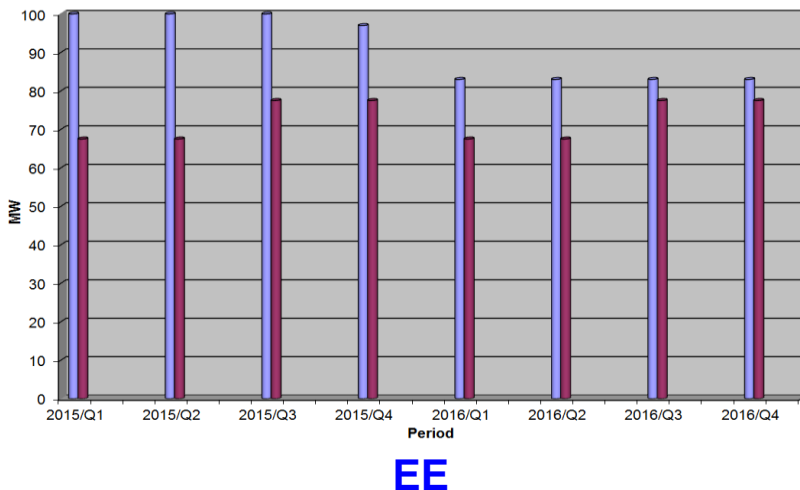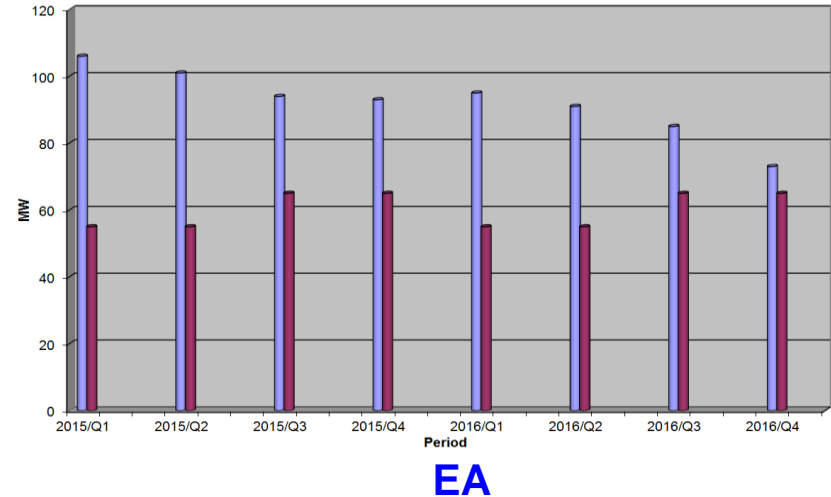
ATLAS MDT: ASD Development

- New ASD chip implemented in cooperation with Sparkling IC in Milan

- Simulation shows improvements in peaking time and ADC-mode operation

- Chip layout has been submitted to the foundry for fabrication in November, 2014, and the die will be received in March, 2015, for measurement
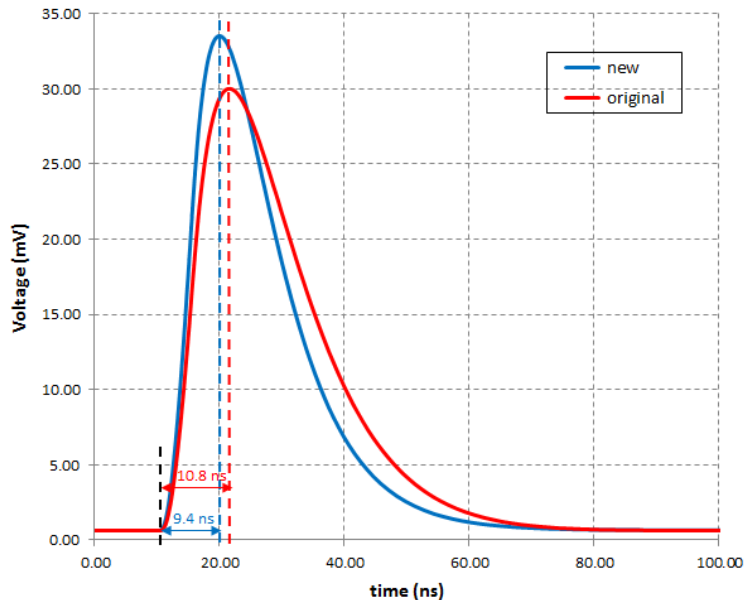

Peaking time improved for Preamp, *e.g.*
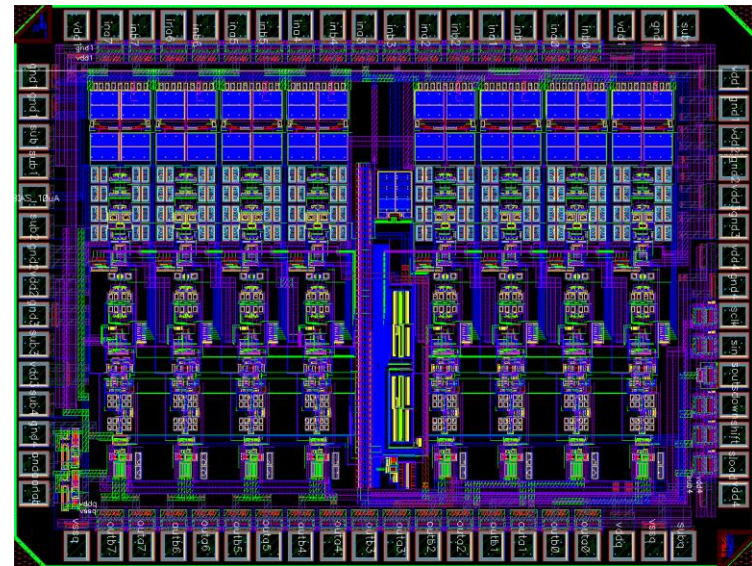
Amplifier-Shaper-Discriminator (ASD): Top Layout

ATLAS MDT: ASD Development

- New functional block – Baseline Restoration (BLR) – under investigation for the next integration
- BLR purpose
  - sMDT chamber has a much higher rate capability ...

  - But performance loss due to undershoot and overshoot in high-speed operation

  - BLR: may constrain undershoot amplitude and affect recovery-time of overshoot
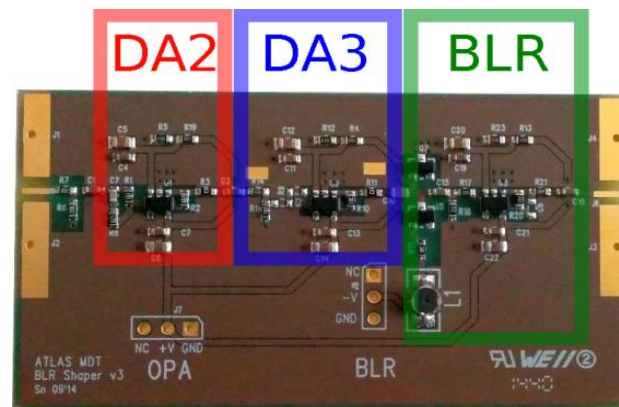

An implementation of BLR in PCB
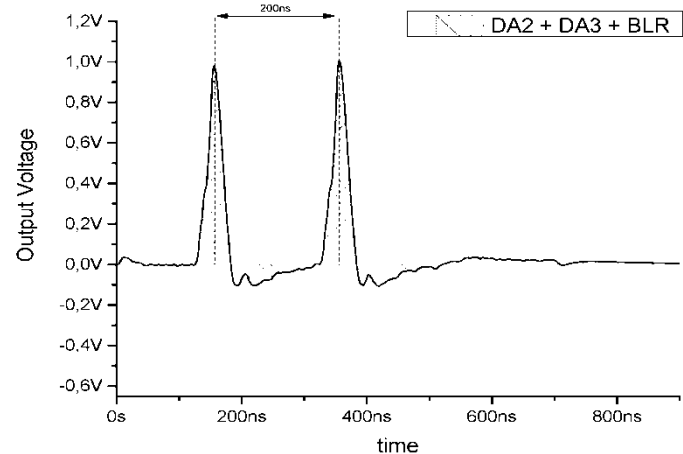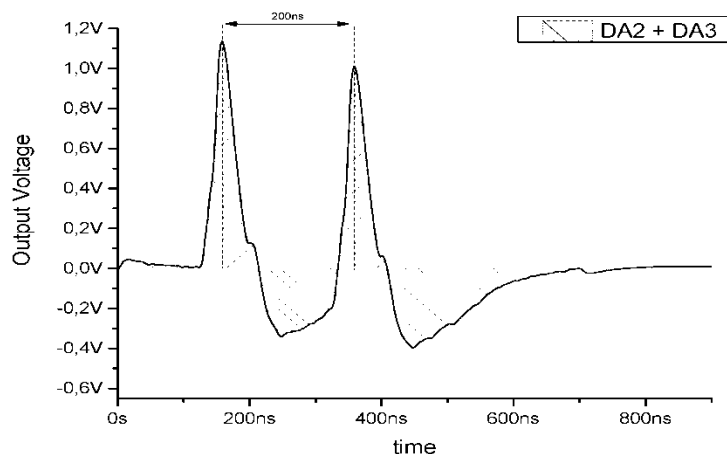
Simulated output of two piled-up signals without BLR (left) and with (right) BLR in PCB

ATLAS MDT: Trigger Demonstrator

- Purpose: Studies of fast hardware-based high p_T-trigger with ~ 10 us latency

- New fast TDC (time-to-digit converter) algorithm implemented in FPGA on trigger mezzanine board

- Firmware development for the communication between mezzanine board and Gigabit link interface board (GLIB) done
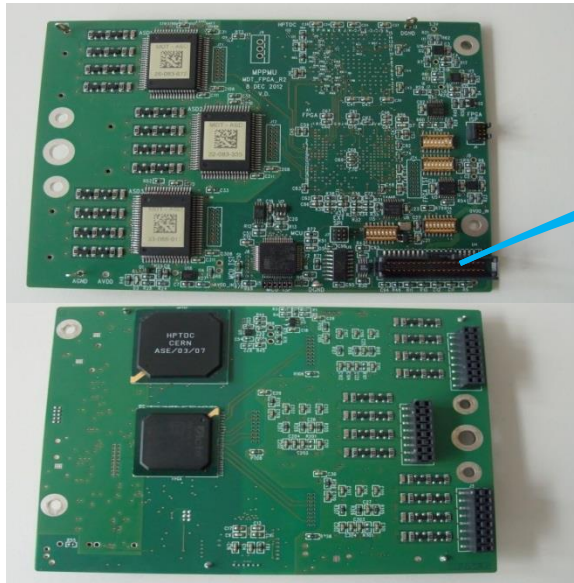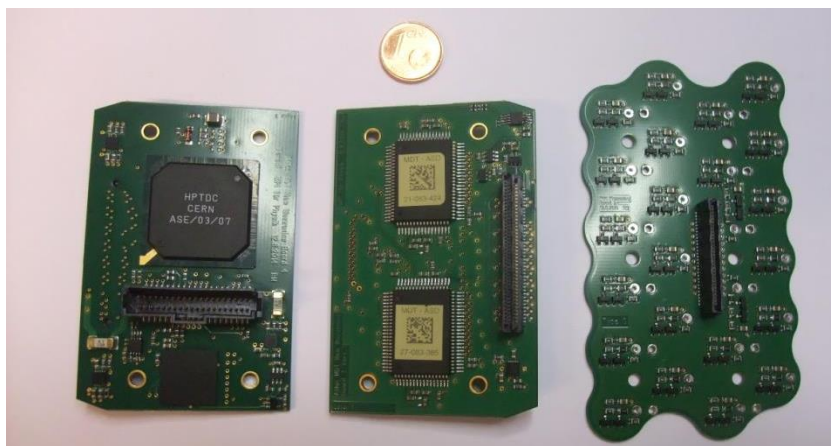

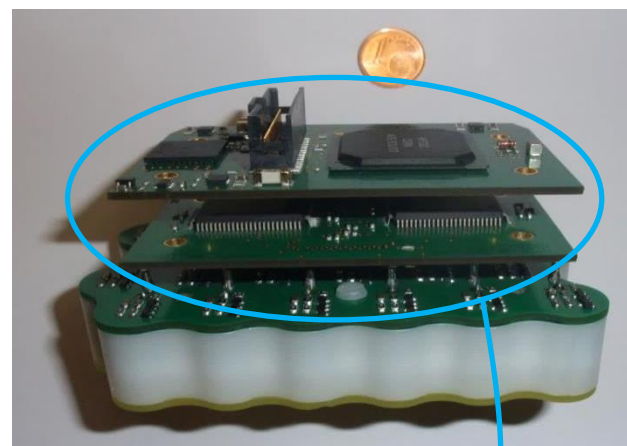Trigger mezzanine card with Actel ProASIC3 600E FPGA running fast TDC firmware
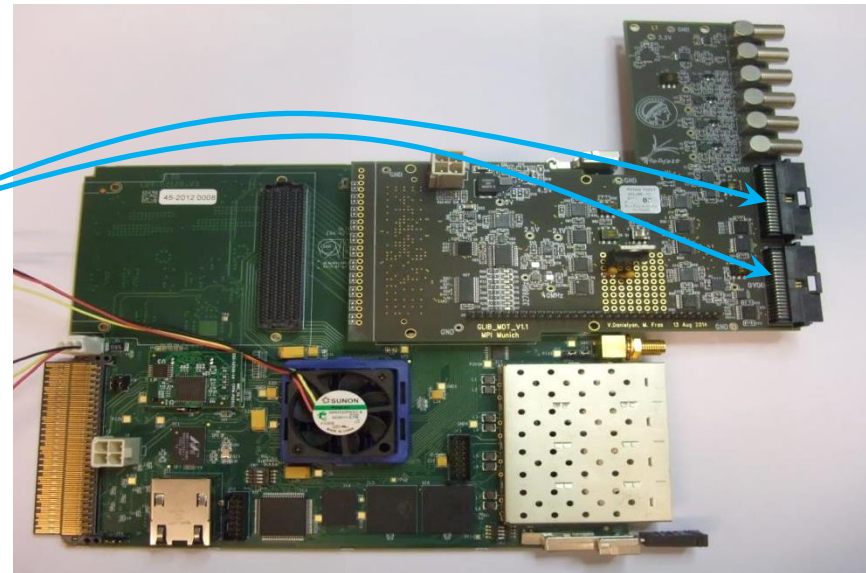
GLIB board from CERN with Xilinx Virtex-6 LX130T FPGA and custom expansion board for 2 mezzanine cards

ATLAS MDT: Small Mezzanine Board

1. Digital (TDC + slow control, left) 2. Analog (ASD, middle)
3. Passive (Termination, Over-voltage protection, right)

Stack including decoupling capacitors
for HW (inside white plastic spacer)

New Mezzanine Module

- For sMDT chambers with 15 mm ϕ tubes

- Stacking to save area

- PCB design, fabrication, FPGA firmware done at electronics division, 250 modules to be produced

- Functions are under test, studies on MDT chamber ongoing
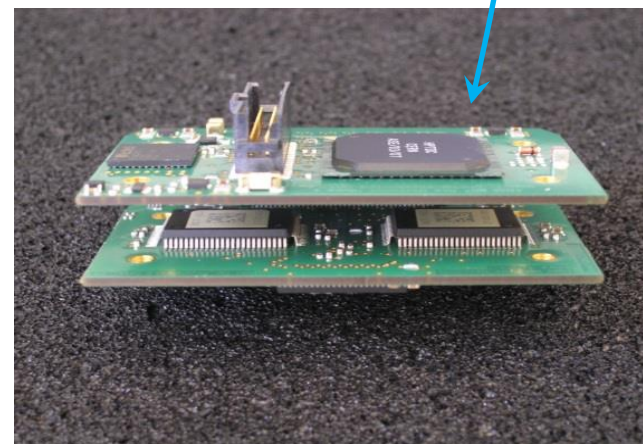
ATLAS MDT: Chambers with Small Tubes

- Adjustment of the semi-automatic machine for wire-tensioning to produce 15 mm tubes up to 1.12 m long

- First 500 tubes will be produced

- Development of test equipment for measurement of leakage current in ±1 nA on tubes under high voltage (3 kV)

- 2 BME chambers with readout electronics and HV supply installed in CERN


BME chamber side view
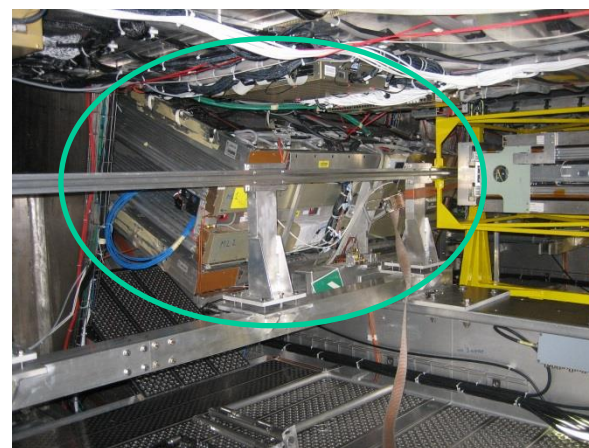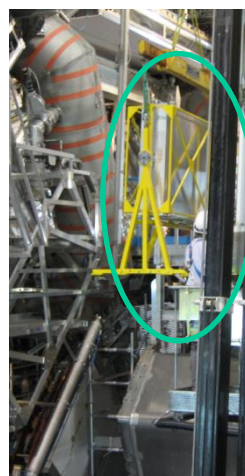
BME chamber installed at CERN

ATLAS HEC: Radiation Test

- Radiation test for standard CMOS technology and current GaAs technology:
  - Radiation hardness of standard CMOS technology strongly depends on if transistors are powered or not during irradiation

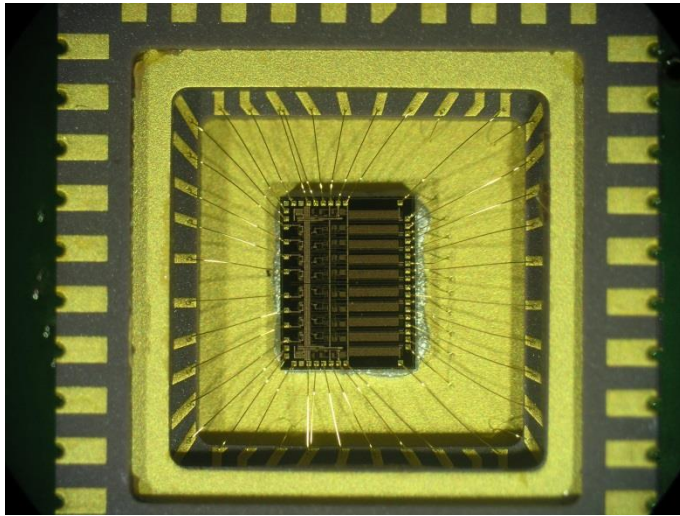 - For GaAs technology, to be powered or not during irradiation makes no difference
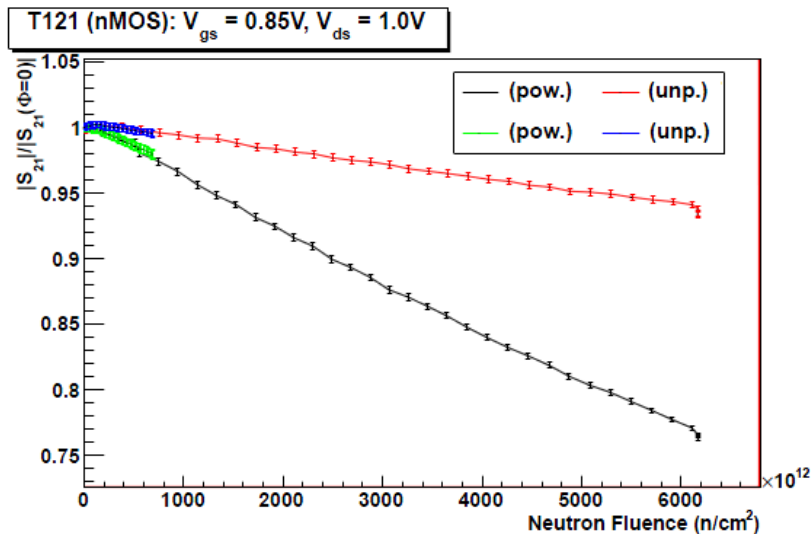
NMOS transistor Gain in function of the irradiation level
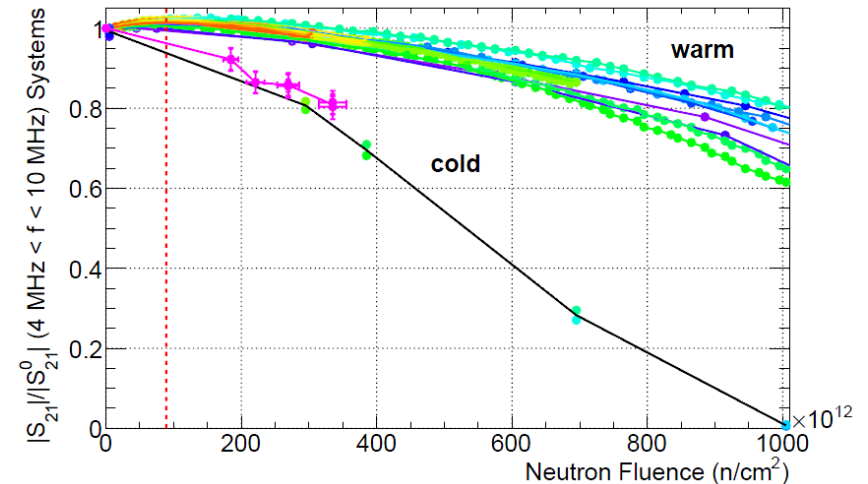
GaAs amplifier Gain in function of the irradiation level

- Extensive irradiation test programs by MPP show that the current readout electronics with GaAs ASICs are enough radiation-hard for HEC

ATLAS HEC: Aging Test

GaAs ASICs wire-bonded in housing

- Aging test for electronics: two temperature tests
  - Cold test: -196°C about 2~3 weeks
  - Warm test: 20°C ↔ 100°C alternatively changed, about 2~3 weeks

- Measured before and after test
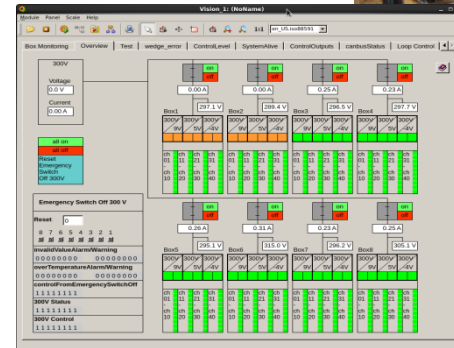- Structure analysis with SEM
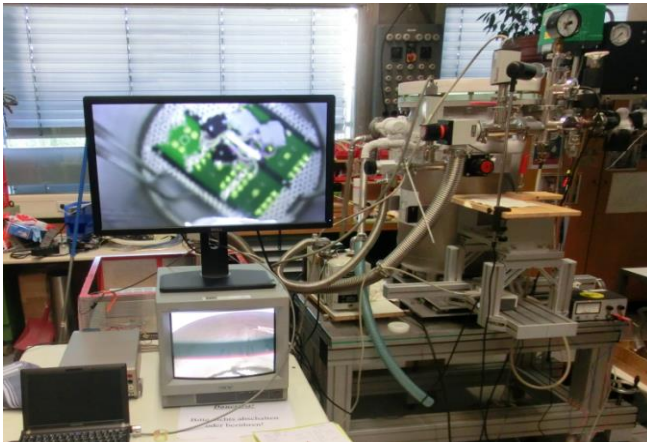
Equipment for cold aging test

Warm aging test in the oven

ATLAS HEC: LV-Supply Upgrades

- New slow control
  - Operating system from Win-XP to Linux
  - Control software ported from PVSS to WinCC
  - New CAN interface hardware

Test setup for the software interface

New user interface for control

LV power supply

- Upgrade for HL-LHC: radiation tests with neutrons and Protons done for logics and power MOSFET

- HEC LV Preamplifier Power supply: 960 output voltages, all controllable by WinCC

Belle-II: Pixel Detector

- Kapton development:
  - Prototype of cable manufactured by 2 companies: Taiyo (Japan), Kaupke (Germany). Both cables have been evaluated, showing room for improvement

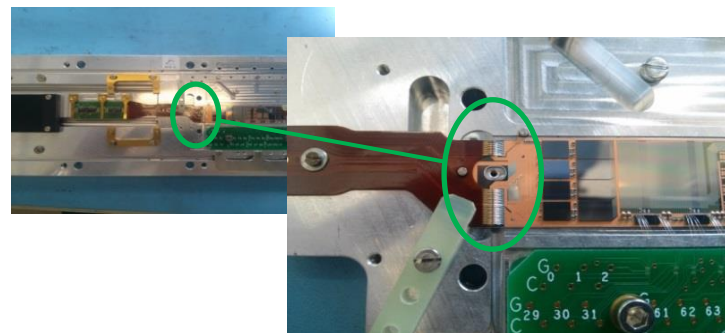 - New design of cable for PXD9 ongoing
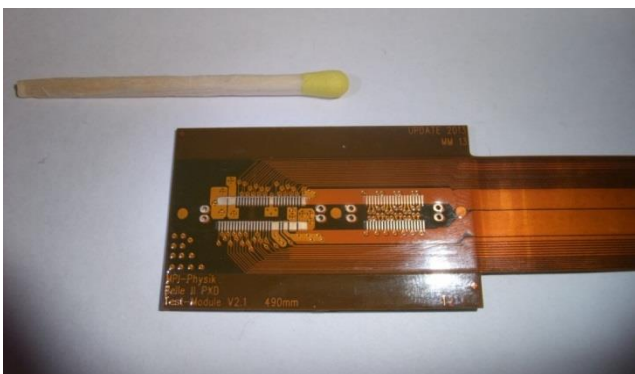
Rigid part for connectors for interfacing power and slow control + readout
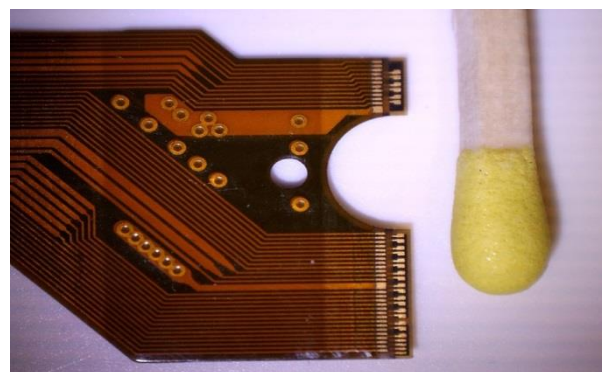
"Shark fin" to be soldered with 4 power pads to the PXD module

- Produce EMCM for tests

- Kapton and Silicon solder connection (Sn42Bi58)

- Studies on maximal current for bonding wires ongoing

- Wire bonding and reliability test afterwards

IB-Belle: CO₂ Cooling System

- CERN first implemented CO_2 system, also interesting for Belle-II

- The same system to be duplicated in MPP, 2015

- At present, CO_2 cooling system specification planned and components defined

CO₂ cooling system at CERN

Serval device for CO2 cooling system

CRESST & GERDA

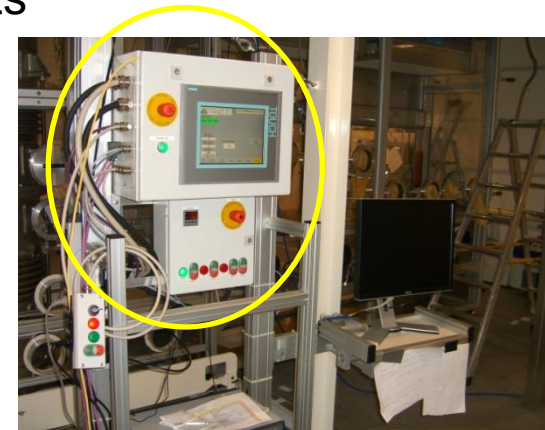- Remote pressure monitoring system for the condenser designed and manufactured for CRESST


Remote pressure monitoring system

- PLC (programmable logic control) for GERDA lock control in Gran Sasso installed
- Extensive tests

PLC controller in the underground laboratory, Gran Sasso

PLC controller for GERDA lock control in MPP
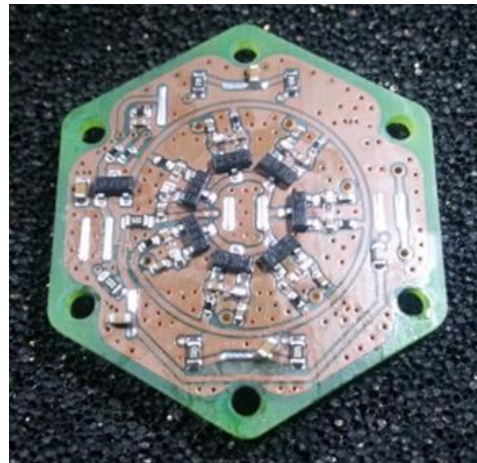
MAGIC: SiPM Pixel

- SiPM pixel module:
  - Pixel module electronics designed, simulated and fabricated for MAGIC Cluster prototype
  - Based on Geiger-mode avalanche photodiode array sensors
  - Designed for fast current signal response despite large parasitic capacitance
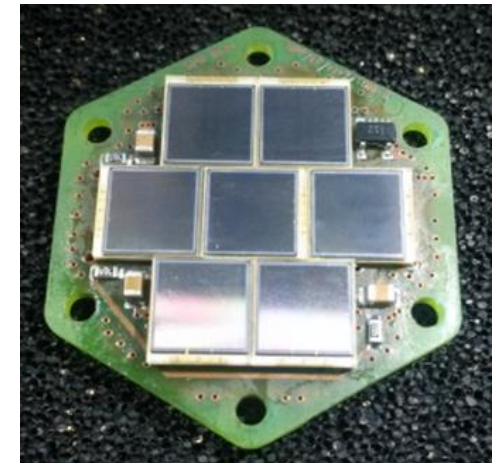 - Deployment in 2015
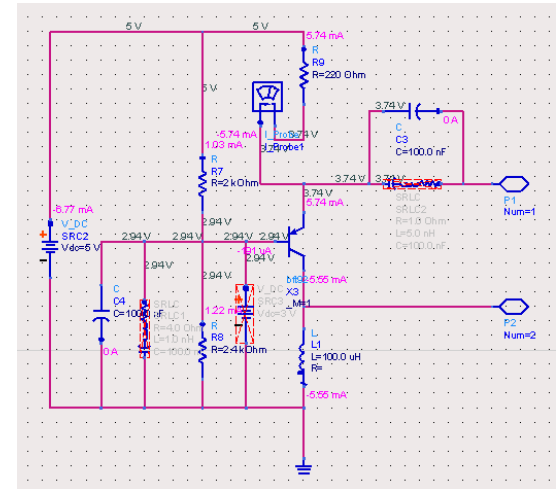
Amplifier schematic used in SiPM pixel
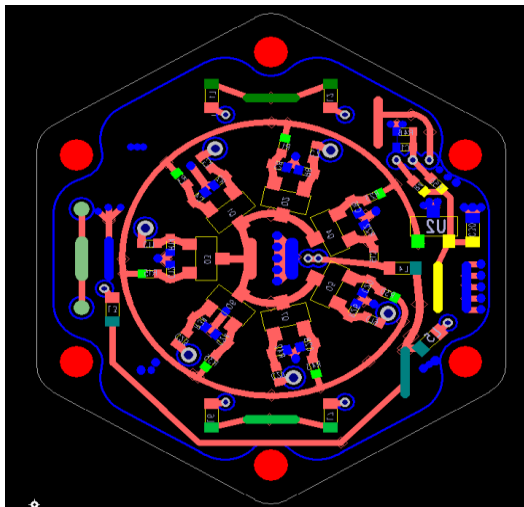
SiPM pixel layout

Implemented module with electronics

Module with SiPMs

MAGIC: SiPM Interface

- SiPM interface board:
    - It is the front-part of SiPM Cluster, used to control and readout the photodiode array by 40 analog outputs, 12-bit digital resolution DAC

    - It measures up to 48 analog values converting to 12-bit digital signal by ADC

    - Consisting of 48 programmable digital I/O

    - Serial interface to the Slow Control of MAGIC Camera, optically isolated for low noise consideration
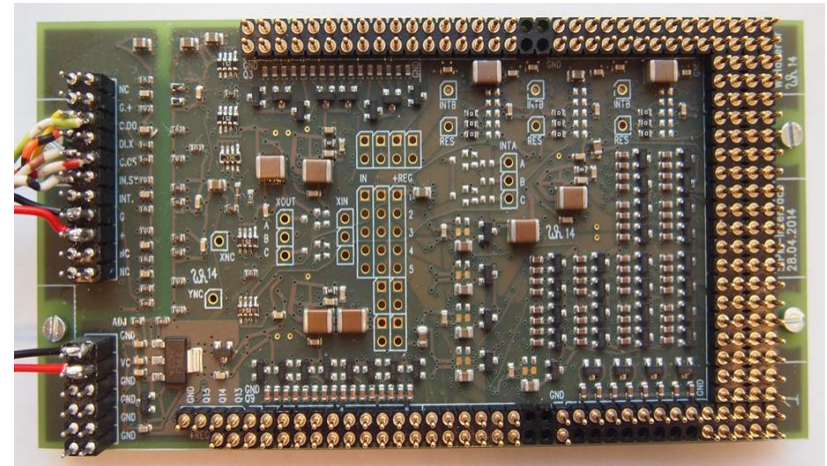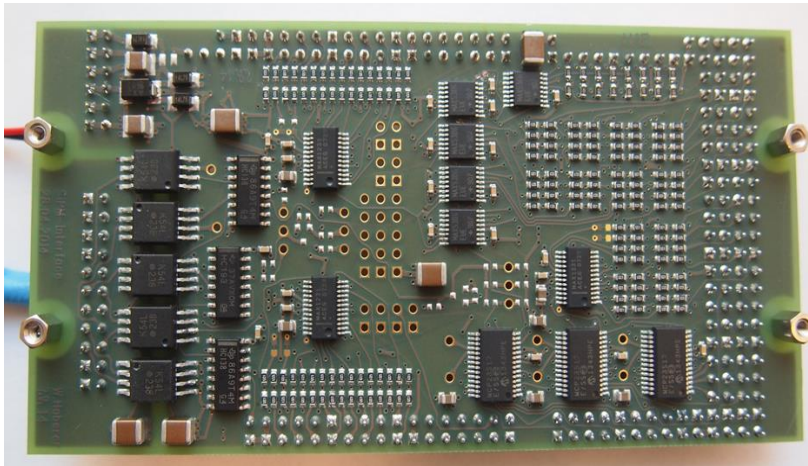
SiPM interface board to control and readout the photodiode array

MAGIC: Maintenance

- Installation of additional vibration measurement systems for continuous operation in La Palma

- Repairing and maintenance for the telescope after ice damage

Before

After

Miscellaneous

- Two new production machines in EP

Laser cutting system

Reflow soldering machine

Conclusion

- Much work on-going in 2014 ...

- More to do in 2015/2016!

- More manpower welcome in 2015/16!

Thank you for your attention!!