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DHPT 1.0 PRELIMINARY RESULTS

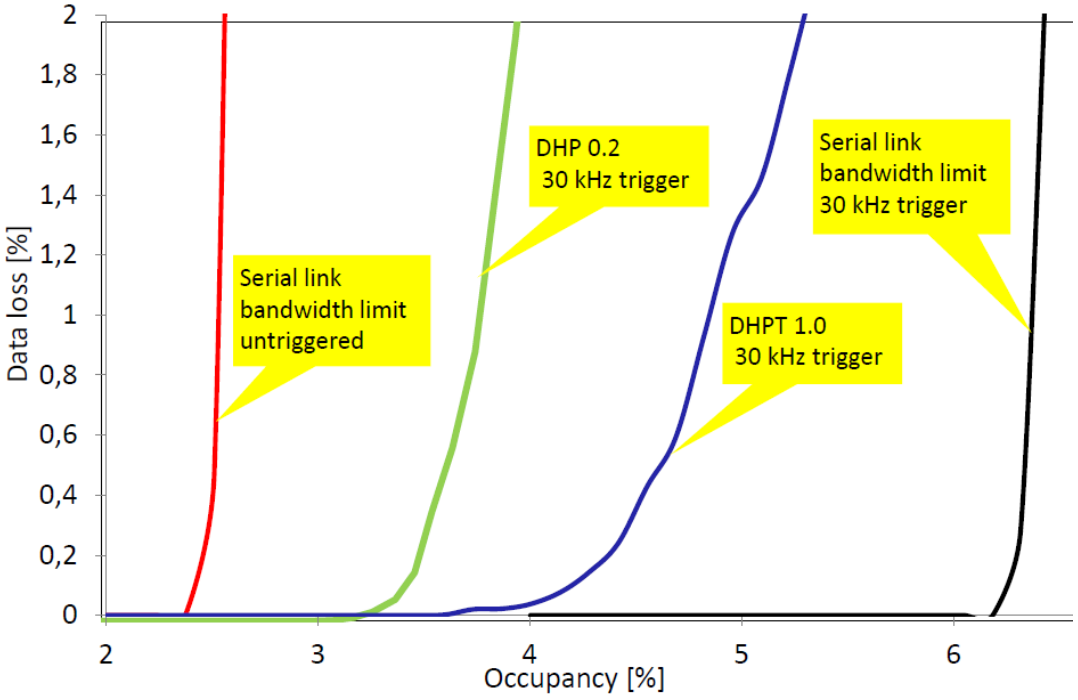
Chip versions

DHP 0.2

- 90 nm CMOS technology
- ~3.5% occupancy (triggered)

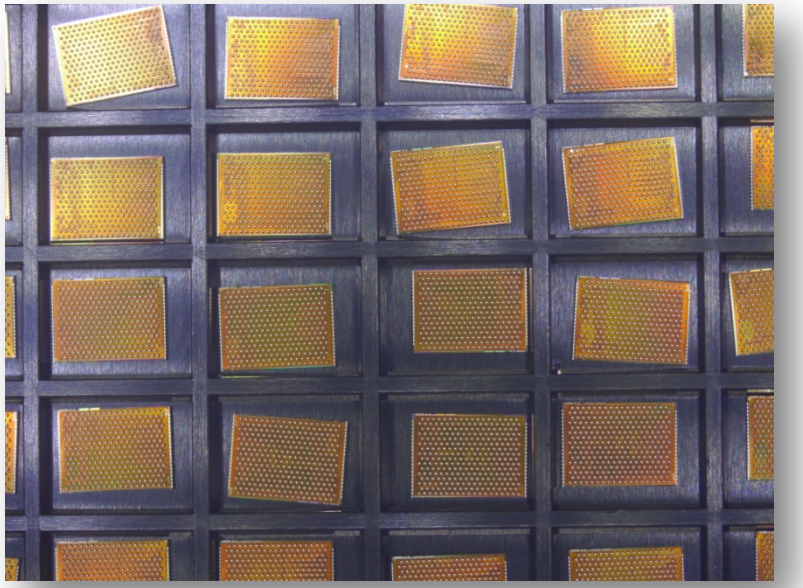
DHPT 1.0

- 65 nm CMOS technology
- ~5% occupancy (triggered)



- DHP02 pin compatible
- Gated mode support
- Enhanced data processing
- Fast commands support(via trigger line)
- Advanced delays' tuning (for higher speeds support)
- Differential clock for DCD

Test Results



- ✓ LVDS lines
- ✓ JTAG interface
- ✓ Fast commands recognition via the Manchester encoded trigger line
  - Memory dumping
  - Veto mode
  - Reset
- ⚠ Serializer -> ok, but tweaks should be applied to run it correctly. Higher voltage and/or slower reference clock.

Switcher lines configuration

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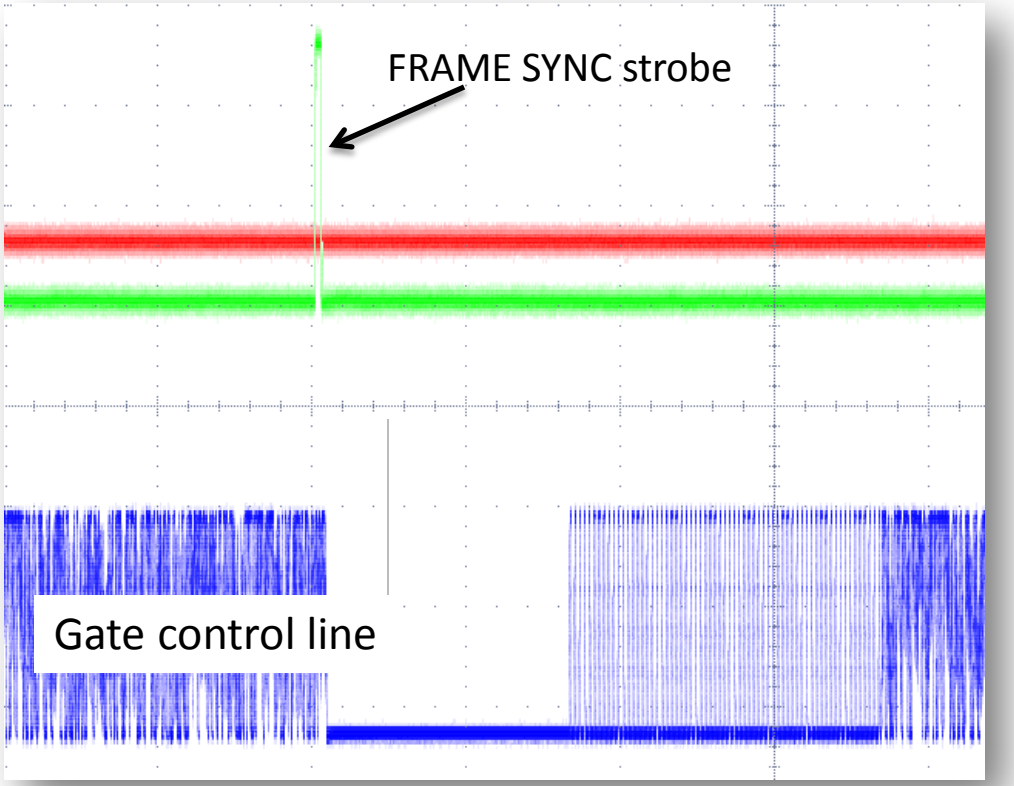
- (New) completely flexible configuration of the switcher line on the row-per-row basis for the normal and gated modes.



Summary

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- First test results show that the new DHPT 1.0 works fine, and will be probably usable for EMCM and other upcoming tests. However, some deviations from the default conditions are necessary to run it properly.

- Further tests are needed for complete chip investigation (date processing, DCD-DHP integration)

- For production, another chip iteration (DHPT 1.1?) will be scheduled to fix the minor bug found