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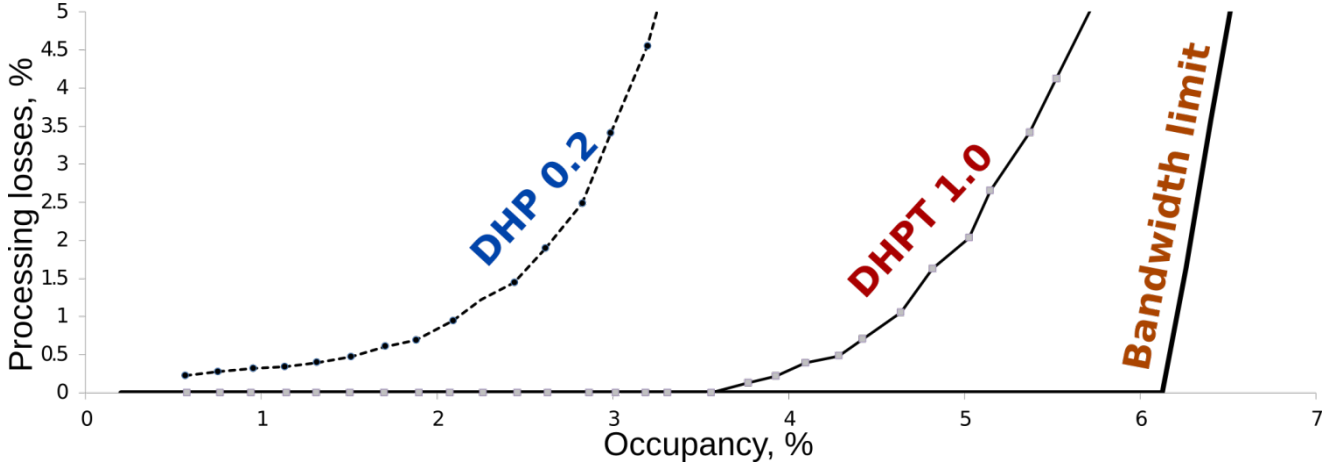
DHPT 1.0 TEST STATUS

DHPT 1.0

- DHPT 1.0 is a full size Data Handling Processor implemented in 65 nm TSMC CMOS technology.
  - Enhanced Data Processing
  - Overflow Handling
  - Command Interface (Manchester Encoding)
  - Fine adjustment of the DHP – DCD timing settings
  - Etc. …



DHPT 1.0 tests

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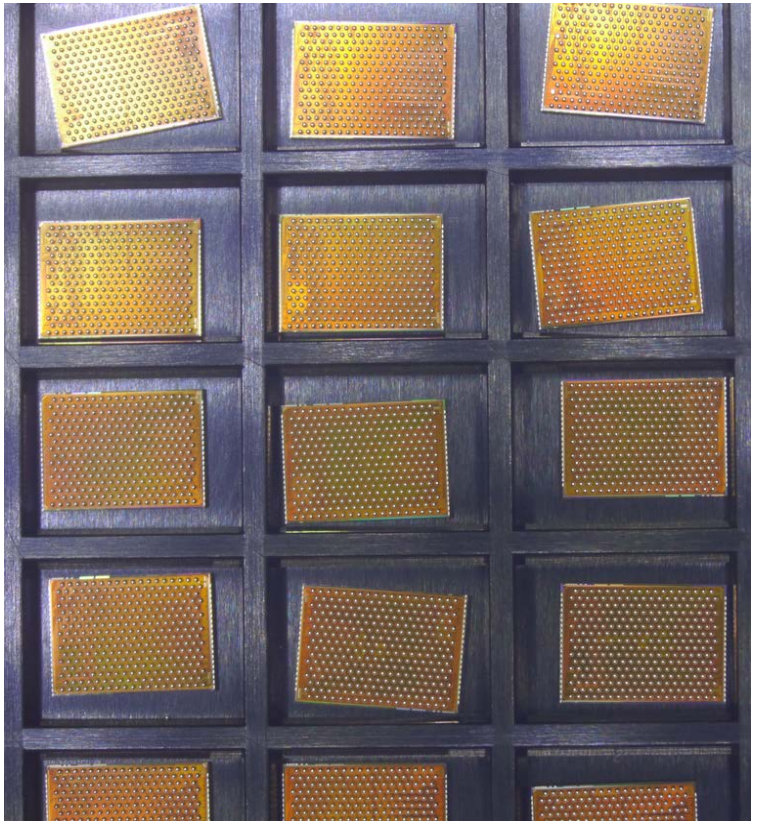
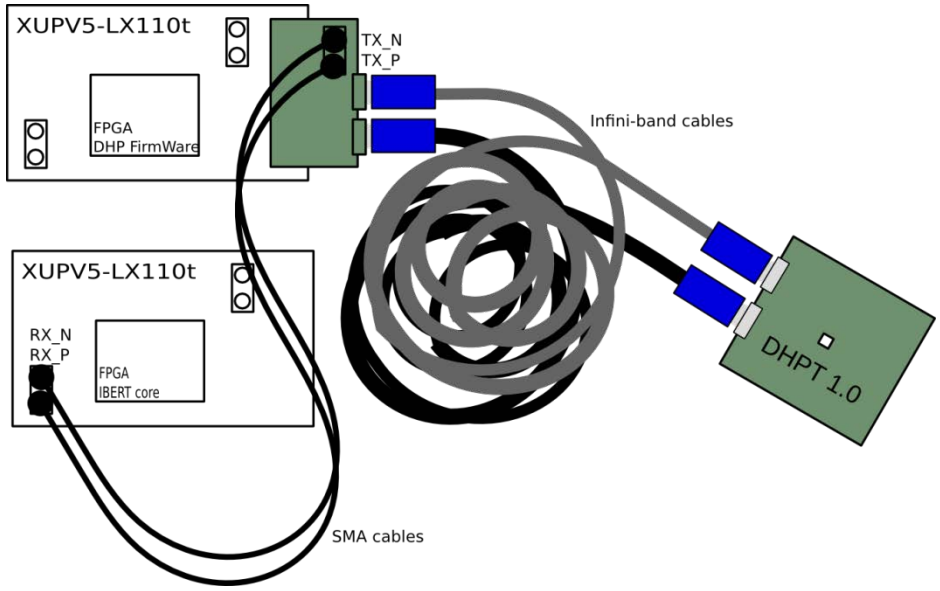
Highlights

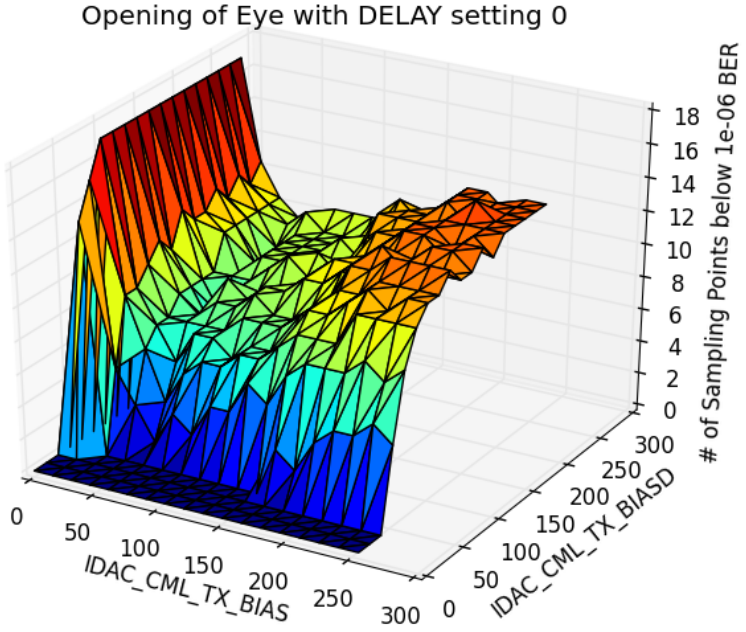


- Analog part
  - ✔ Gigabit link (Leonard Germic)
    - ✔ Data transmission
    - ✔ BERT (TBD)
    - ✔ Parameter optimization
  - ✔ Temperature sensor (Oscar Alonso)
  - ✔ Delay Settings
    - ✔ DCD clock, Row2sync
    - ✔ Switcher settings
    - ✘ Per channel delays (for DCD-DHP adjustment)

IBERT tests (Leonard Germic)

- Error rate tests and parameters optimization for designed 15m cables





Parameter optimization for 15m data cable

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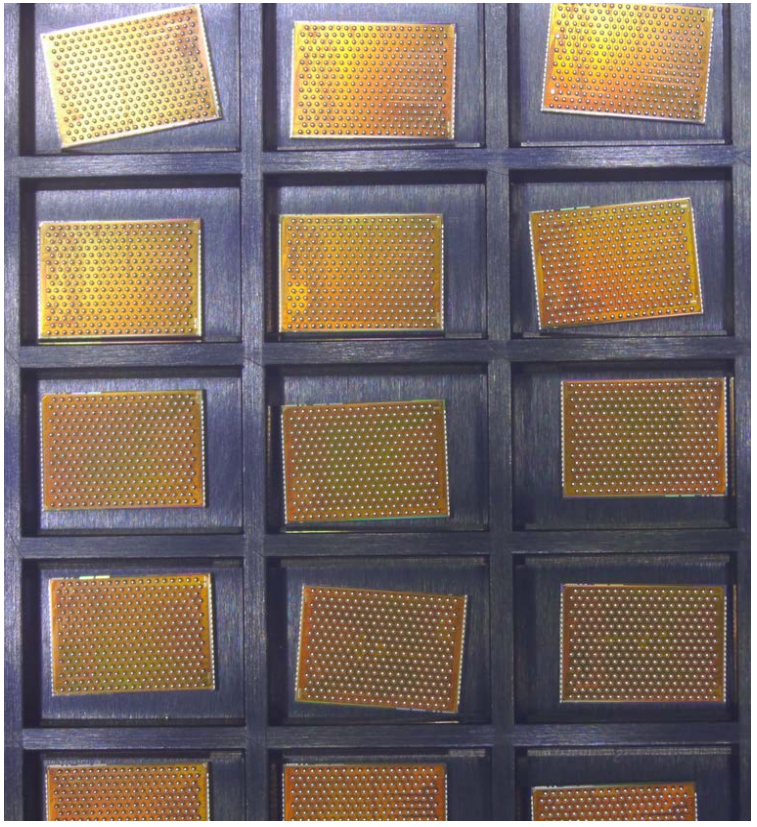
Highlights



- Digital part
  - ✔ Manchester encoded trigger line
    - ✔ Memory dump
    - ✔ TRG+RST+FSYNC
    - ✔ Veto Sequence generation
  - ✔ Memory configuration via JTAG
  - ✔ Temperature sensor
  - ✔ Data Processing
    - ✔ Channel masking
    - ✔ Double precision common mode
    - ✗ High occupancy tests

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- The following (non-critical for prototyping) issues were observed and should be corrected for the next chip iteration:
  1. Serializer timing issue (works only with non-standard conditions)
  2. Fine tune delays for DCD-DHP interface
  3. Data processing stability for high occupancies
  4. Wrong Common mode values for high occupancies (probably related to 3)

- Remains to be done
  - DCD-DHP setup tests
  - Needle board test setup to be prepared

- DHP 1.0 manual will soon be available

DHPT 1.0 planner

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DHPT 1.0 Planner - Google Chrome

DHPT 1.0 Planner

File Edit View Insert Format Data Tools Help Last edit was 7 days ago

DHPT 1.0 Test Plan

	A	B	C	D	E
7		Eye diagram @ 15m	Leonard	ok	
8		BERT	Leonard	ok	
9		Parameter optimization for VDD_CML, bias and delays	Leonard	ok	
10	**Temperature Sensor**				
11		DAC	Oscar	ok	
12		Calibration	Oscar		
13		Automation	Leonard		
14		ADC_UB JTAG register readback			output bit sequence to be corrected
15	**HSTL**				
16		needle card	Mikhail		
17		DCD+DHP	Mikhail		
18	**LVDS_TX+CMOS_OUT**				
19		DCD_CLK	Leonard		
20		SW_XXX	Leonard		
21		delay settings dcd_cmos_clk_dly	Leonard	ok	
22		dcd_row2_sync_dly	Leonard	ok	
23		offset_dly[][]	Leonard	no	does not move to chages
24					
25	**Digital**				
26	**Mem test**				
27		data via JTAG	Mikhail	ok	when writing 144 bits, change the order of {src+data} to {data+src} for the readback to be correct also it would be nice to have the following address space: mem_select=conf_address[3:0], mem_address=conf_address[13:4]
28		offset via JTAG	Mikhail		
29		SW sequence via JTAG	Mikhail	ok	
30	**Switcher sequencing**				
31		Normal <> Veto transition		ok	
32	**Trigger modi**				
33		FSYNC	Mikhail	ok	
34		VETO	Mikhail	ok	
35		TRG	Mikhail	ok	
36		MEM_DUMP	Mikhail	ok	
37		RST	Mikhail	ok	
38	**Data Processing**				
39		Common Mode	Mikhail	ok	wrong CM processing with occupancies >1%
40		Set number of channels	Mikhail	ok	
41		Double Precision	Mikhail	ok	
42		Zero Suppression Efficiency	Mikhail		cannot be done because the chip stucks at high occupancies
43		High Occupancy Test (overflow reconvery)	Mikhail	stucks at high rates	> 1% !!!!
44	**DCD interface**				
45		Test sequence	Leonard		
46		data receiver (HSTL)	Leonard		
47		Full speed (delay settings)	Leonard		
48		DAC offset settings	Leonard		
49	**Automation**				
50		Script for pedestal acquisition			
51		Time offset settings to work with the full speed			
52					
53					
54					
55					
56					
57					

New Features + Bug Fixes | Verification plan | Comments, ideas (put them here) | Analog fixinging | DHPT 1.0 Test Plan

Try the new Google Sheets

THANK YOU