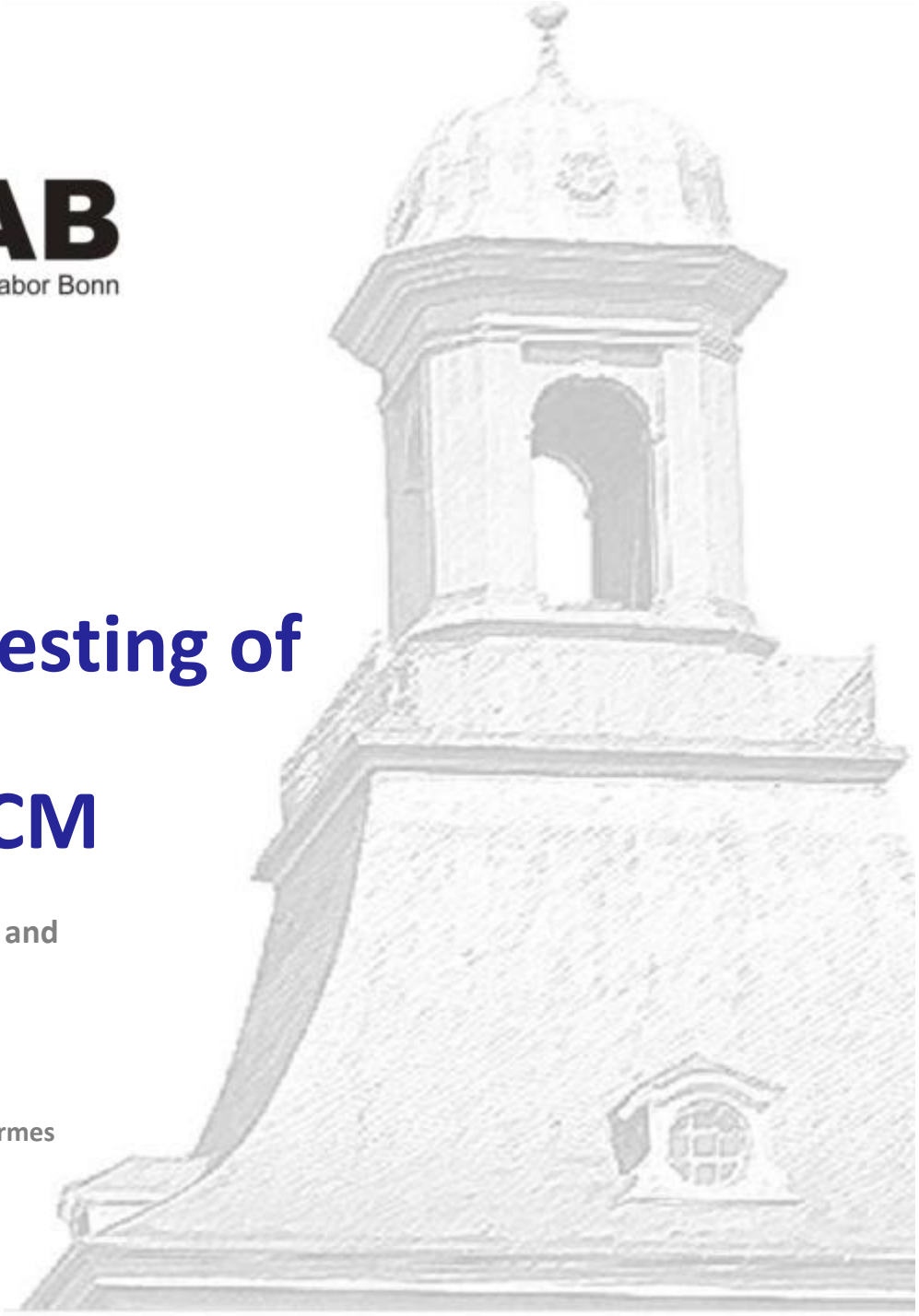
universitätbonn

SI LAB
Silizium Labor Bonn



The results of the Needle testing of

DHPT 1.0 for the EMCM

16th International Workshop on DEPFET Detectors and Applications

25-28 May 2014, Kloster Seeon

Leonard Germic, Carlos Marinas, Hans Krüger, Norbert Wermes

University of Bonn

germic@physik.uni-bonn.de

Contents

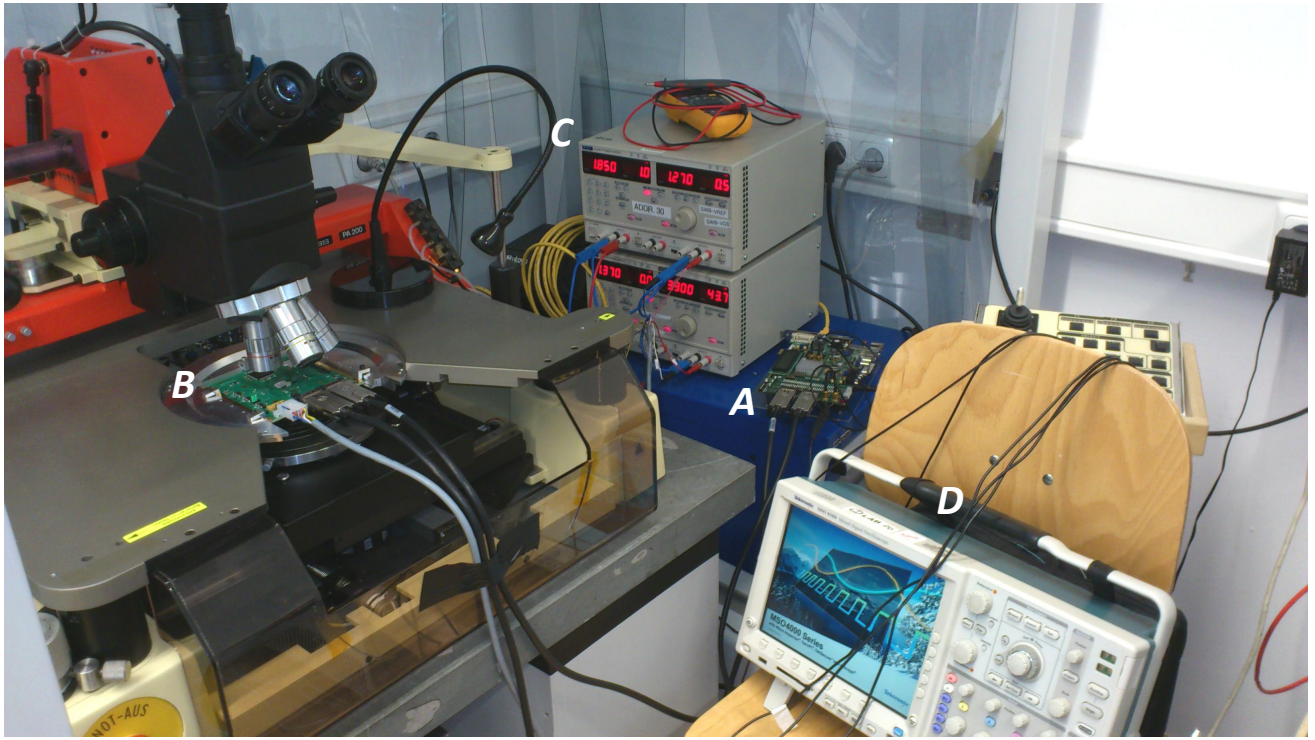
universitätbonn

- Needle card test system
- Bumps connection
- First progress
- Issues
- Outlook

Needle card test system

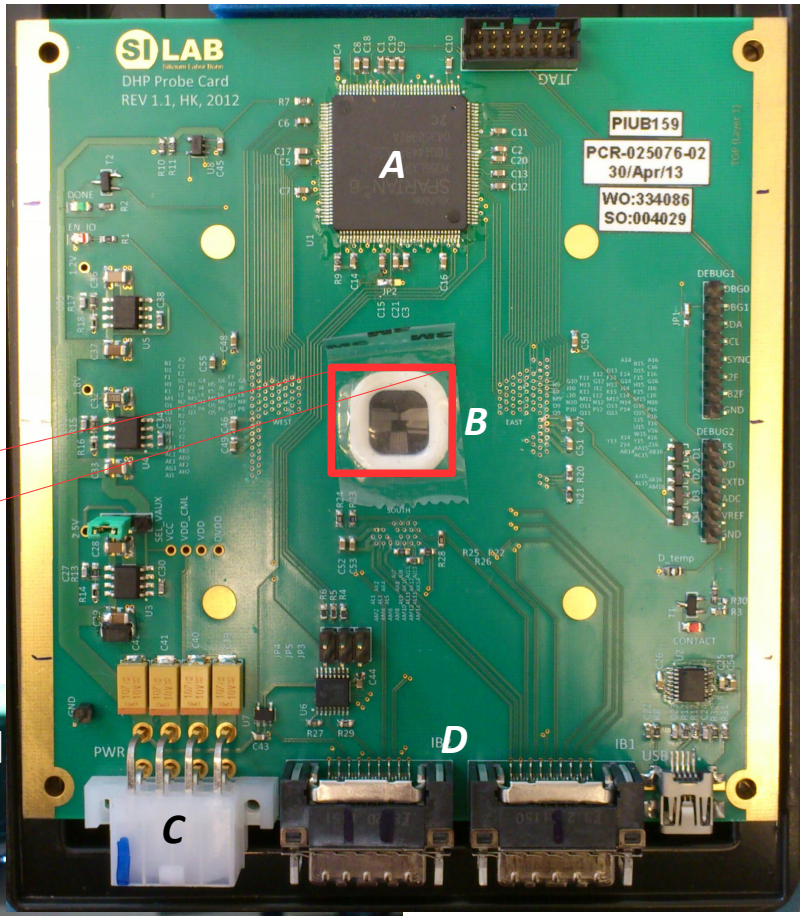
universitätbonn

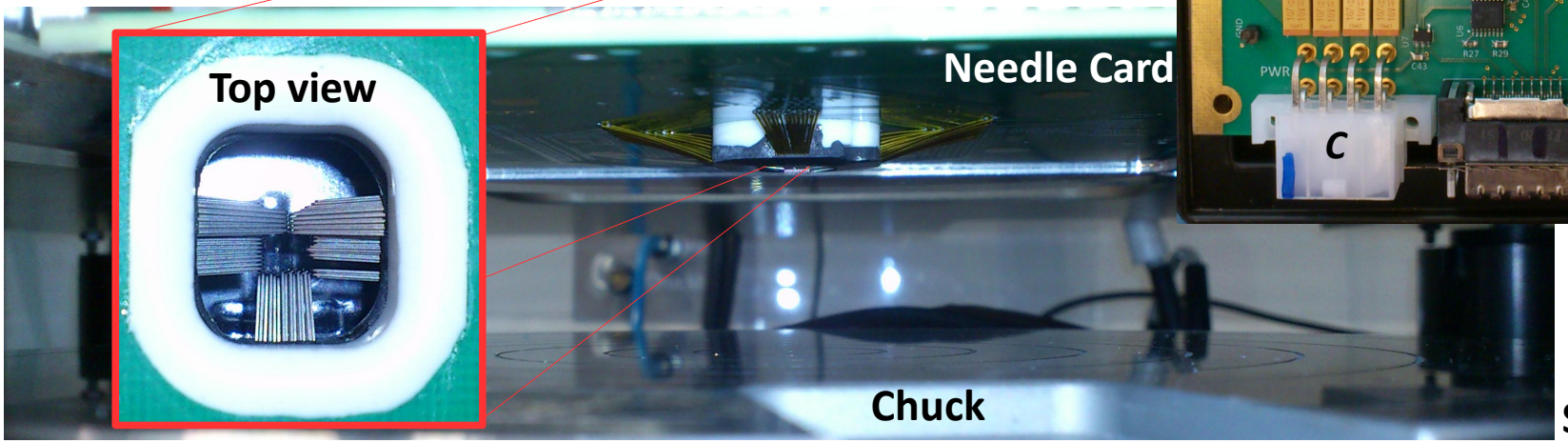
- Xilinx XUPV5 Evaluation Platform (DHH emulator) A
- Needle card with DCD emulator B
- Power VDD = 1.2V, VDD_CML = 1.2V and DVDD = 1.8V C
- 1 GHz Oscilloscope D



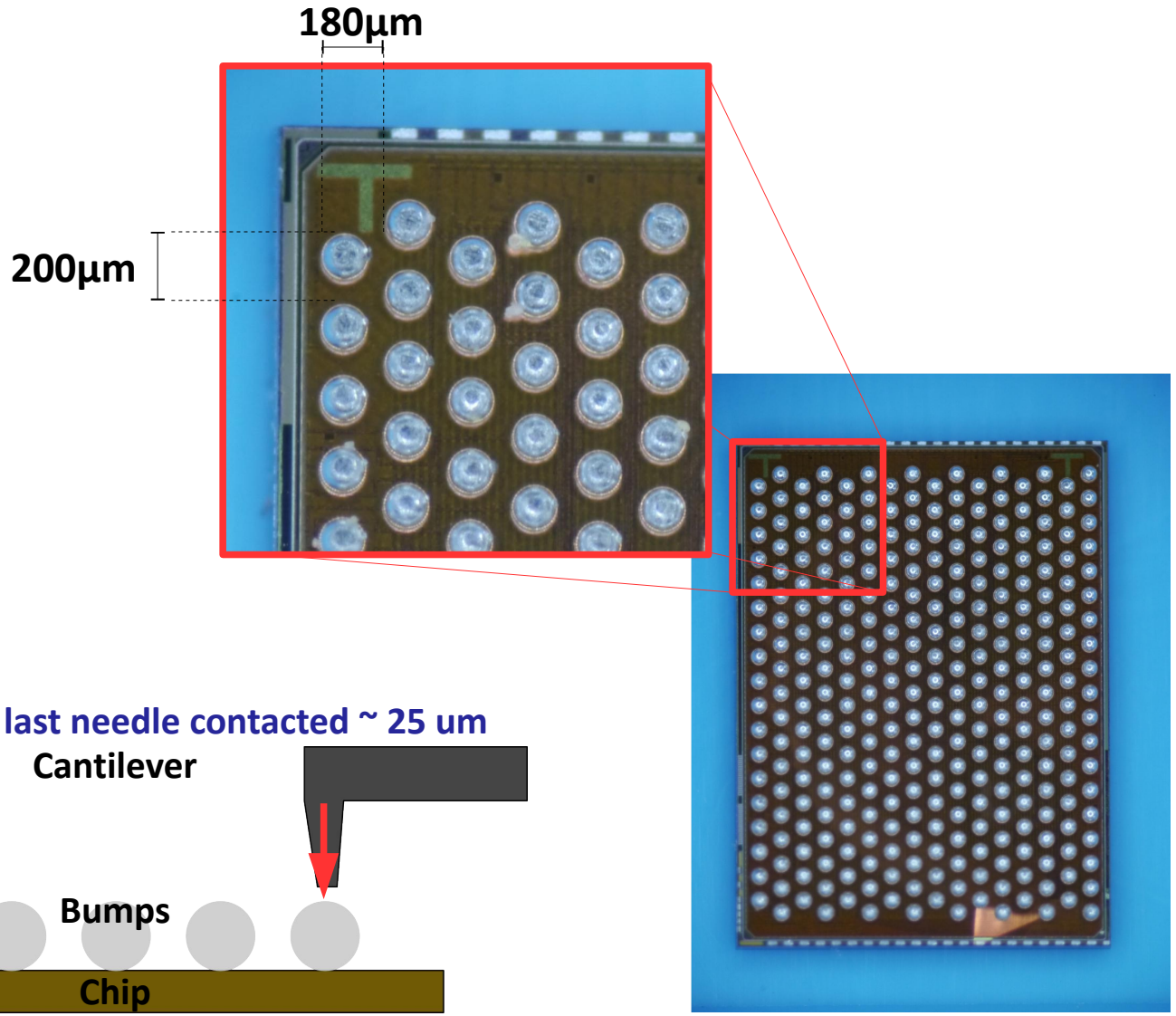
Needle card test system

- Xilinx Spartan 6 (DCD emulator) A
- Cantilever Needles B
- Power Connector C
- Infini Band Connector to DHH emulator (Data, JTAG) D





Side view

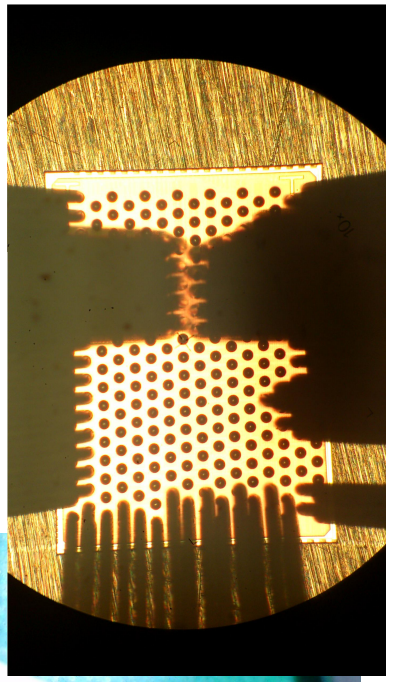


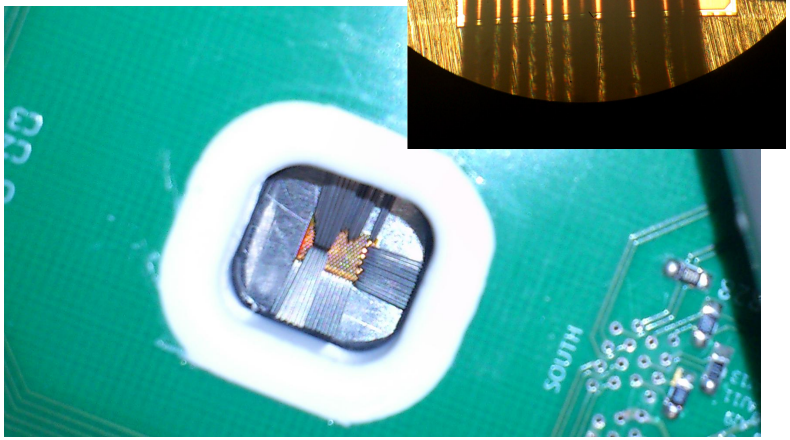
- 158 bumps connected
  - Power, JTAG, DCD I/O and SW
- Oxide on bumps

- Over travel of the needles after last needle contacted ~ 25 um

Bump Connection

- For good connection of the bumps high over travel is needed → High stress for the needles
- Sensitive to alignment of the needles
- On needle card some mechanics will be mounted (back plate) for higher stiffness





- Powering VDD (core), VDD_CML (serial link) and DVDD
  - Current consumption
- Stable JTAG communication
  - DHH (Configure DHPT)
  - DCD (Dis/enable DCD from JTAG chain)
- Serial link
  - PLL
  - CML driver
- SW sequence (Gated mode, etc)

Tested Chips

universitätbonn

#Chip ID	Power			JTAG			DCD	Serial Link		Issues
	GCK	VDD+VDD_CML	DVDD	DHH	DCD	sw sequence	Data	PLL	CML dirver	
1	x	<10mA	<30mA	x	n/A	n/A	n/A	n/A	n/A	no response
2	ok	~90mA	~37mA	ok	ok*	ok**	n/A	ok	ok**	
3	ok	~82mA	~42mA	ok	ok*	ok**	n/A	ok	ok**	
4	ok	~104mA	~31mA	ok	ok*	ok**	n/A	ok	ok**	
5	ok	~105mA	~39mA	ok	ok*	ok**	n/A	ok	ok**	
6	ok	~102mA	~38mA	ok	ok*	ok**	n/A	ok	ok**	
7	ok	~103mA	~38mA	ok	ok*	ok**	n/A	ok	ok**	
8	ok	~90mA	~32mA	ok	ok*	ok**	n/A	ok	ok**	
9	ok	~97mA	~34mA	ok	ok*	ok**	n/A	ok	ok**	
10	ok	~101mA	~33mA	ok	ok*	ok**	n/A	ok	ok**	
11	ok	~111mA	~40mA	ok	ok*	ok**	n/A	ok	ok**	
12	ok	~113mA	~31mA	ok	ok*	ok**	n/A	ok	ok**	
13	ok	~106mA	~36mA	ok	ok*	ok**	n/A	ok	ok**	

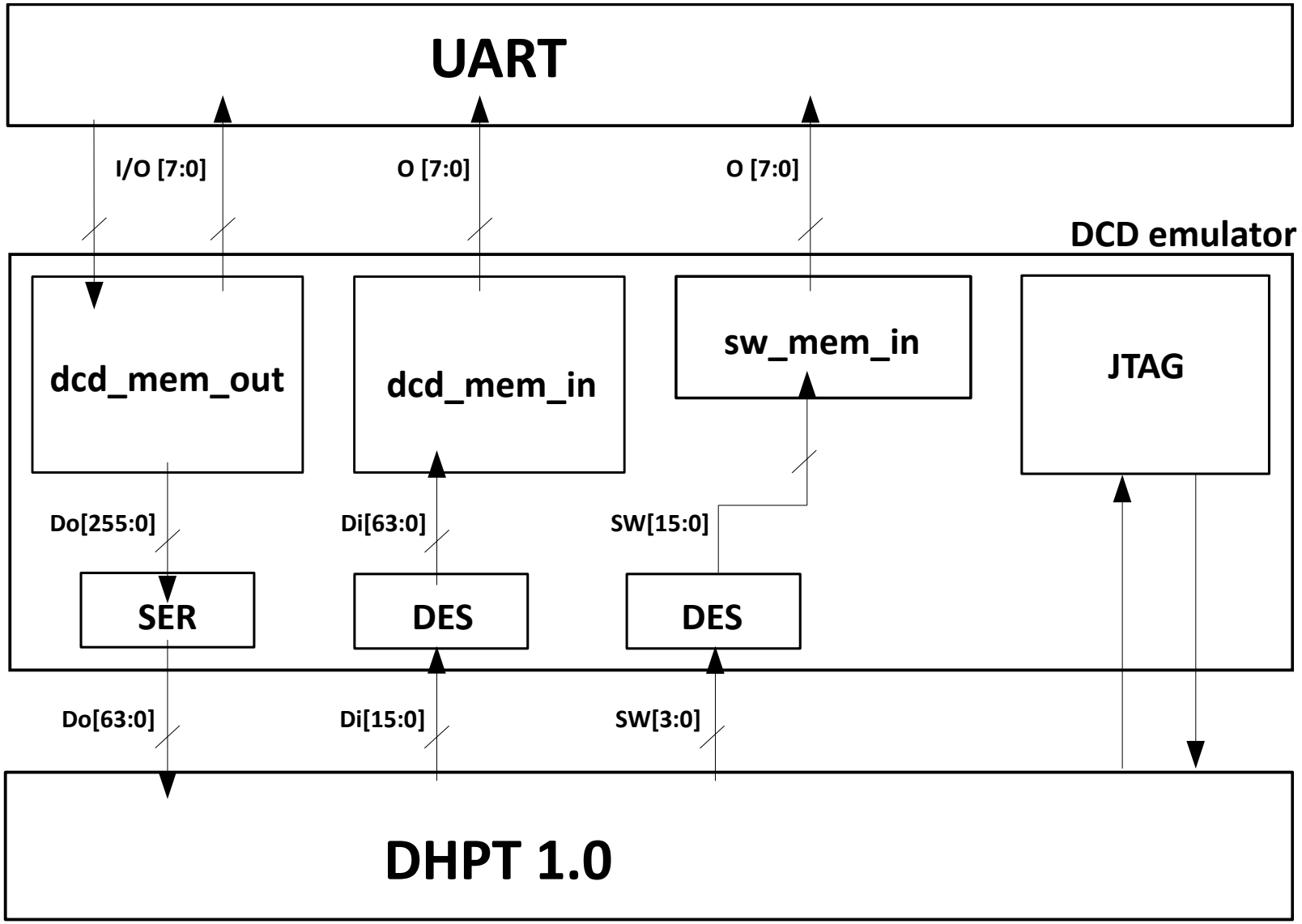
- ok* loop back: DHH emulator → TDI → DCD emulator → TDO → DHH emulator
- ok** Oscilloscope inspection (incl. Gated mode via veto (trigger) and LFSR output)

Issues

- Contact with needle
- Oxide on bumps
- Power drops suddenly
  - VDD, VDD_CML or DVDD bumps disconnected?
- No GCK on chip
  - PLL, CML not working
  - Core not clocked

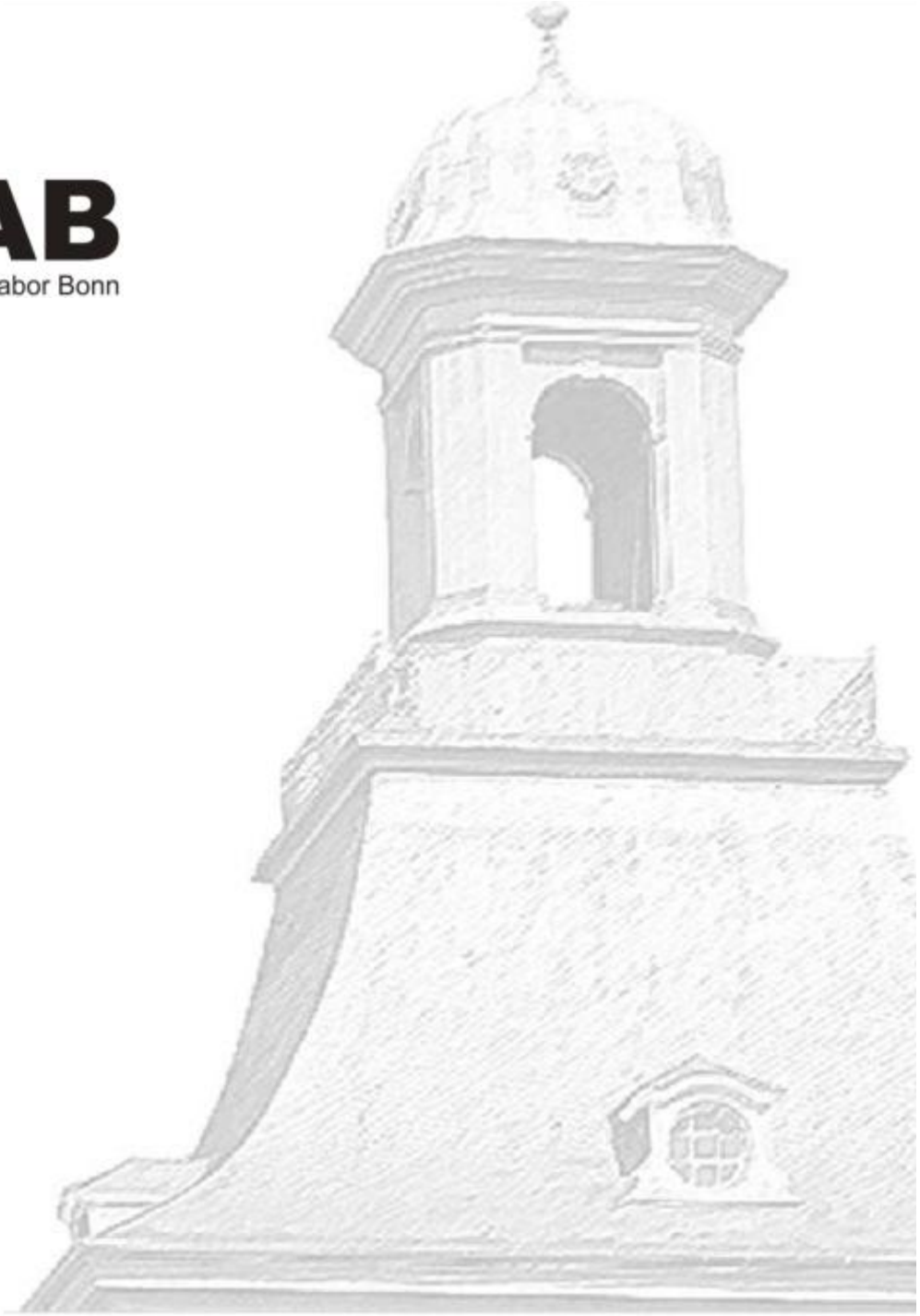
  → Core works if deserializer clock (e.g. 320MHz) is used

  BUT
- Test environment was not used for long time → Debugging
- First test cycles show promising results
- Transition from manually tested to automatic test system (UART interface)


UART
I/O [7:0]
O [7:0]
O [7:0]
DCD emulator
dcd_mem_out
dcd_mem_in
sw_mem_in
JTAG
Do[255:0]
Di[63:0]
SW[15:0]
SER
DES
DES
Do[63:0]
Di[15:0]
SW[3:0]
DHPT 1.0

universitätbonn

SI LAB
Silizium Labor Bonn



Thank you

germic@physik.uni-bonn.de