DHH news

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and applications**
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New software version
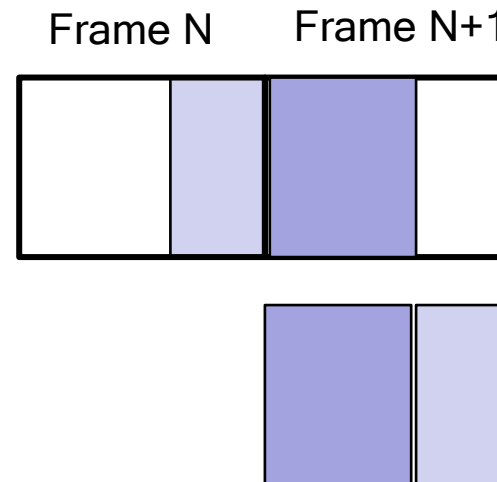
New version of DHH software:

- o removed redundant code
- o Object oriented style instead of procedural
  - o Class for every ASIC, register, bit field
  - o New register added by defining bit-fields, address and length
- o Old part of bit stream generation
  - o Bug in data decoding
  - o DCD configuration problem on certain setups
    - o Bit stream length varies
  - o No support for boundary scan, requires access to two ASICs at the same time
    - o Alternative - commercial software

New ASICs integration

- o DCD pipeline has been integrated
- o DHPT still to be integrated

Firmware development

- ## Handling overlapping events with ΔT < 20us
  - Position of trigger within frame memorized and used to define event boundaries
  - Simulated with DHP data generator
  - To be tested with DHP

- ## Data reordering and remapping (clustering preprocessing)
  - Simulated
  - To be tested with DHP

Frame N   Frame N+1

- Before Easter, an introduction to the DHH software was given to Chaouki Boulahouache
- Successfully installed the software and established data link to the DHH
- Modification and testing of the AMC module for operation with the TLU will be done before sending the module to Tabuk

Dima and Chaouki after successfully established communication between DHH and a virtual machine on a laptop at HLL

DHH power supply problem

Problem:

- – Unstable JTAG for FPGA programming
- – Works more or less fine @5V
- – Does not work at all @12V

Reason :

- - Induced current by DC/DC converter on TDI and TCLK lines

Solution for existing modules:

- –   100 pF capacitor to GND on TDI and TCLK lines

Solution for mass production:

- – Changing layout to avoid cross talks

DHH production

Done
- Layout finalized
- MMC integrated in DHH

Still to be done
- Current source test to be done by Felix
- Problem with high speed link of DHP02 which loses Aurora link synchronization

Carrier card production moved to summer 2014