Depfet Movie Chip

design status and schedule

16th International Workshop on DEPFET Detectors and Applications

25.-28.05.2014 Kloster Seeon

Requirements from the detector

- DH1k:
  - 512x512 sub detector
  - Double folded readout (2x128, single side)
  - 1k frame rate, 8-10bit ADC
- DH80k:
  - 512x512 pixel sub detector
  - four folded readout (4x64, double side)
  - 80k frame rate, 8 bit adc
  - peak data rate of 10Gbit/s out of DCD

    local mem for 256x64x100 8bit, slow readout after 100 frames captured

Design constraints

- digital interfaces as reference from:
  - DCD-Bv2
  - SwitcherB18 v2.0
- Design focus on DH80k, at the end possible modification for DH1k use
- Choice of technology:
  - Which technology is able to implement the memory under the area constraints (256x100x64*8bit)?
  - With TSMC40 0,5µm^2 per SRAM bit (area without dec,buf,..)
    approx 7mm^2 for the memory (3*2.3mm)

Interface to dcd/switcher

- 8x8bit x32 dcd2movie time mux bus
- 8x2bit x32 movie2dcd time mux bus for pedestals (opt. In case of dcd internal mem)
- conf and debug via jtag
- switcher seq (SwitcherB)
- DCD Clk 320MHz and Sync_Reset

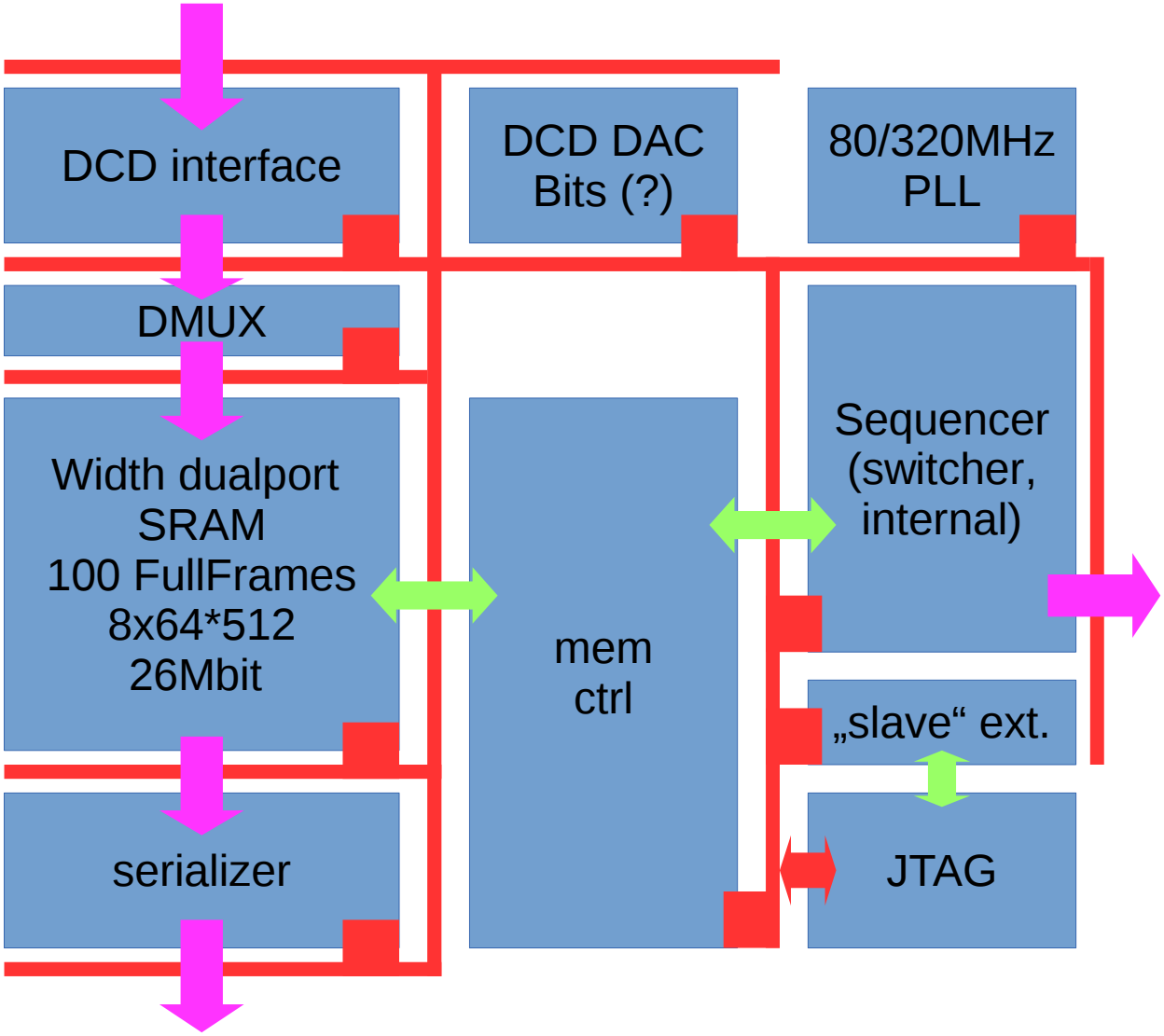
interface to daq

- max 6x LVDS DAQ downstream (2x needed for DH80k spec.)
- JTAG for slow control
- signals from/to sequenzer
  - FrameStart
  - Veto
  - StartReadout

parts

- 80MHz 4x analog PLL (320MHz out) for dcd (pipelined?) ✓
- JTAG core with external „slave“ chains ✓
- DCD interface (data „descramble“) (pipelined?) ✓
- Commercial dual port sram block (1024x80@400MHz)
- programmable Sequenzer (Switcher, internal operation) ✓
  - Window mode
    - Loop seq: 1x Fullframe and x Smallframes

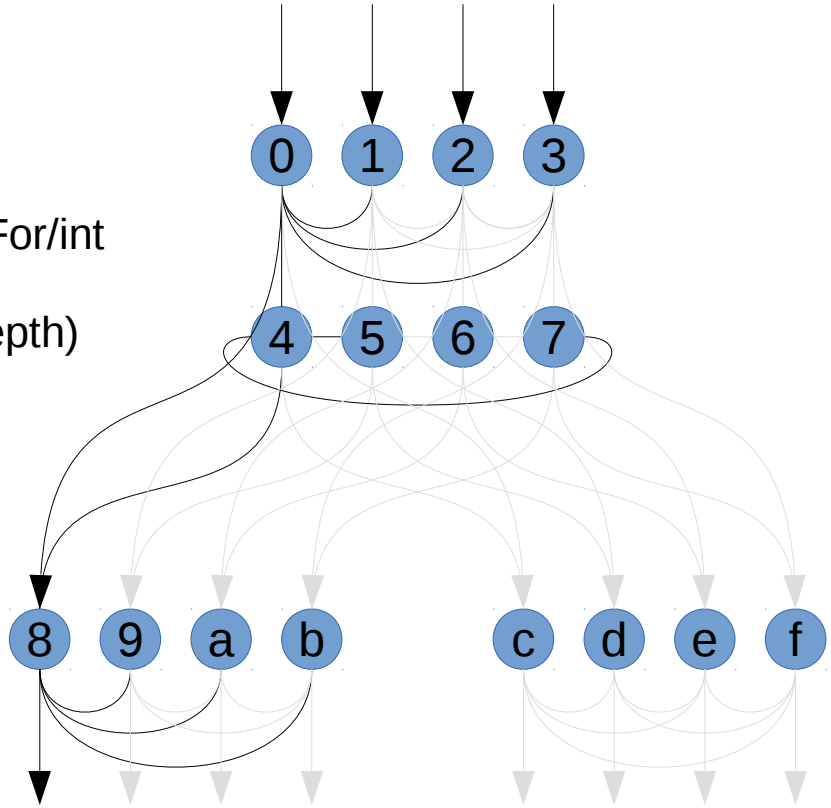
DMC internal



switcher sequencer

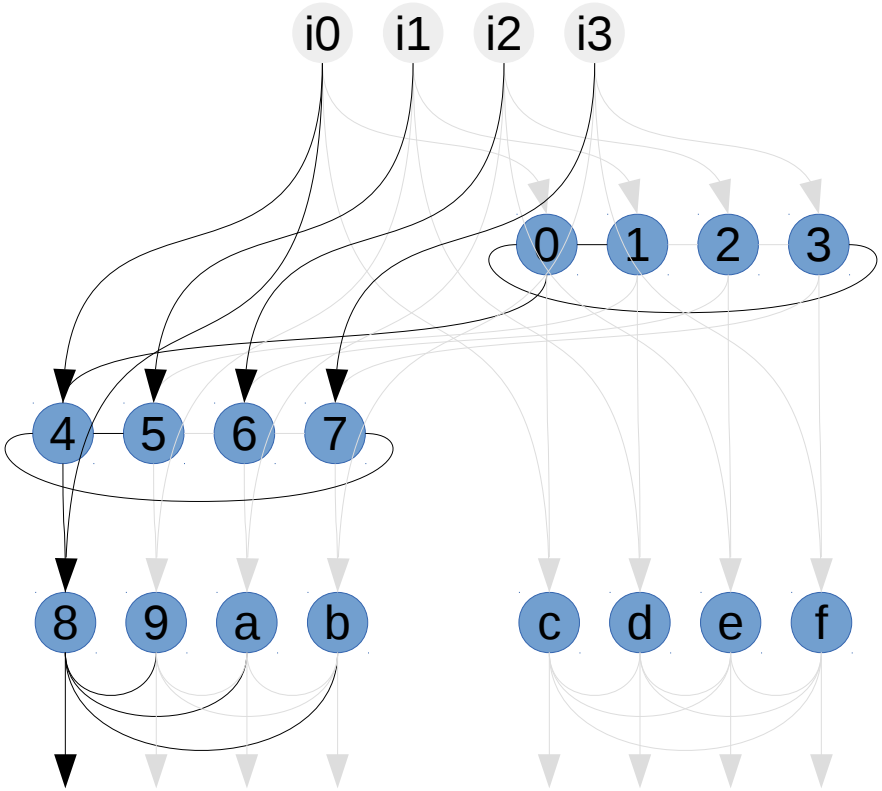
- deep and width memory array vs. loosely coupled stat machines
  - waste of memory bits for static signals in long seq.
  - Unflexible for „independent“ sequences

  - one node for each each output signal (internal/external)
  - each node has 2 loop counter, 5 waitFor/int maskable inputs
    stack with depth for 4 reg sets (call depth)
    simple instruction set



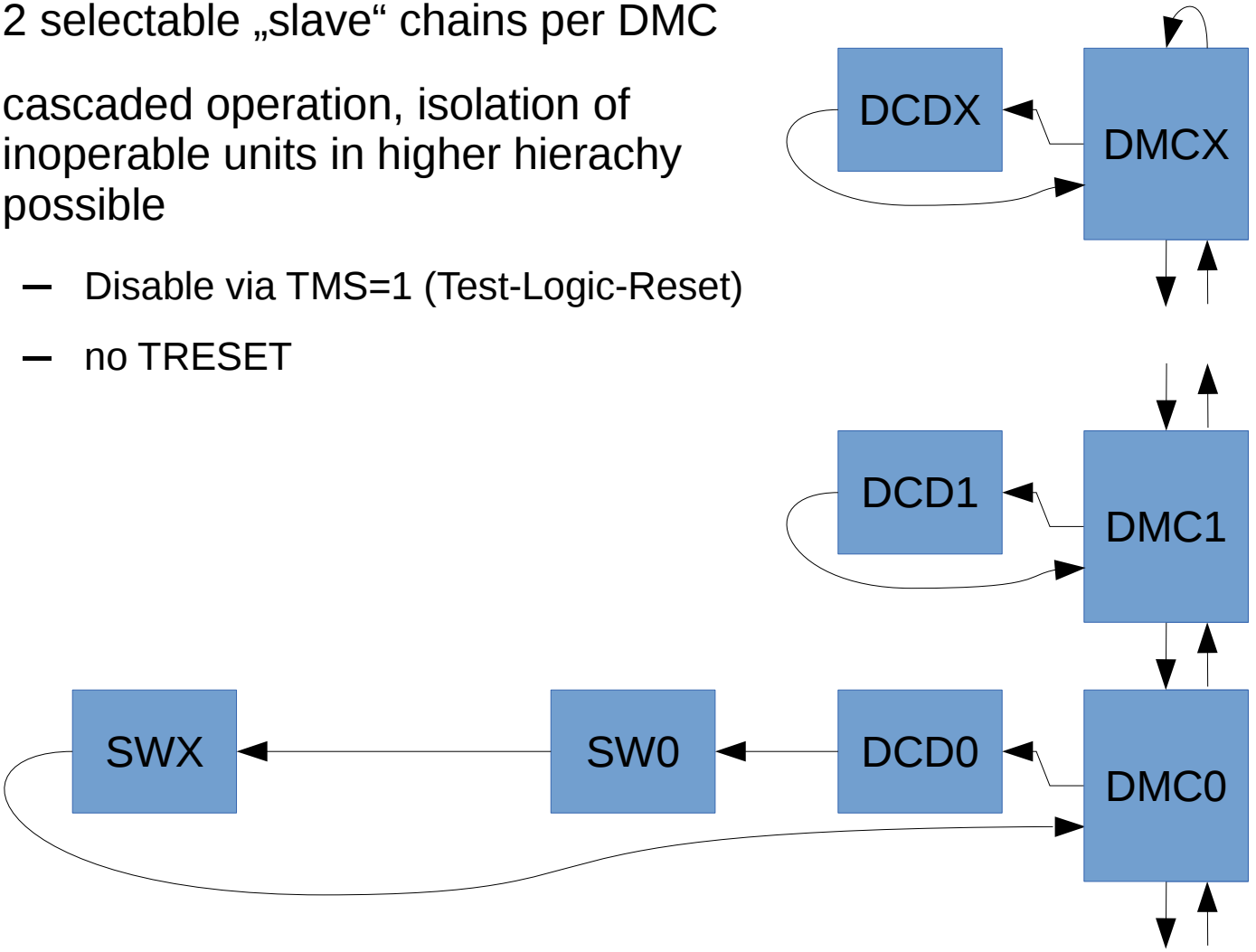
switcher sequencer (cont.)

- alternative sequencer interconnection
- backup via direct mode to drive the outputs
- selectable via JTAG configuration



JTAG „slave“ chains

- 2 selectable „slave“ chains per DMC
- cascaded operation, isolation of inoperable units in higher hierachy possible
  - Disable via TMS=1 (Test-Logic-Reset)
  - no TRESET



Whats next ?

- Verification of the dcd interface with an dcd+dcdro via FPGA emulation
  - COB PCB for IgelLight DDR3B slot
    - Which voltages are needed to drive at least the digital parts of the dcd ?
    - dcd+dcdro hybrid available ?
- Test of Switcher interface
  - max value of sclk frequency for switcher ?

DMC timeline 20140526

- with start of chip assembly from the current design point (without hardware verification to DCDB/RO and SwitcherB)
  - miniasic prototype (tapeout deadline 10.09.2014, two per year) with reduced (<half) interface to dcd, limited (~10) framebuffer, wirebond, 1,8^2mm^2 (20K€)
    - 2 months fabrication time
    - End 2014 prototype setup for testing ready
  - DMC full chip tapeout (May-Jun 2015, one per month)
    - 2-3 months fabrication time (bumps)

Use of DMC for the DH1K option

- DCDB v2: rotation of the data bit vector by 90° (change from byte parallel to bit serial transmission for the different channels) via JTAG config bit
- 5x LVDS + 1 spare for downstream
- DCD clk frequency?

Thank you

DCDEMC or DCD+DMC ?

- reduced amount of bump bonded asic's 12/16 (25%)
  - reduced area, costs (~1k/asic), less interconnects
- possible crosstalk from driver power domain to adc and frontend
  - reason for dcd+ro, weak driver in present dcd
- external steering of the switchers needed (cabling/connectors/firmware for IgelLight/Seq)

- identical interface for DH1K and DH80K on the detector
  - less work on firmware (reuse/sharing of components)
- needs a DMC already at the DH1K assembly mile stone

(pro are also the cons of the opposite option)