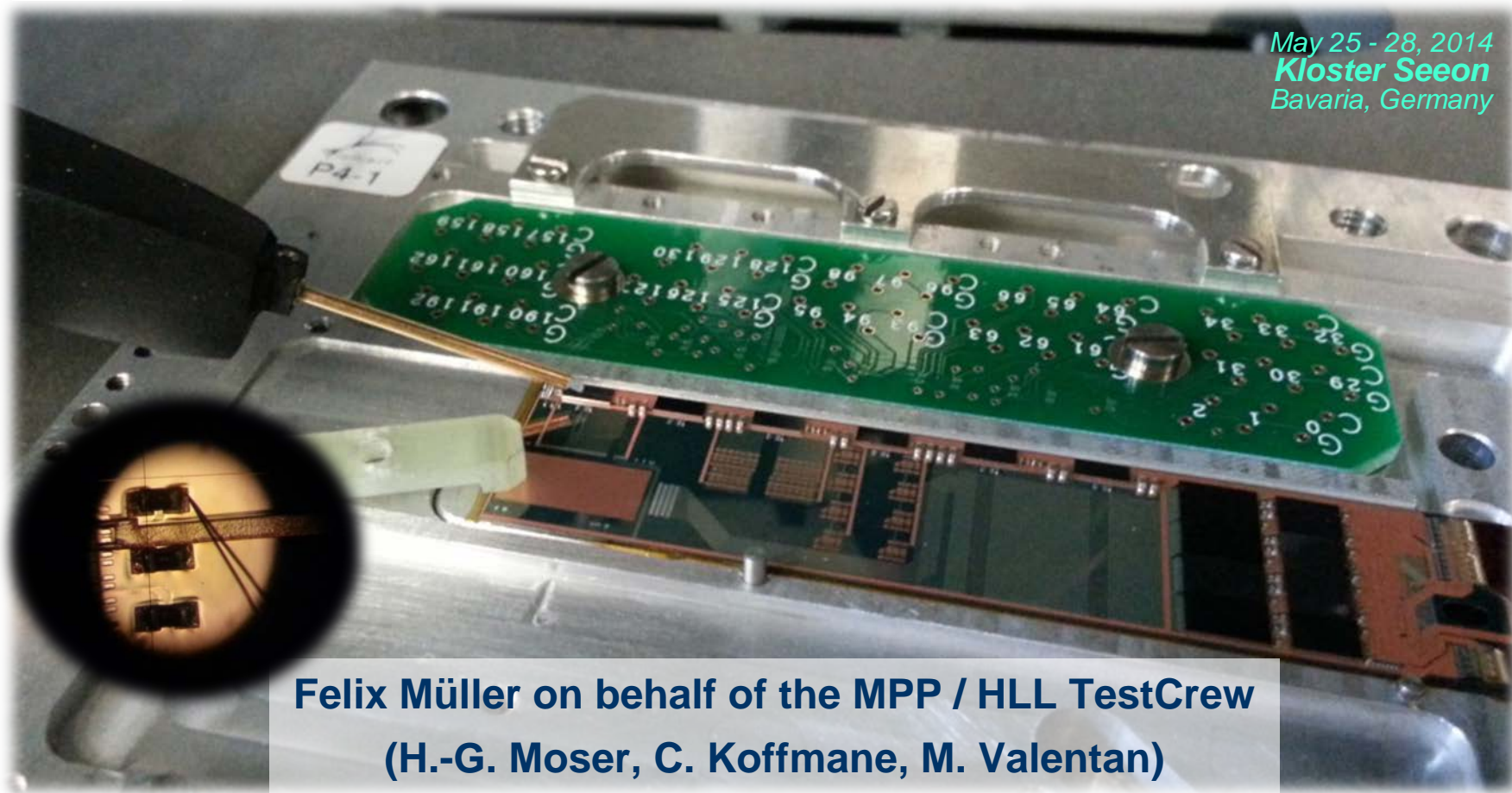


DEPFET



# Electrical Test of EMCM

May 25 - 28, 2014  
Kloster Seeon  
Bavaria, Germany



Felix Müller on behalf of the MPP / HLL TestCrew  
(H.-G. Moser, C. Koffmane, M. Valentan)

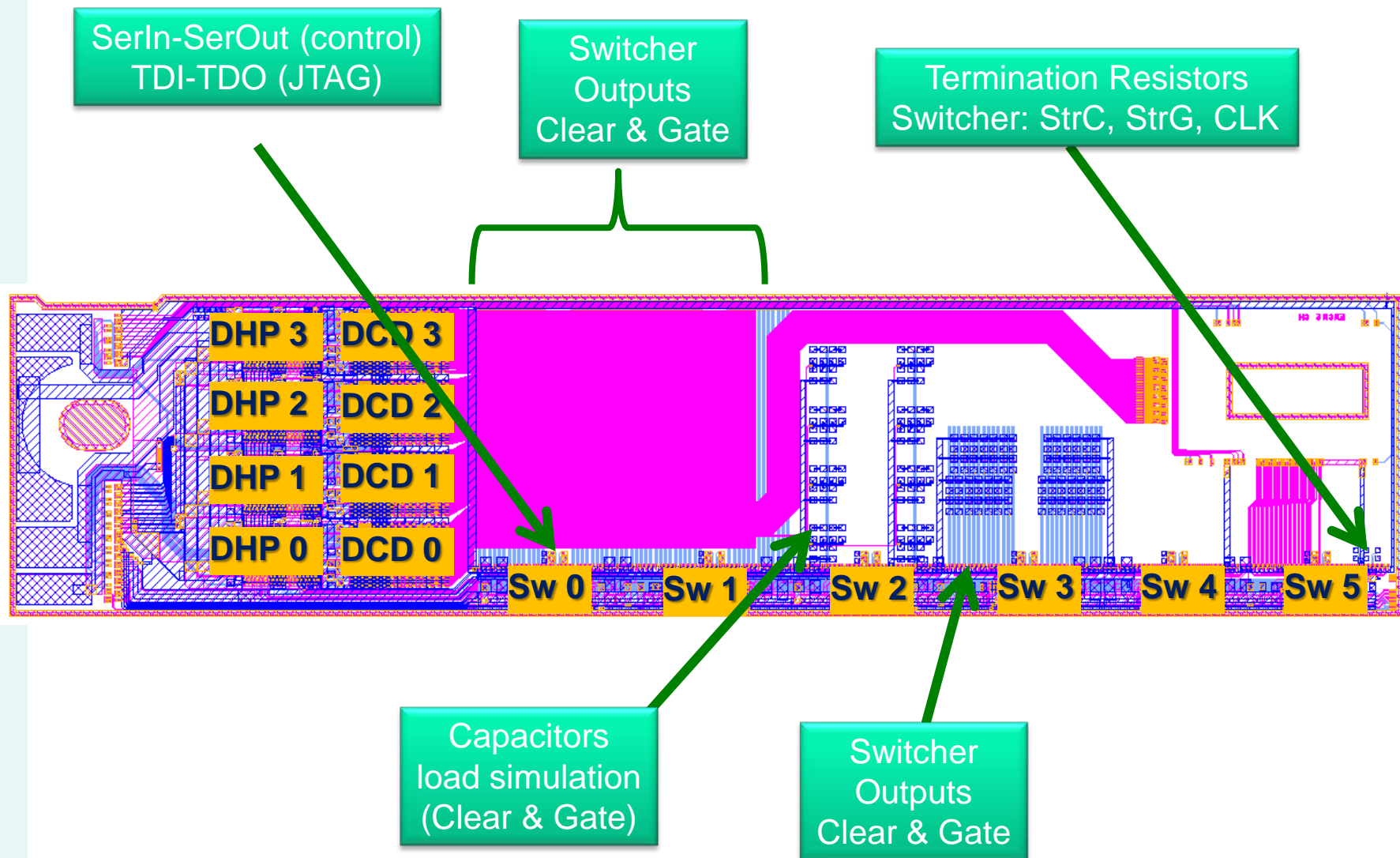
1. Overview of EMCs
2. Nomenclature
3. Setup
4. EMC (fully populated one)
5. DCD ADC characterization
6. Latest Test Devices
7. Drawbacks
8. Conclusion and Outlook

# Overview of EMCMs

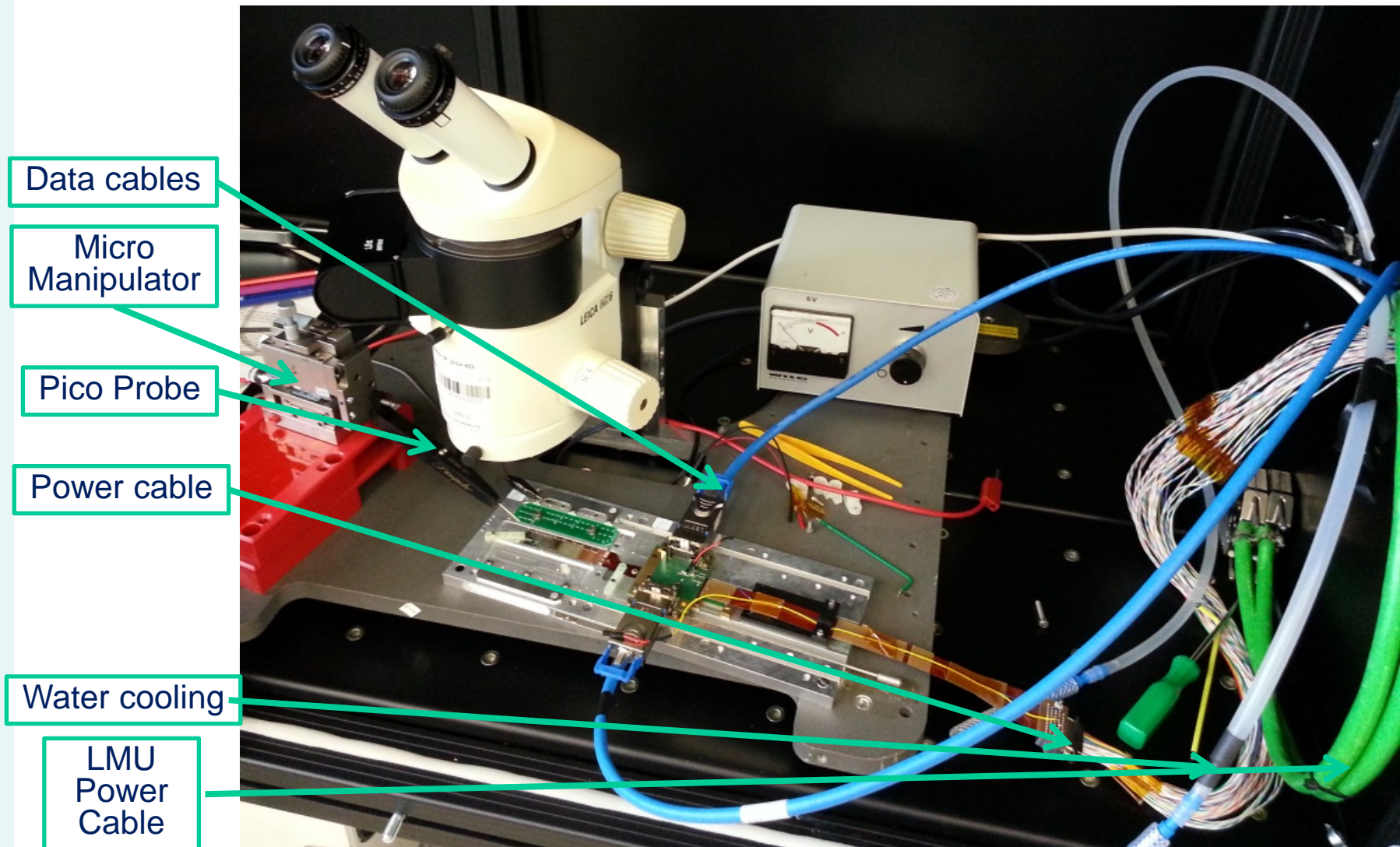
ID	Project	DHP 0.2	DCD Bv2	Sw B18v1	Location	Comment / Status
P4-1	ZMI5	4	4	6	MUC	Fully populated
P6-1	EMCM_1	1	1	1	MUC	
P6-2	EMCM_2	1	1	1	BN→MUC	
W2-4		1	1	1	MUC	Matrix glued (DESY)
W9-1	EMCM_2-2	1	1	6	MUC	Short of term. resistors
W9-2	EMCM_2-2	1	1	6	MUC	Short of capacitors
...	EMCM_3-2					
...	EMCM_3-2					
...	EMCM_3-2					
...	EMCM_3-2					
...	EMCM_3-2					

many more

# Overview of EMCM - Nomenclature



# Measurement Setup @ Semiconductor Laboratory



Data cables

Micro Manipulator

Pico Probe

Power cable

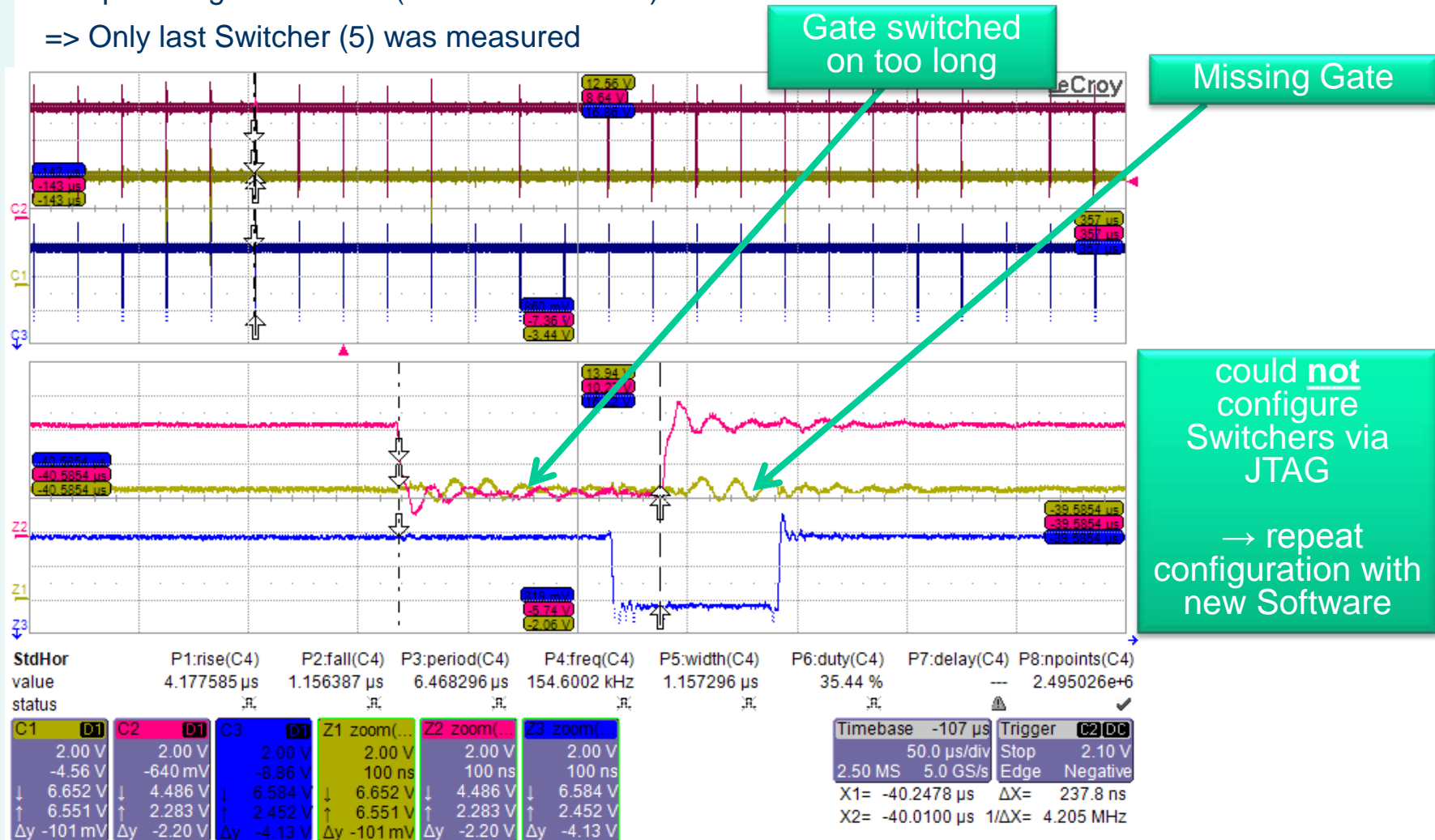
Water cooling

LMU Power Cable

# EMCM P4-1 -- Switcher

Switcher: Output signals; falling edge of the gate signal is much too slow after problems with the powering of the SWB (bond wires melted)

=> Only last Switcher (5) was measured



timing problems

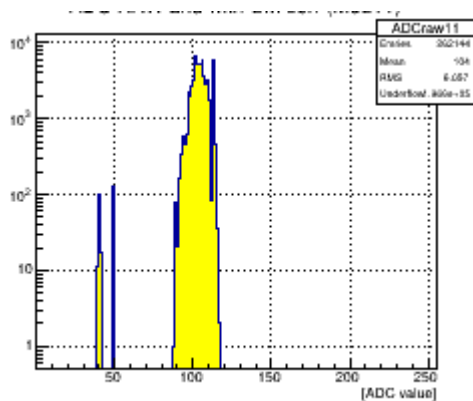
# EMCM P4-1 -- DCDs

DCD0 and DCD3 seem to work

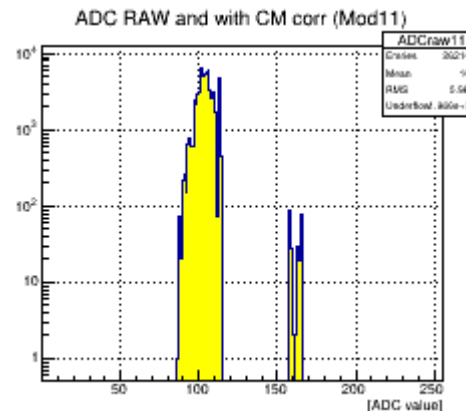
DCD1 does not react on changes VNSubIn (0-127), maybe trans-impedance amplifier is damaged

In addition, only if EnMonIn is off, one can see a test current 'peak'. One can see a double structure => is it an artifact of odd and even ADCs ? (has to be further investigated)

DCD2: Auroralink crashes when one tries to read a "full frame" from DHP2. Moreover, all Auroralinks (DHP0,1,2,3) break.

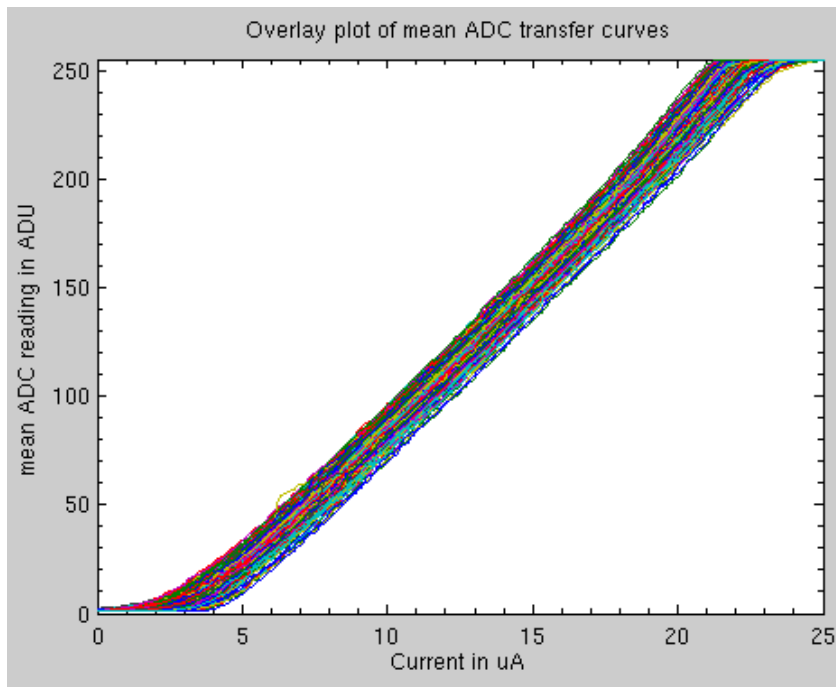


DCD0,  
EnMonIn off,  
VNSubIn 2, VNSubOut 10,  
SMU: 4uA, 1.8V,  
ADC-channel 128



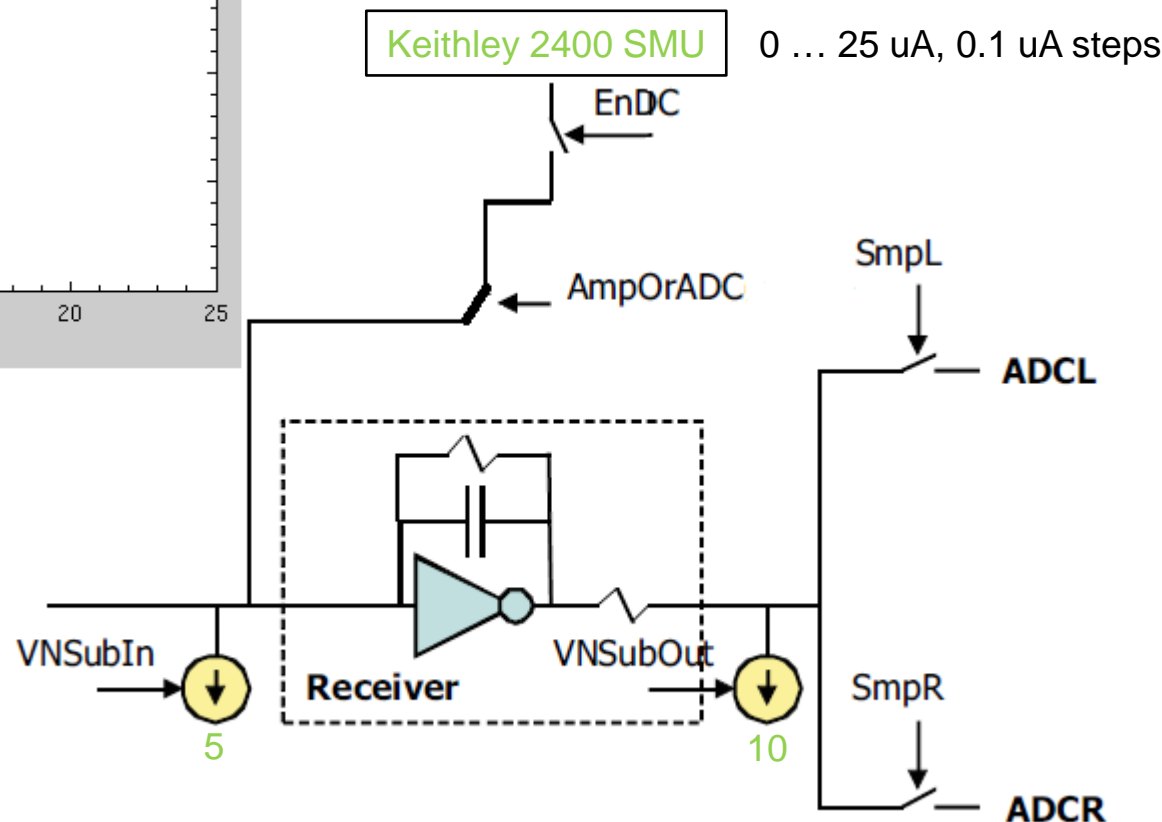
DCD0,  
EnMonIn on,  
VNSubIn 2, VNSubOut 10,  
SMU: 4uA, 1.8V,  
ADC-channel 128

# EMCM P4-1 -- DCDs



Setup is prepared for automatic characterization of ADC transfer curves: still needs couple of hours

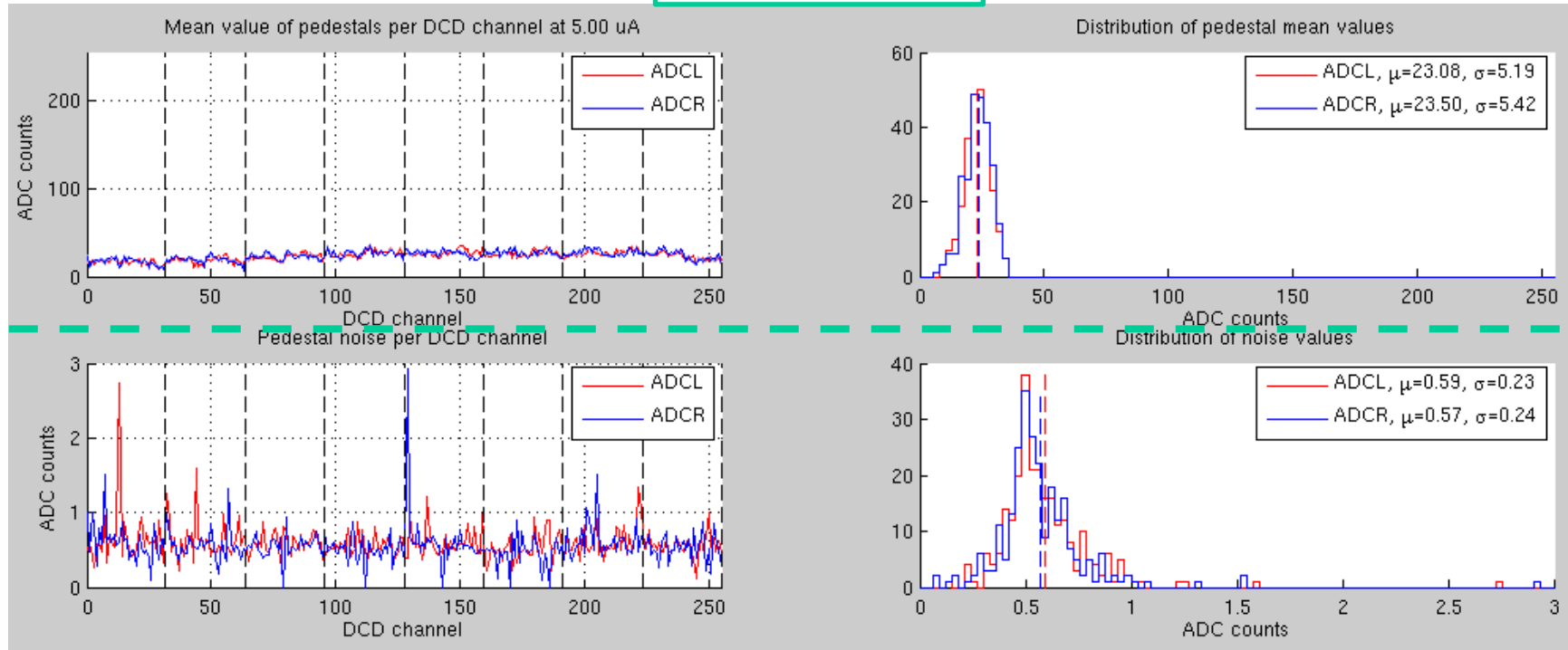
scan was done with 250MHz



# DCD Characterization - Noise

128 Measurements of each ADC

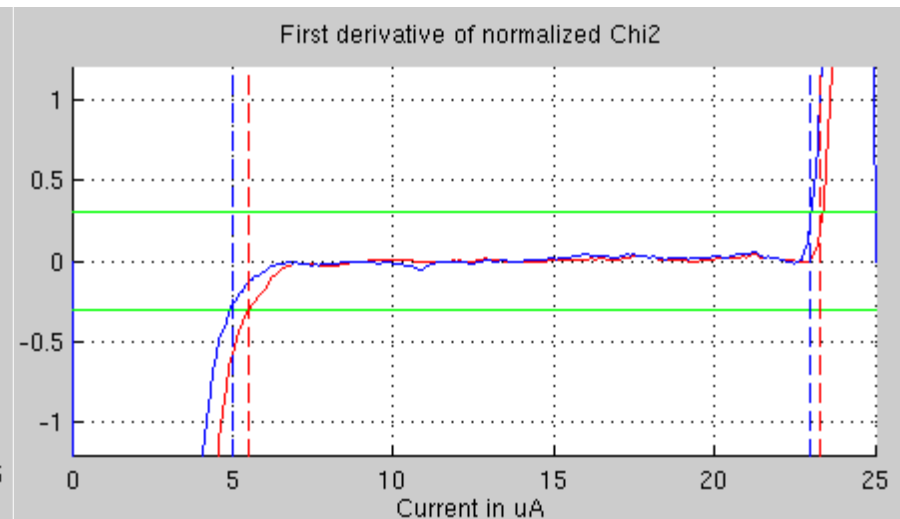
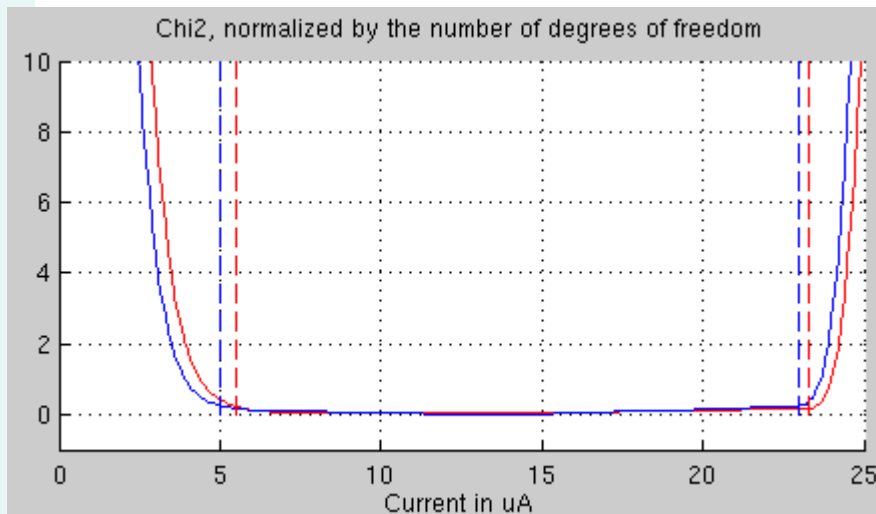
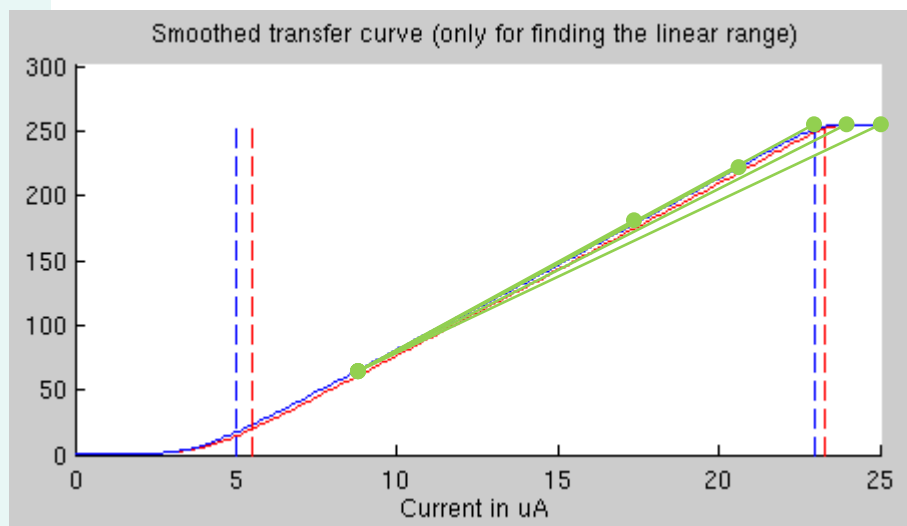
## Pedestals Mean

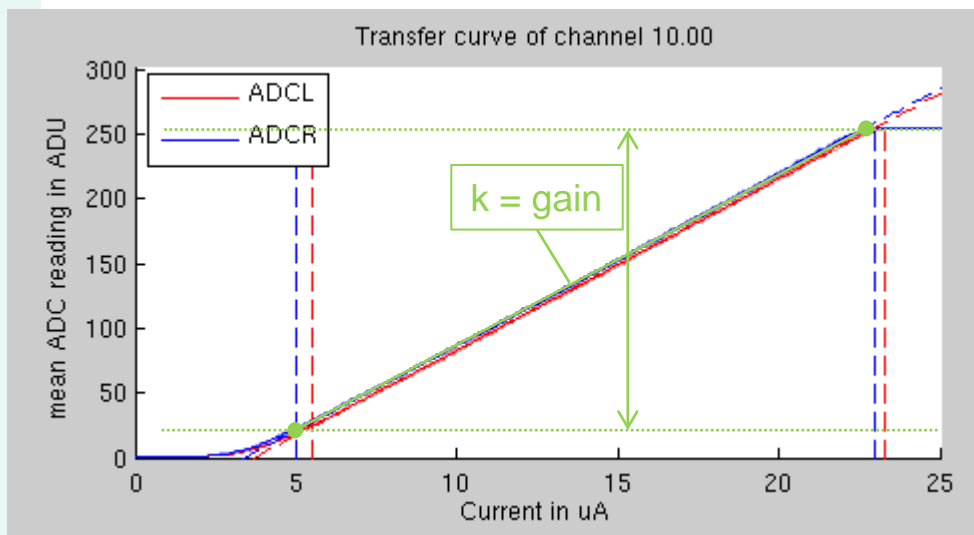


## Pedestals Noise

# DCD ch. - Detailed analysis: Finding the linear region

- 1) Smoothen the curve: each point is the average of 10 adjacent points
- 2) Linear fit to upper part of the curve, repeat as function of upper limit. Calculate sum of square deviation ( $\chi^2$ ), divide by number of degrees of freedom (= #points - 2 fit param).
- 3) Same for lower part of the curve
- 4) Calculate gradient, arbitrarily define linear region as “gradient < 0.3”



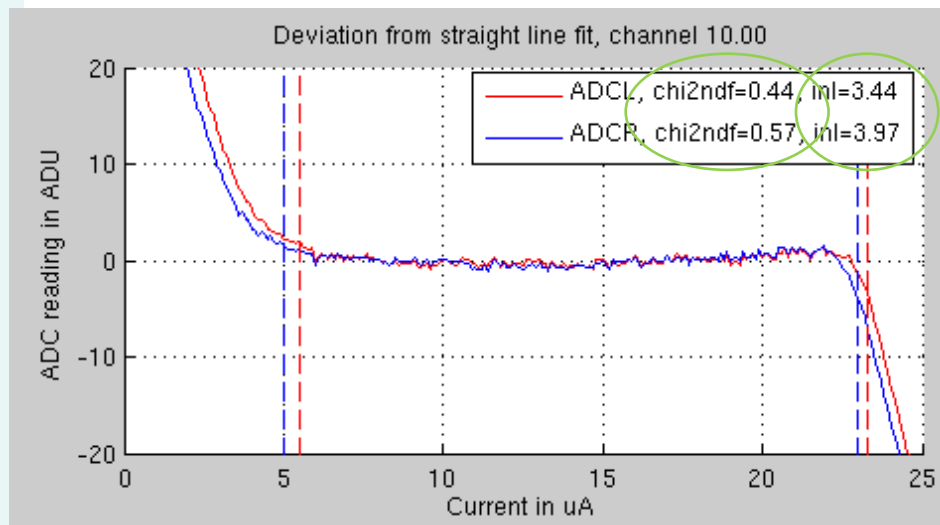


From transfer curve:

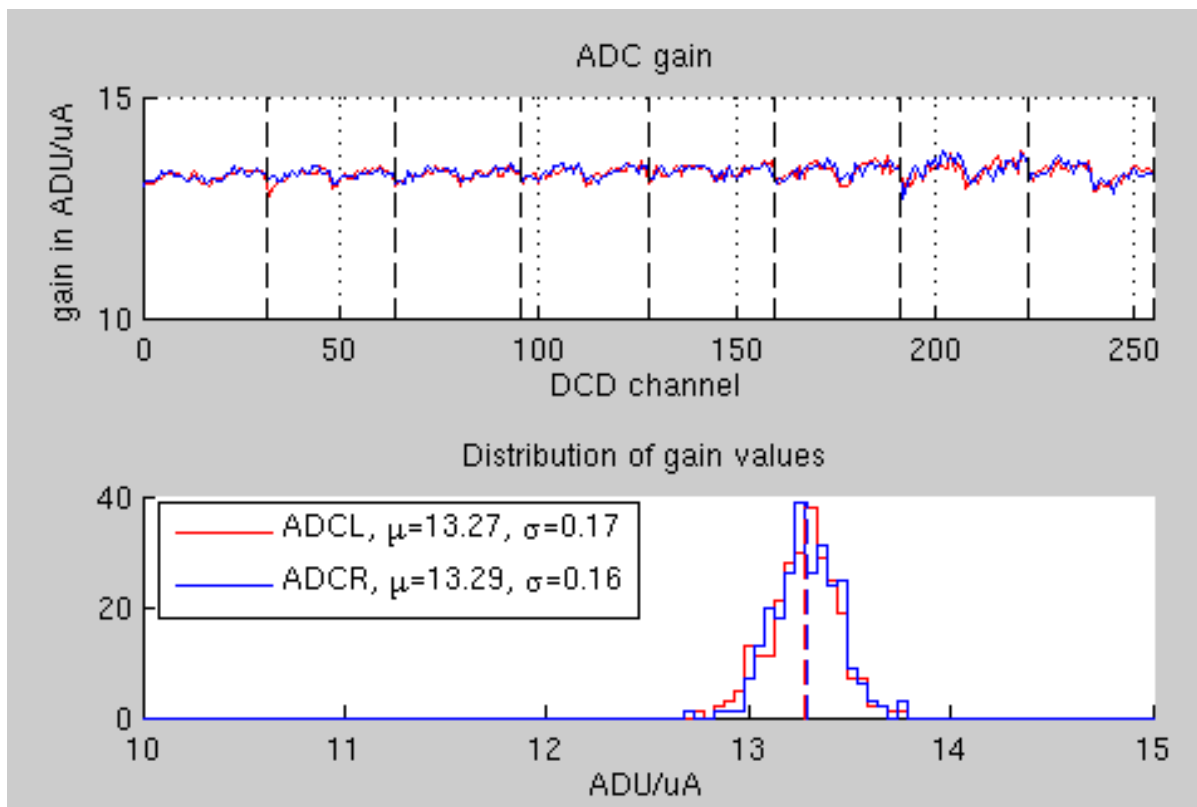
- 1) Gain: Fit to linear range, find inclination
- 2) Linear region in ADUs

From deviation from fit line:

- 3) Integral nonlinearity: maximum deviation from fit line (within the linear region)
- 4) Sum of square deviation from fitline, normalized by the number of degrees of freedom (within the linear region)



# DCD characterization - Results



periodic structure w.r.t. half columns

## P6-1 (1x Switcher, 1x DCD, 1x DHP):

- Switcher: output signals don't toggle after accident during probing (bond wires touching)
- DHP & DCD ok
- DCD has not been characterized

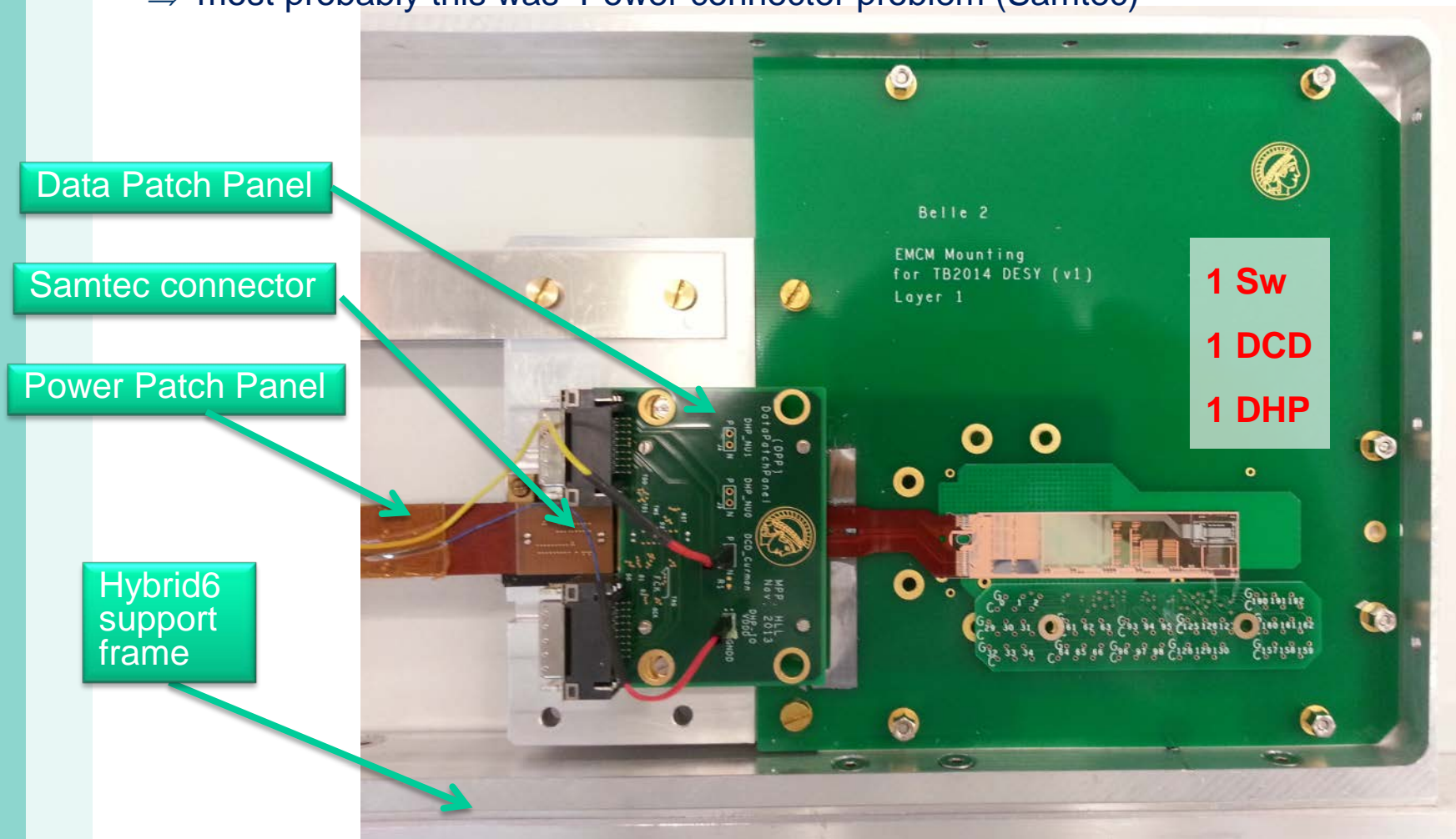
## P6-2:

- Clear to Source short → not suited for PXD6 matrix
- SWB, DHP and DCD ok
- Item was located at Bonn ⇒ is currently sent to Munich
- Switcher outputs have to be measured again (⇒ Rework - slide 17)

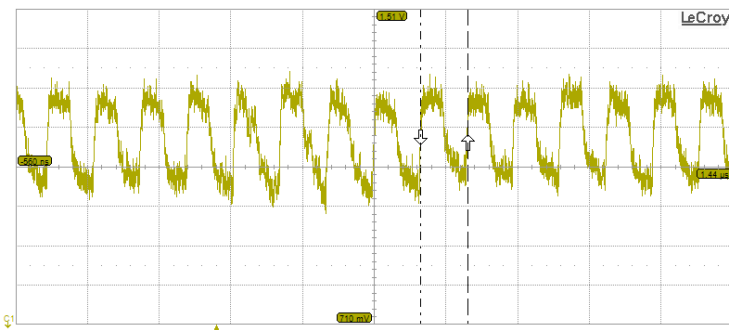
# EMCM W2-4

Backup solution for Beam Test in January

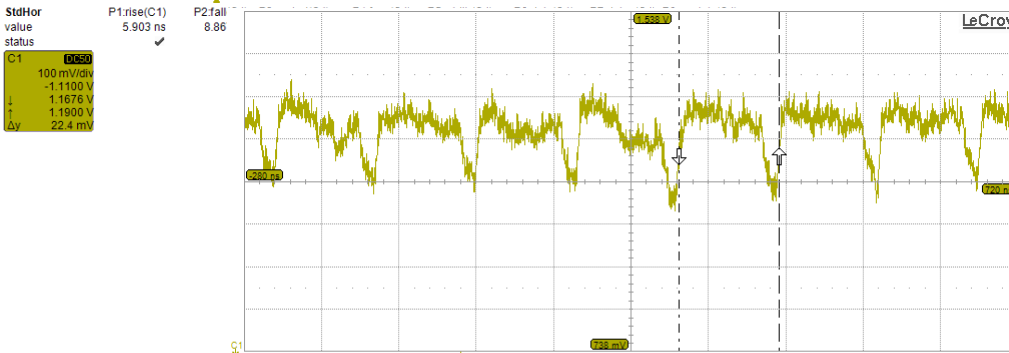
- ⇒ was brought untested to DESY (due to missing test devices in MUC)
- ⇒ showed strange voltages & currents (Clear, Gate)
- ⇒ most probably this was Power connector problem (Samtec)



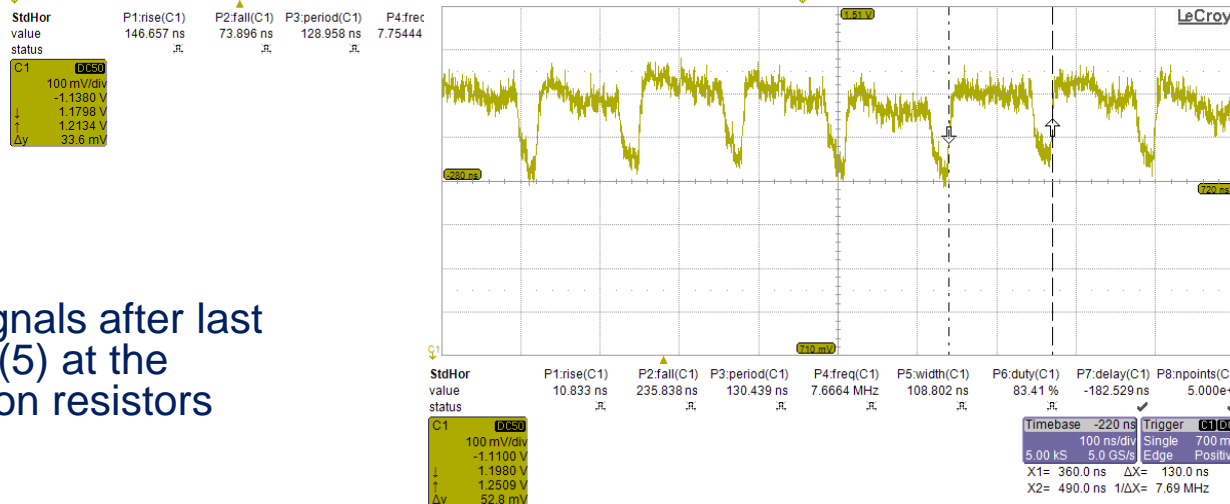
# EMCM W2-4 -- Switcher



Clock  
~130 ns



Strobe Clear  
~130 ns



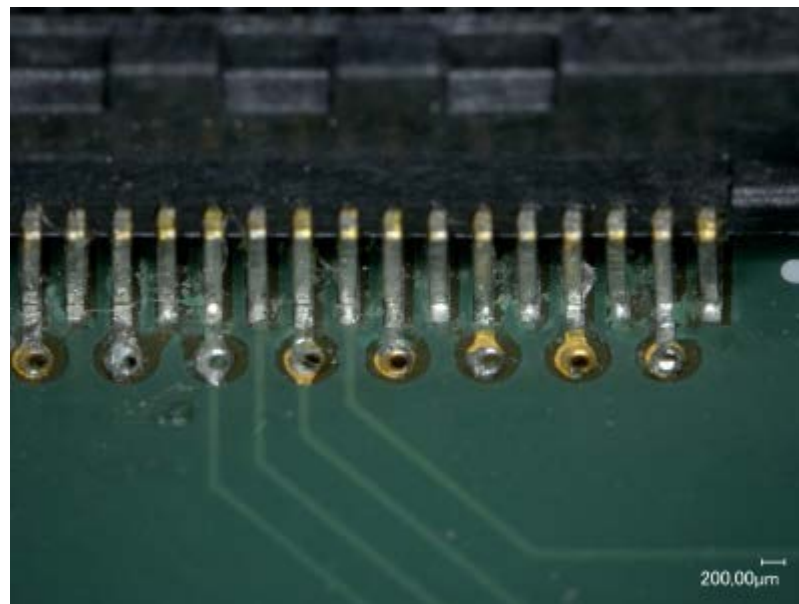
Strobe Gate  
~130 ns

Probe signals after last  
switcher (5) at the  
termination resistors

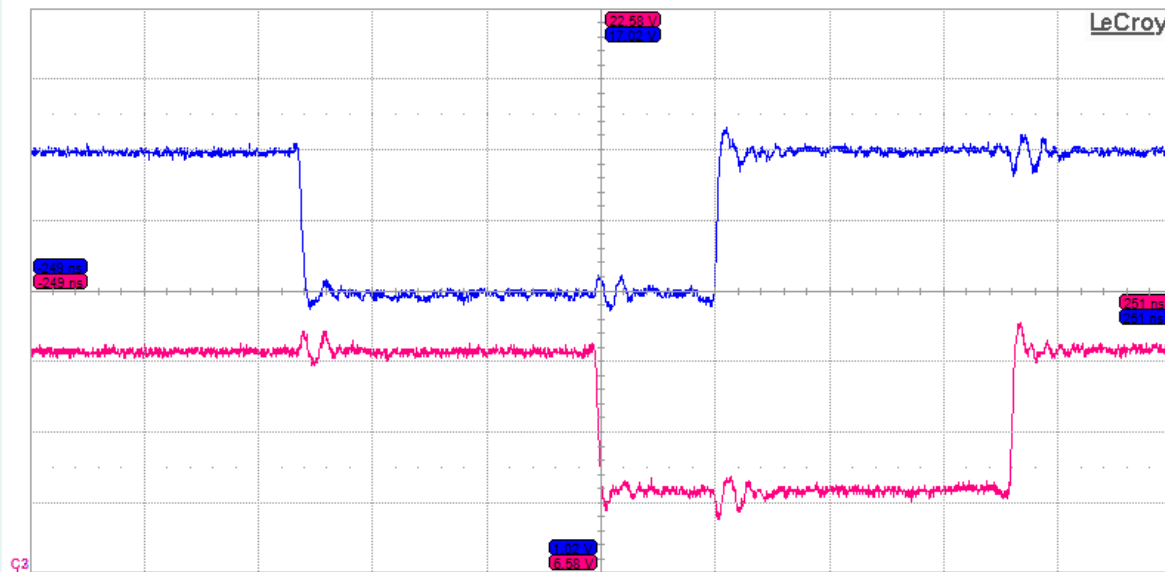
# EMCM W2-4 – Power Patch Panel

SWB: output signals don't toggle, Clear channels are stuck to ClearOn potential

⇒ Repair of Samtec Power Connector

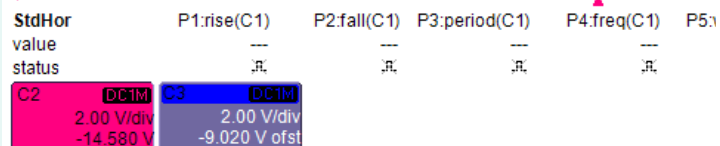


# EMCM W2-4 -- Switcher

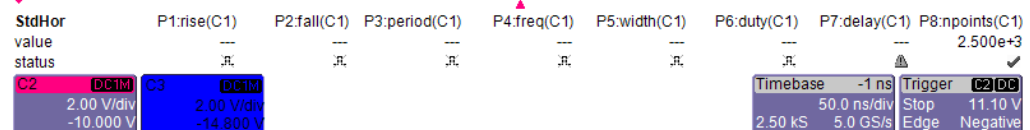
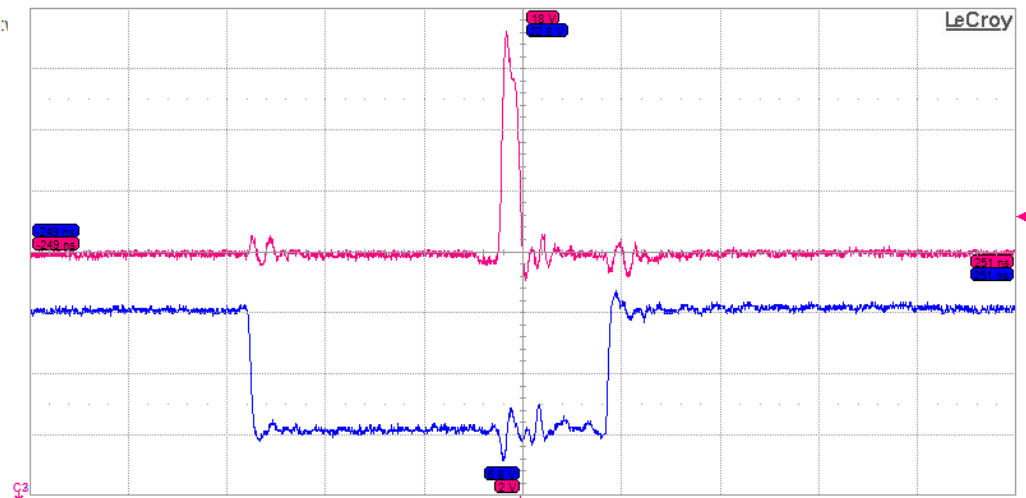


row 190 - Gate

only 1 Switcher (5)  
assembled



row 190 - Clear  
row 190 - Gate



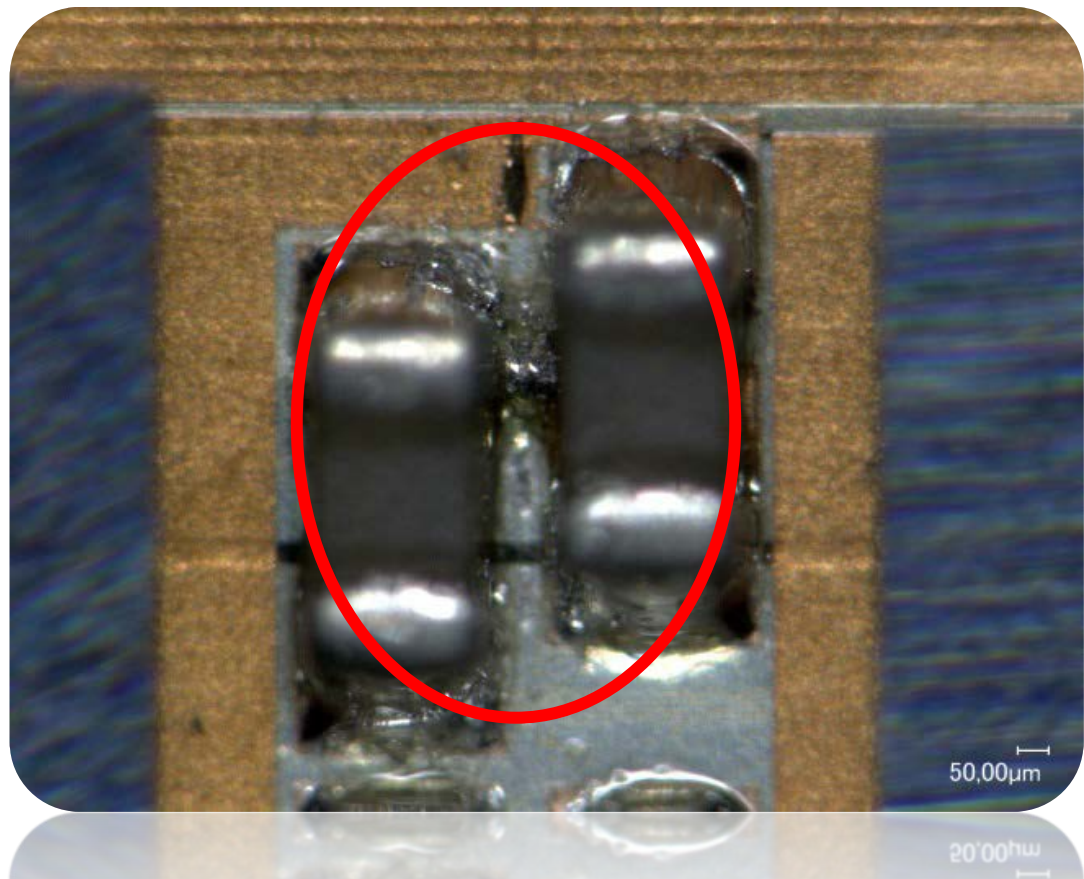
## Shorts of Termination Resistors of LVDS Switcher Signals

=> does not work



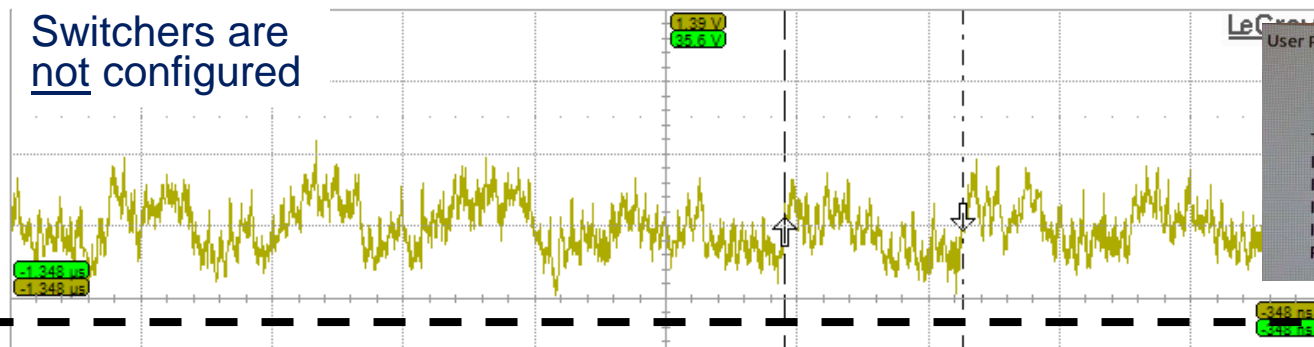
DCD: RefIn is shorted to GNDA

=> not suited for matrix since DCD cannot work properly



# EMCM W9-2 – Switcher Clock

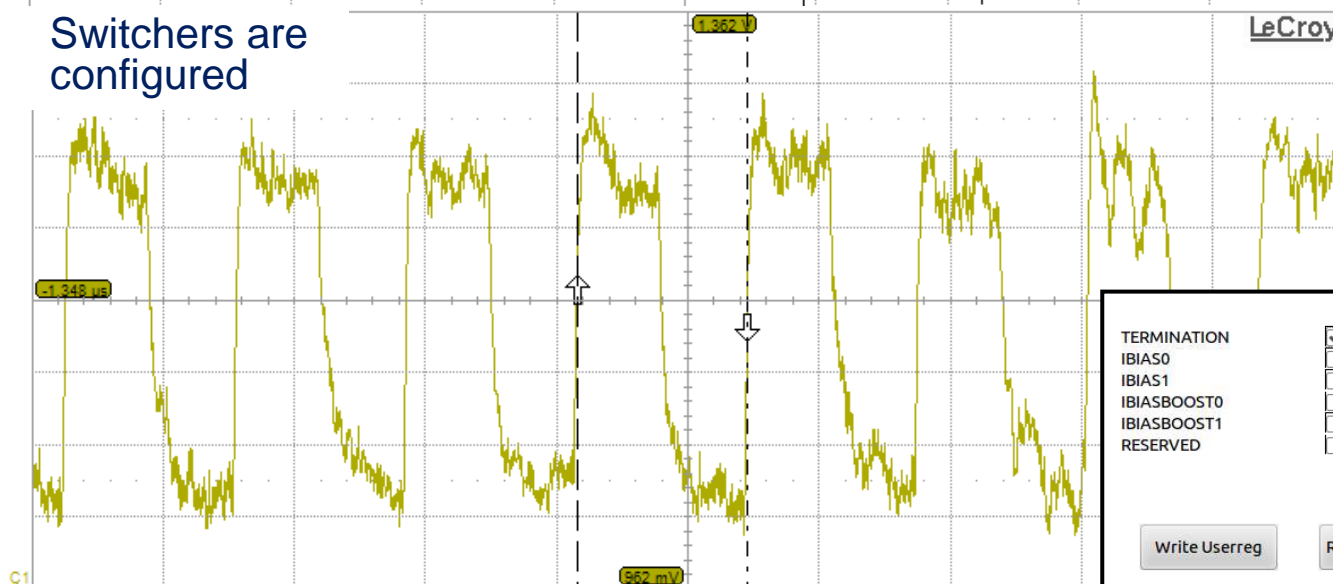
Switchers are not configured



User Register Extest Sample/Preload switcher0

TERMINATION	
IBIAS0	<input type="checkbox"/>
IBIAS1	<input type="checkbox"/>
IBIASBOOST0	<input type="checkbox"/>
IBIASBOOST1	<input type="checkbox"/>
RESERVED	<input type="checkbox"/>

Switchers are configured



TERMINATION

IBIAS0	<input checked="" type="checkbox"/>
IBIAS1	<input type="checkbox"/>
IBIASBOOST0	<input type="checkbox"/>
IBIASBOOST1	<input type="checkbox"/>
RESERVED	<input type="checkbox"/>

IDCODE 0x23456789

Read IDCODE

Write Userreg Read Userreg

StdVer	P1:pkpk(C1)	P2:ampl(C1)	P3:max(C1)	P4:min(C1)	P5:sdev(C1)	P6:mean(C1)	P7:base(C1)	P8:top(C1)
value	322 mV	211.2 mV	1.320 V	999 mV	100.9 mV	1.1521 V	1.0362 V	1.2474 V
status	✓	✓	✓	✓	✓	✓	✓	✓

C1	DC50
50.0 mV/div	
-1.1620 V	
1.1341 V	
1.1784 V	
Δy	44.2 mV

Timebase	848 ns
100 ns/div	
5.00 kS	5.0 GS/s
X1= -803.0 ns	ΔX= -129.4 ns
X2= -932.4 ns	1/ΔX= -7.73 MHz

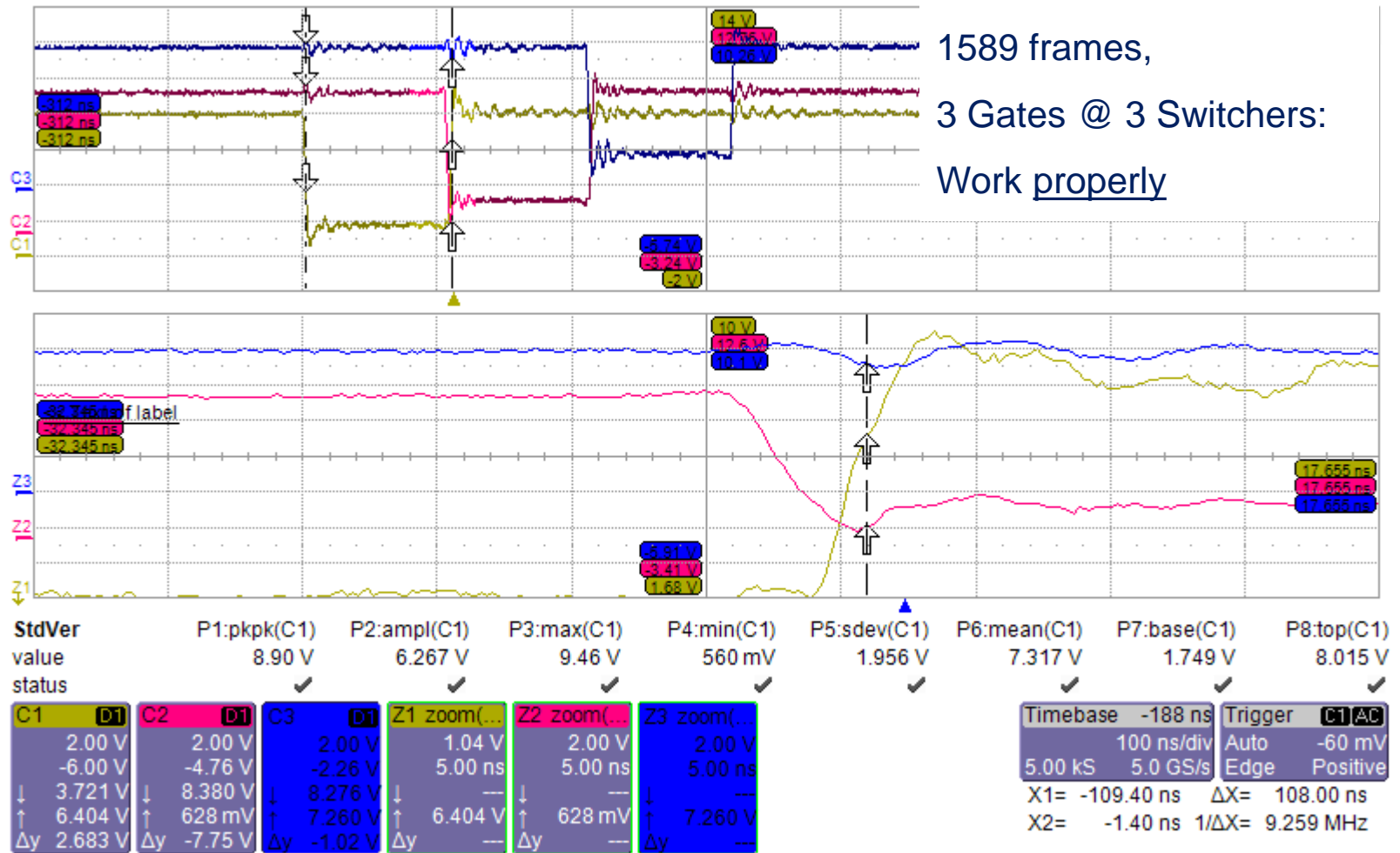
  

Trigger	C1 AC
Stop	205.0 mV
Edge	Negative

# EMCM W9-2 - Switchers

Switcher 6: Output of 3 consecutive Gates (190, 191, 192)

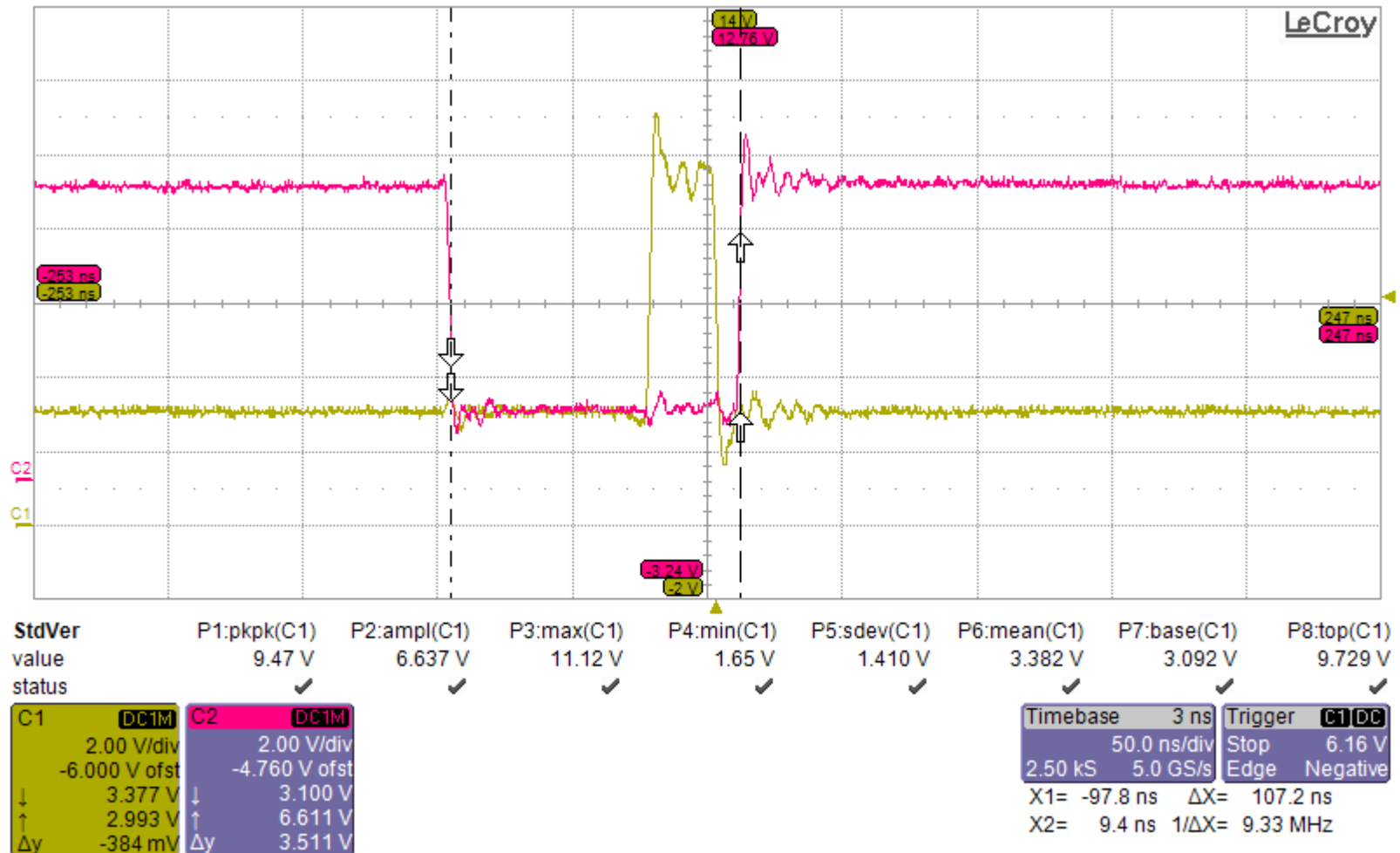
305MHz



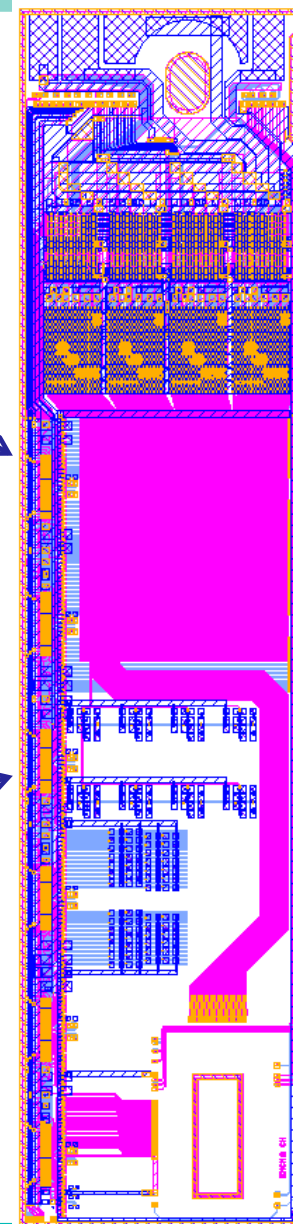
# EMCM W9-2 - Switchers

Switcher 6: Output of Gates & Clear, Channel 191

305MHz



# EMCM W9-2 – Switchers 1-3



# Software (JTAG)

DCD Settings and Switcher (Termination Resistors) are configured via JTAG

→ is **required** !

Software for 4 DCDs/DHPs and 6 Switchers is different compared to

Software for 1 DCD/DHP and 1 Switcher

(Bitarray, Bitstream, Dummy Bits)

not fully understood (Assembly problem?, DCD problem?)

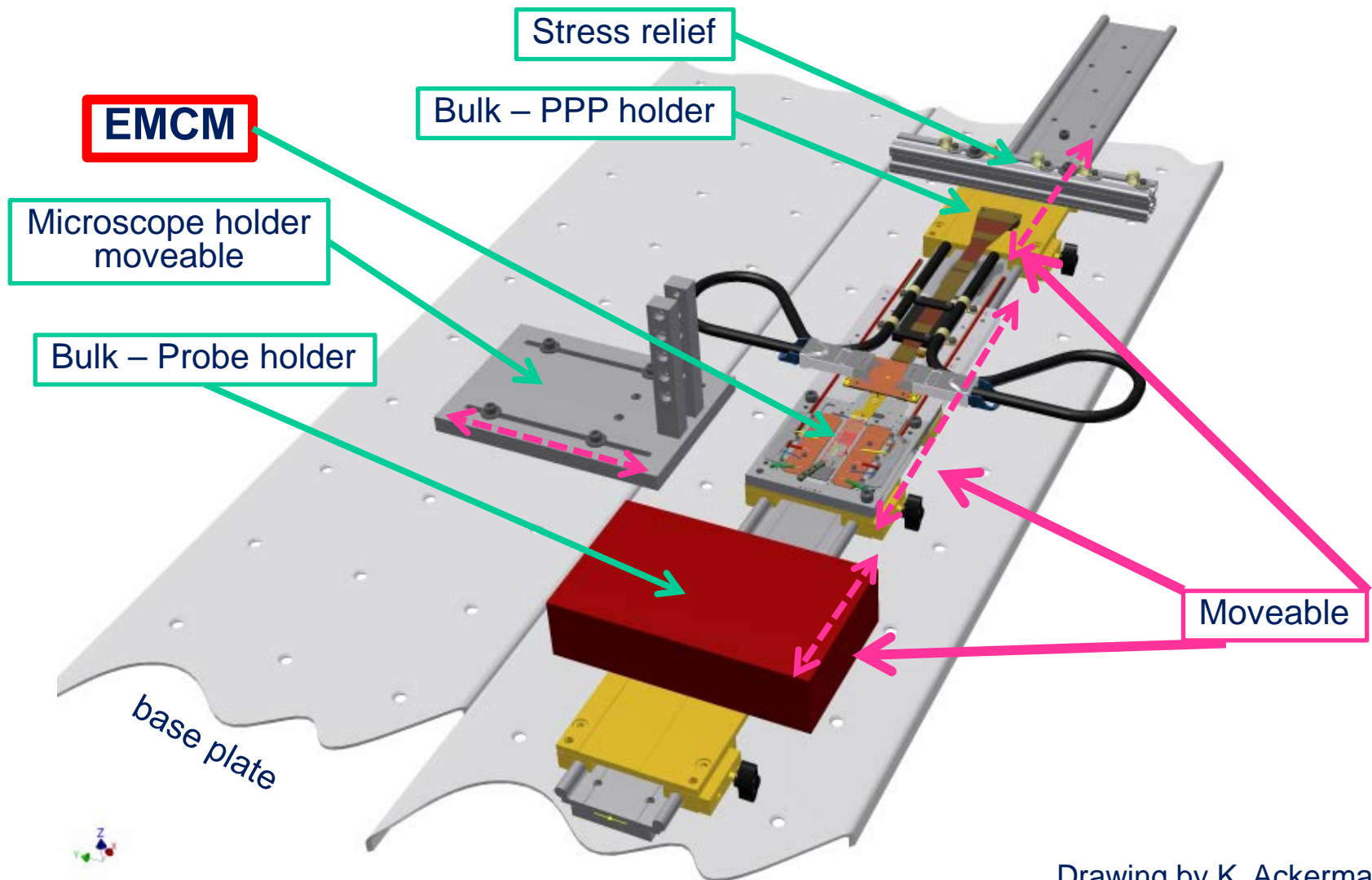
→ in discussion with Ivan, Igor, Dima, Florian ...

# Drawbacks

- Connectors (Power Samtec and Infiniband) – bulky cables
  - ⇒ finding the cold / bad solder connection is a mess!
  - ⇒ Ordered additional Power Patch Panel
  - ⇒ 5 'new' Data Patch Panel are assembled
- Software / Bitstream
- Switcher-B18v1.0 → cannot apply nominal voltages → use ClearHigh only 13V
  - ⇒ hard / impossible to operate small PXD6 test matrix

ID	Project	DHP 0.2	DCD Bv2	Sw B18v1	Location	Comment / Status
P4-1	ZMI5	4	4	6	MUC	Fully populated
P6-1	EMCM_1	1	1	1	MUC	
P6-2	EMCM_2	1	1	1	BN→MUC	
W2-4		1	1	1	MUC	Matrix glued (DESY)
W9-1	EMCM_2-2	1	1	6	MUC	Short of term. resistors
W9-2	EMCM_2-2	1	1	6	MUC	Short of capacitors

# Improved Setup – Inside the Dark Box



Drawing by K. Ackermann

## Done:

6 Switchers are working properly (still some timing issues)

One Aurora link crashes (at fully populated EMCM)

Bitstream Shifts

## To do:

PXD6 operation on EMCM

Faster DCD Characterization

Gated Mode

## We need:

data base