PXD9 Production Status - first Yield Estimation

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Outline

- PXD9 production status
- short survey through the PXD technology and possible defects
  - detection of defects, relevance of defects
- yield estimate

Production Status

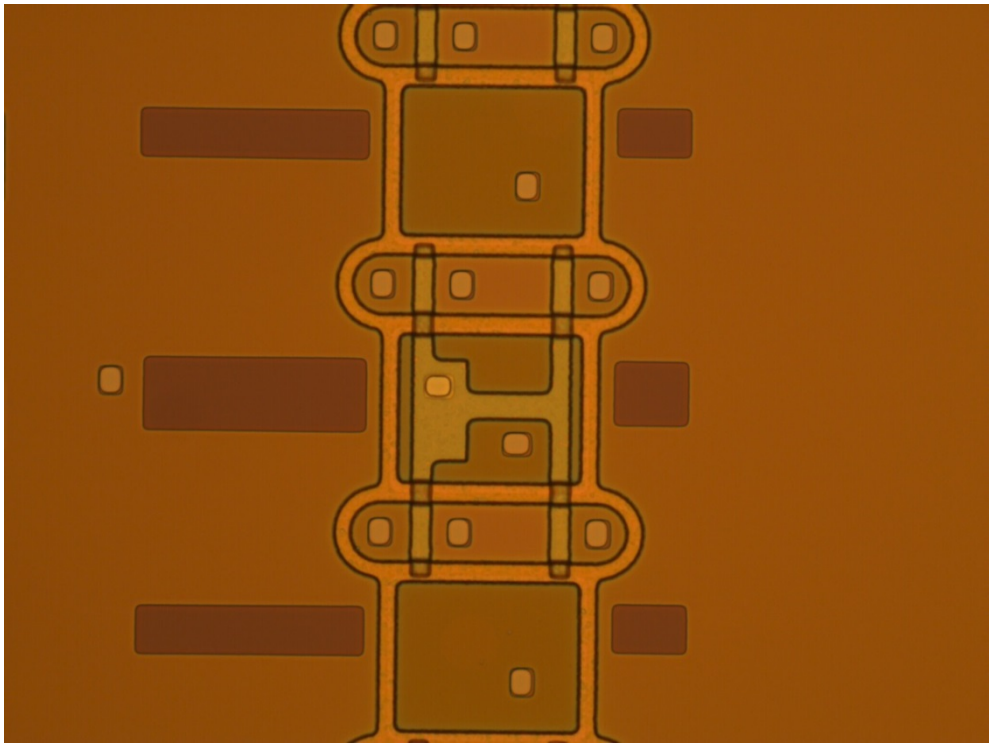
PXD9-2: 13 wafer finished
PXD9-4: 8 wafer finished
PXD9-5: 8 wafer finished
next week

Done:
SOI wafer sandwich
Top side production
2 polysilicon layer
14 masks steps
10 implantations

To be done:
2 Al layer
1 Cu Layer
backside thinning
passivation

7 mask steps remaining

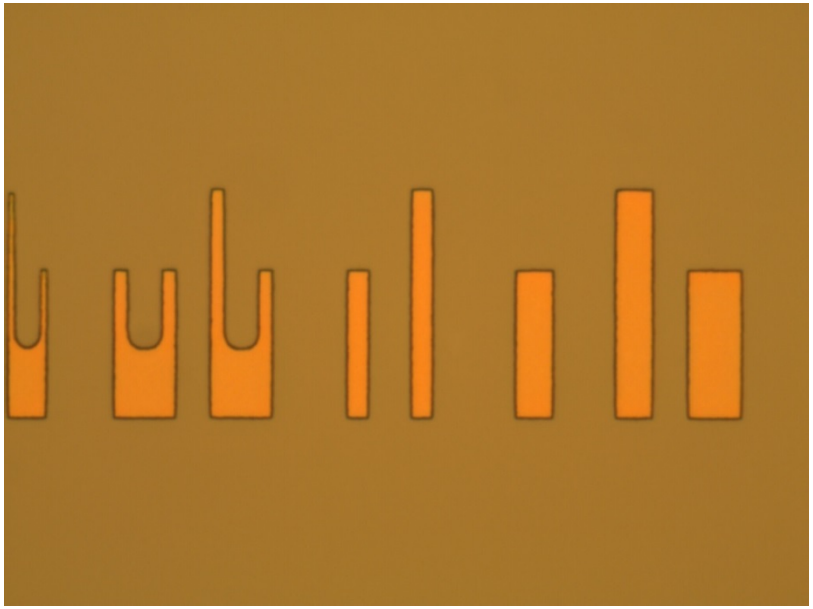
bulk and poly silicon contacts



Time for a yield estimate

Inline control of all technology modules

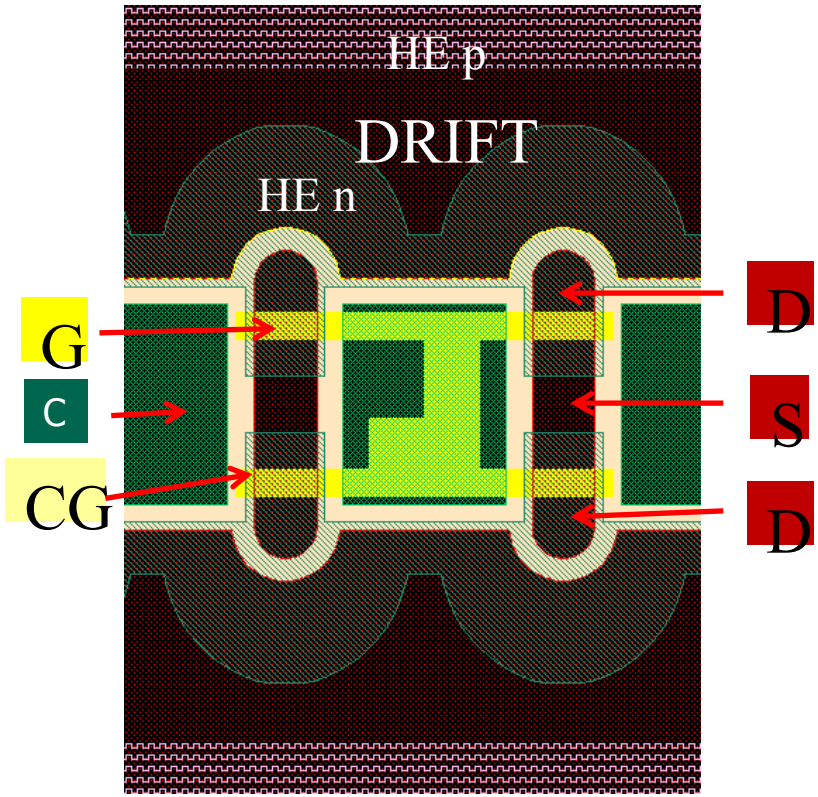
Equipment control: furnaces, etching, lithography, cleaning
layer depositions, implanter, metal sputtering
Test Diode productions
Contamination monitoring
Layer thickness control …
Line width control

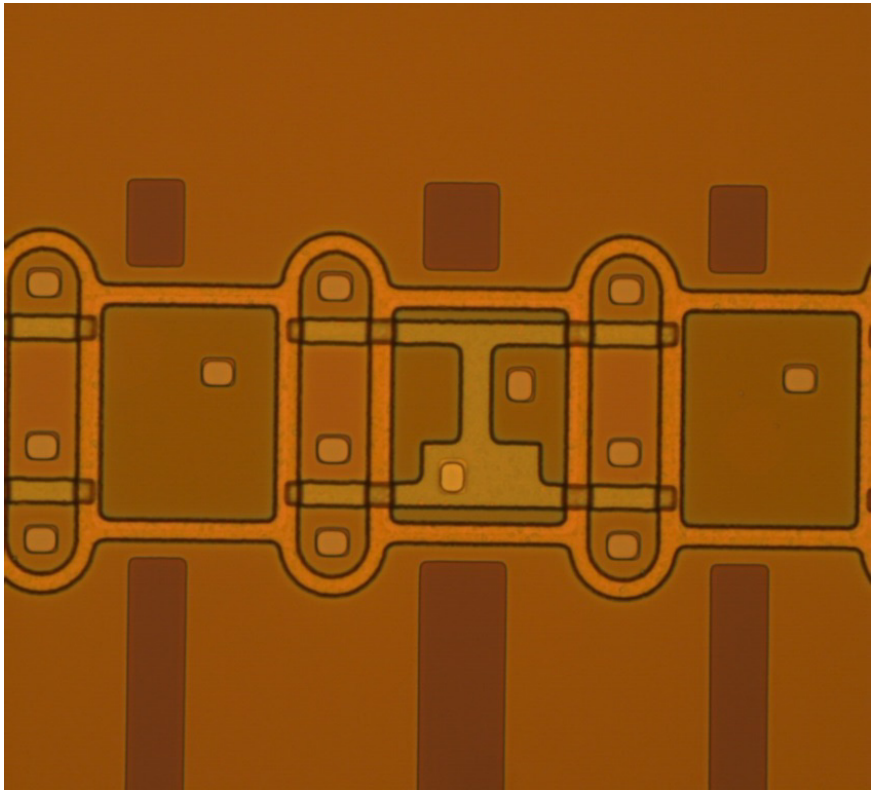


Yield killer:
particles
lithographic defects

Long lasting process …

DEPFET Design





Microscope inspection by eye -> automatization

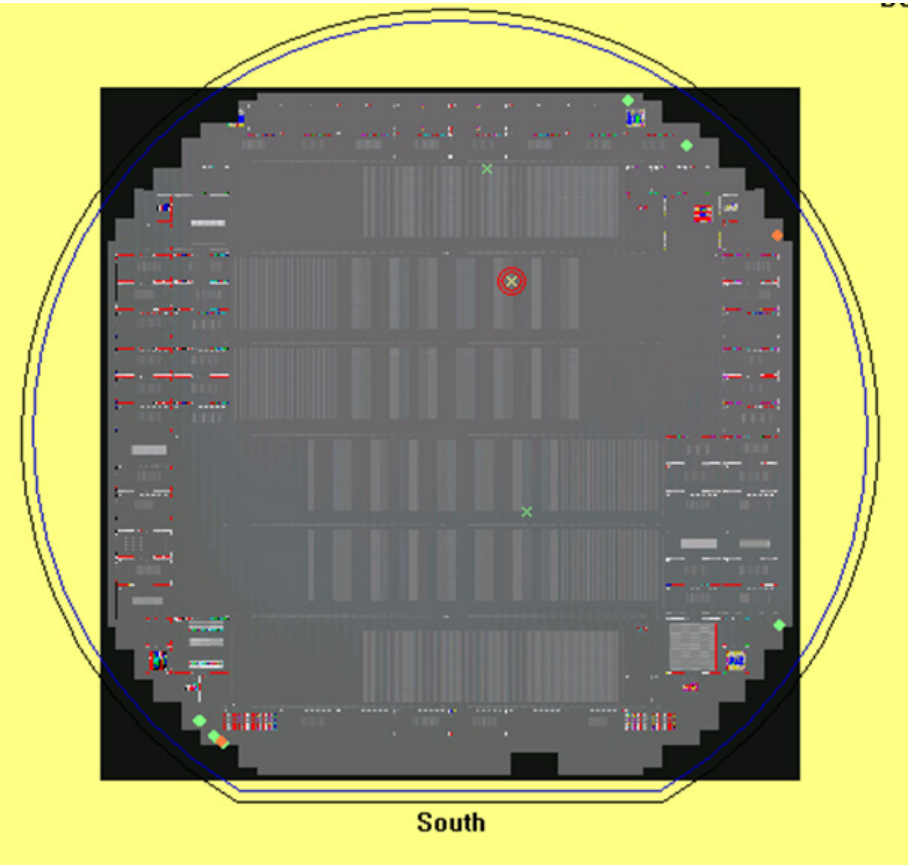
Muetec: microscope + camera
+ computer (lot of memory)

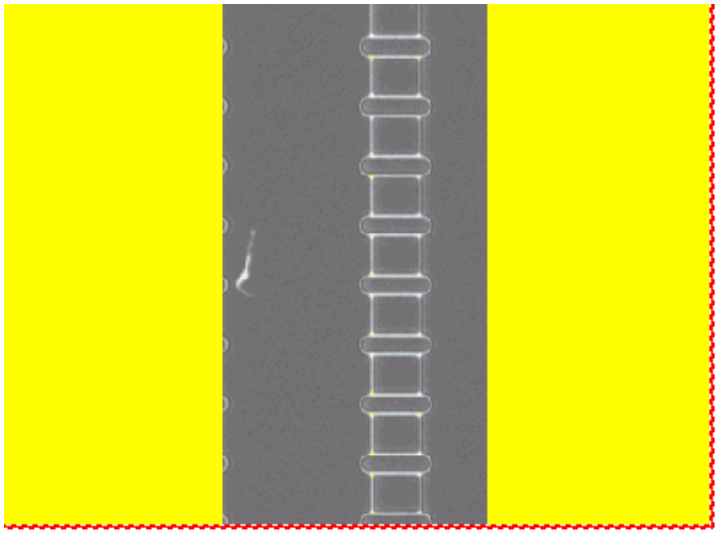
At least 4 wafer are scanned

Averaging of at least 4 images: any deviation from the average is reported

most of the microscope pictures were take to cross check with Muetec

Example





Defect counting

During the fabrication process:
all wafers are scanned by Muetec for each mask step

Results of crucial mask steps were taken
defects are counted, classified and assigned to chips

Cross checks by classical microscope pictures

Note: many of these defects do not show up in static electrical measurements
just in final operation (drift field anomalies, closed contacts)

Giving marks to the chips

German way (lowest is the best)

0 – no severe defects

1 – low impact defect – affecting just single pixels

2 – medium impact defects – affecting single rows and columns

3 – high impact defects – potentially affects a whole modul

4 – lethal defects – most likely kills a module

5 – unknown impact or not properly measured – to be clarified (if possible)

Modules on wafer

	0	1	2	3	4	5	sum
Chip1	9	9	2	2	1	6	29
Chip2	16	6	1	0	0	6	29
Chip3	15	4	3	2	0	5	29
Chip4	11	3	5	3	1	6	29
Chip5	11	4	4	2	2	6	29
Chip6	15	3	2	2	1	6	29

0 – no severe defects

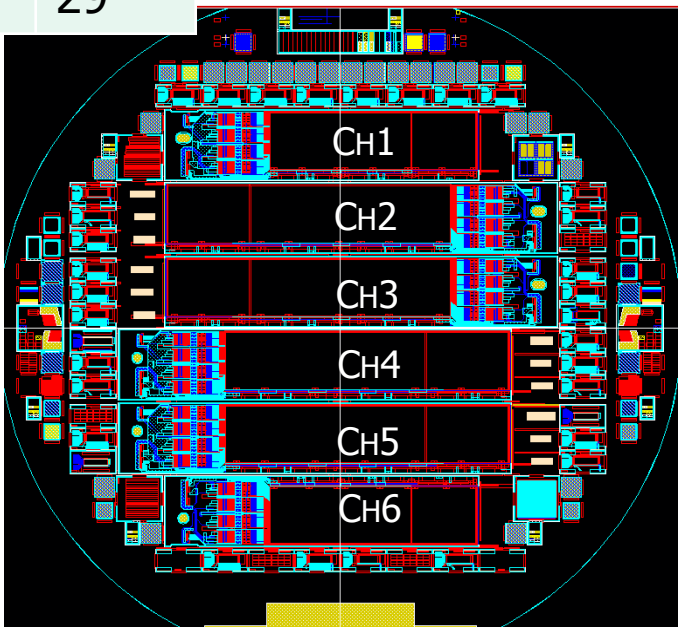
1 – single pixel

2 –single rows and columns

3 – whole modul affected?

4 – whole module killed

5 –to be clarified



Module statistic

Chip1 - inner backward
Chip2 and 3 - outer forward
Chip4 and 5 - outer backward
Chip6 - inner forward

Modules	0	1	2	3	4	5	Needed
Inner fwd	14	4	2	2	1	6	**8**
Inner bwd	10	8	2	2	1	6	**8**
Outer fwd	31	10	4	2	0	11	**12**
Outer bwd	22	7	9	5	3	12	**12**

Not bad but something is still coming!

Keep in mind it's an estimate based on best but limited knowledge!