**Minutes of the technical board meeting, April 28, 2014**

Present: L. Andricek, C. Niebuhr, P. Fischer. C. Kiesling, C. Koffmane, C. Kreidl, H. Krüger, H.-G. Moser, J. Ninkovic, I. Peric, S. Rummel.

**Switcher Bumping**

It was planned to submit an engineering run with switcherG in AMS 180nm HV technology and do the bumping by IZM. Ivan has already asked IZM for bumping and got a quote. Recently Ivan learned from AMS that they will not offer engineering runs any more unless they are followed by a volume production. This excludes our original plan. Fabrication is actually done by IBM and it seems that they want to stop the collaboration with AMS. Following options were discussed:

1. Use AMS 180nm HV as MPW and do the bumping in Mannheim (Gold stud & solder jetting).
2. Use AMS 180nm HV as MPW and do single chip bumping by Pactech (recommended by AMS).
3. Go back to AMS 350nm HV: there one has the possibility to get full wafers from an MPW (for extra 10-15 k€) which then can be bumped by IZM.
4. Ask other providers to get engineering runs in AMS 180nm HV and bump as originally planned by IZM (Mosis, CMP, Europractice)

Concerning 1): there are concerns that the gold stud bumping is unreliable since the gold is diffusing into the tin. Laci got warnings from IZM and another packaging company. Furthermore this option puts a lot of workload on Mannheim. Hence this option was abandoned.

Concerning 2): We need to ask Pactech if this is feasible and affordable. Pactech does not use gold studs but electroless Ni plating, which is reliable.

Concerning 3): We have already a working switcher version in AMS 350nm HV. Nevertheless it needs some redesign: the gated mode has to be implemented and for the JTAG the chip needs a level shifter to get the 3.3V supply to the JTAG level of 1.8V (The old chip used a special 1.8V supply line for JTAG, but this line has disappeared on the PXD9 layout in order to give more space to other critical supply lines. A re-design of the PXD9 should be avoided). According to Stefan the 3.3V supply is no problem for the power supplies. The chip is larger than the 180nm version, but the module mechanics has been designed for the 350nm technology (the change to 180nm came later) and should therefore be fine. The chip has been tested and is radiation hard. The 350nm technology offers a larger voltage range which is of some advantage (we may have destroyed some 180nm switchers by applying too high gate or clear voltages). Ivan can make the required design changes in less than two month and the changes should be safe (Hans pointed out that there was a problem with the JTAG reset polarity, to be checked). Some of us had concerns if the AMS 180nm HV may disappear and we would be forced to use 350nm anyway (similar to what happened to the IBM 90nm). Hence AMS 350nm HV sees to be a safe bet.

Concering 4). Ivan already inquired if engineering runs are offered directly by IBM. Then problem is that AMS standard cells cannot be used which requires a complete re-design of the digital part. This means more work and especially more risk. In principle CMP and Europractice offer this technology as well, but it is not clear if the can offer engineering runs and if the use of AMS standard cells is possible.

Discussing all this options and taking into account the dates of the next submissions we came to following conclusions:

* Ivan should investigate whether CMP and/or Europractice offer engineering runs (or MPW with wafer delivery) and allow the use of AMS standard cells. The information needs to be available by May 26 (DEPFET meeting in Kloster Seeon)
* Laci will investigate the Pactech option. Again, the information should be available by May 26.
* In the DEPFET meeting at Kloster Seeon we decide based on this information if we can continue with AMS 180nm (Next submission would then be in June). Otherwise we will use AMS 350nm HV. Submission would then be in August.

**DCDpipe(line) tests**

Two hybrid4 boards with DCDpipe exist and first tests have started. Unfortunately the wire bonds on the hybrid were damaged and the boards is now in Munich for repair. Four more boards will be assemble in Munich (they have ASICs for three boards but need DCDpipe and RO – both bumped – for the fourth).

In parallel the software will be adapted to the new chip, various software versions need to be unified and the code needs cleaning up (e.g. using a consistent naming convention). Test can then be made in Mannheim, Bonn and Munich.

**EMCM tests**

Two EMCMs (2-2 version) were populated with one DCDV2/DHP0.2 and 6 SwitchersB (no gating). They are now back in Munich and testing started. Unfortunately it turned out the both have shorts between SMD components. One has termination resistors shorted and is probably unusable. The second has a short of Refin to ground. This does not allow powering the analogue part of the DCD, but it is probably possible to test the functionality of the switchers.

Four EMCM3 wafers are ready for cutting. We wait essentially for the ASICs (SwitcherG, DCDpipe DHPT). In order to progress it would be good to have them as soon as possible (Last Thursday Carlos Marinhas offered 3 weeks for the DHPT, a bit late). Hans reported that their probe station is a bit unreliable which delays the DHPT testing. Jelena offered to use a probe station at the HLL in case the problems persist.