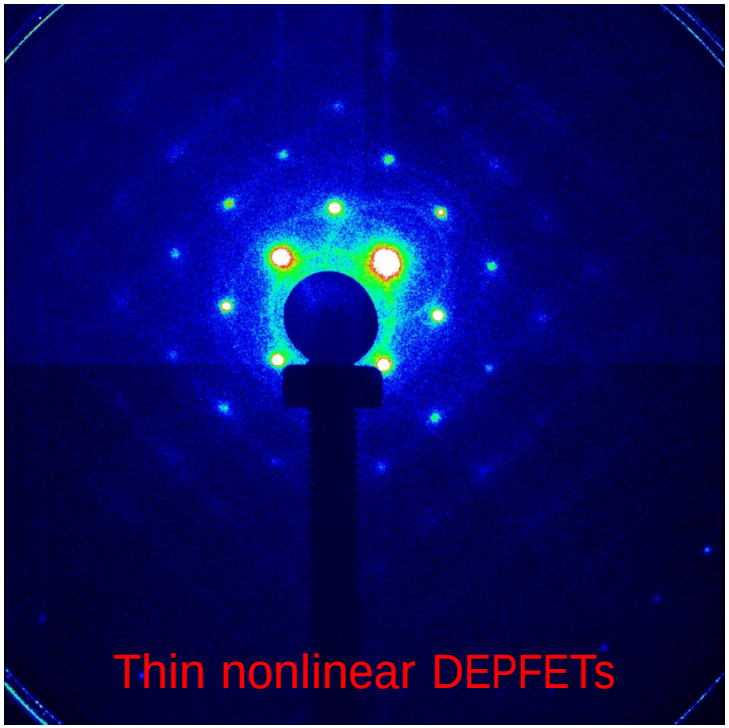
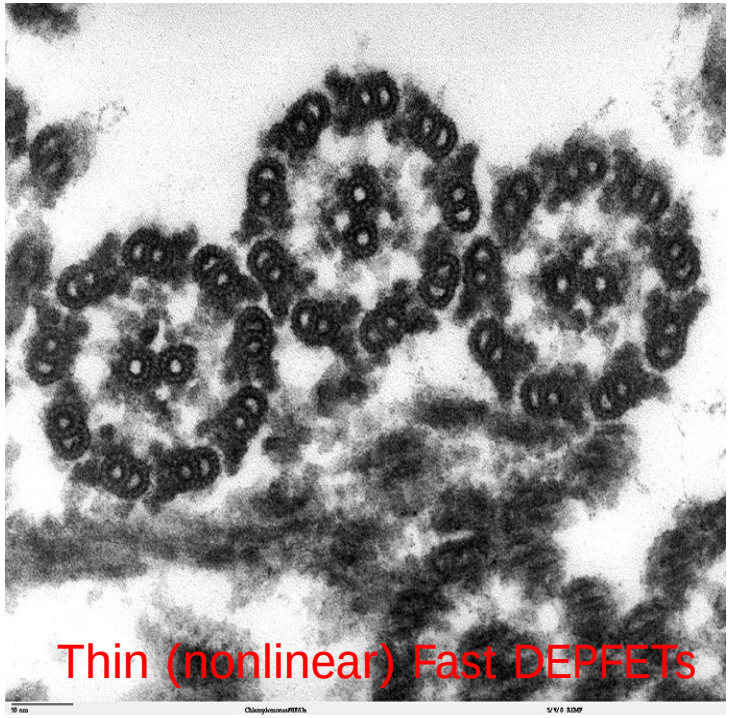
Electron detector(s) – decision to proceed with 2 detectors

Direct hit detector (DH1K) reciprocal space



- Thin detector (20-50 µm)
- ~ 1000 Hz full frame rate
- Primary electrons 60 -300 keV and 1-5 MeV
- $1E^5$-$1E^8$ electrons within < 1ps, (1000 Hz rep. Rate)

Fast application (DH80K) real space imaging



- Thickness of detector (20 - 50 µm)
- 80 kHz +/- full frame rate
- Primary electrons 100 -300 keV
- $1E^8$ electrons within < 10ns, (80 kHz rep. Rate)

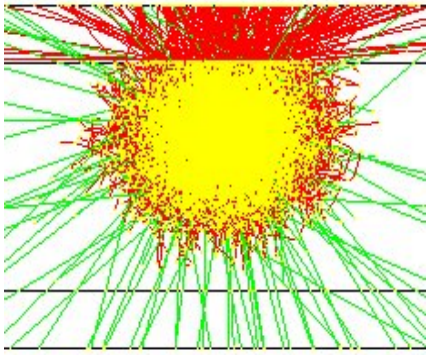
Electron Detector – DAQ Overview

- Direct Hit (DH1k) and ultra fast detector DH80k need different read-out due to their different frame rates:

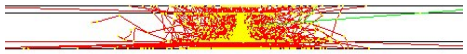
	Direct Hit (DH1k)	**DH80k**
Frame Rate	1 kHz	80 kHz
Data Stream	Continuously	Burst with 100 frames
Read-out	DCDEMCv1 + FPGA or DCDEMCv2 +DEPFET Movie chip	DCDB? + DEPFET Movie Chip
Pixel arrangement	512 x 512 2 fold readout	512 x 512 4-fold readout
ADC resolution	8 bit?	8 bit
Image type	Momentum space image	Real space image (additional pixels for Common Mode correction needed)

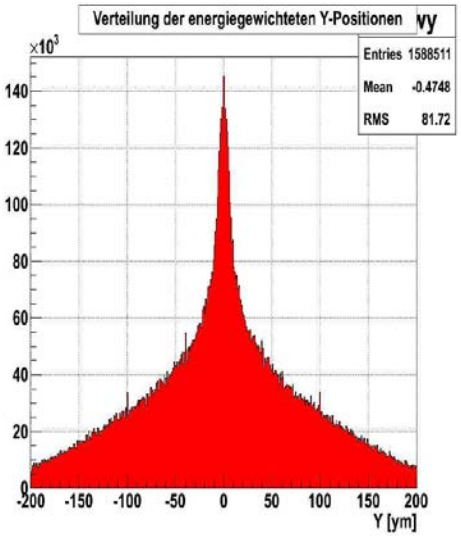
Electron detectors: simulation

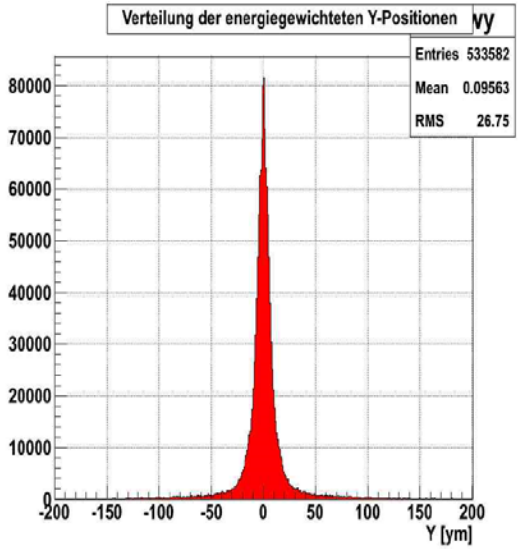
Sensor definition ongoing. Initial thickness studies done (Florian). PhD student took over.
Required information: backscattering from the material behind the sensor

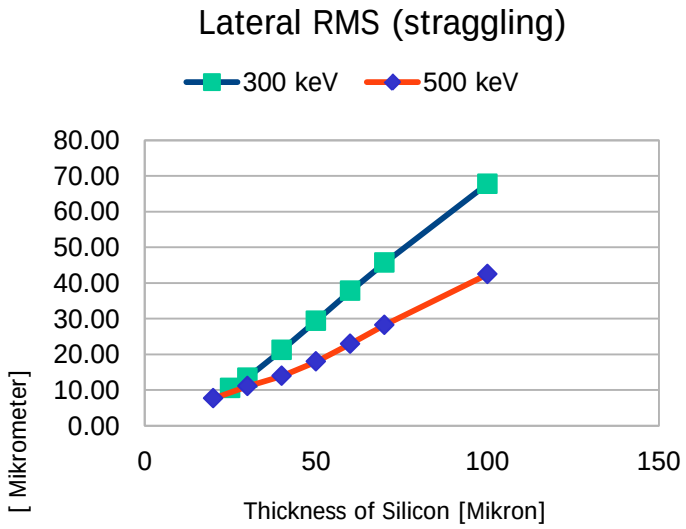


300 keV electrons









450 µm thick Silicon

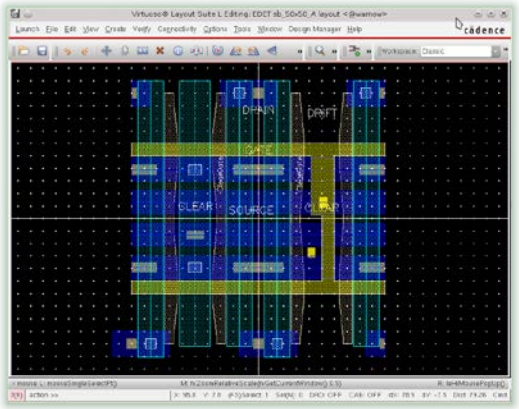
50 µm thick Silicon

Question to Sasha:

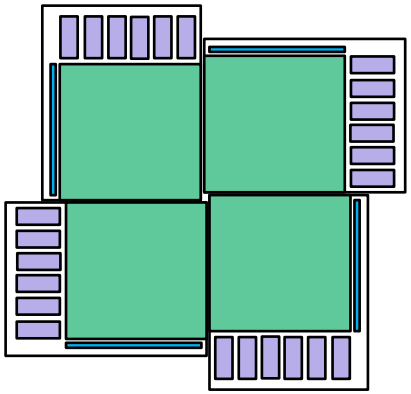
- How much material (Si) can we afford to have behind the detector
- What is optimal thickness of the sensor with 60um pixel size

Electron detectors: Sensor Status DH1K

- Conceptual design of sensors done - basic cell defined and simulated – nonlinear DEPFETs
- require new ASIC developments – collaborative effort with external groups DCDEMC (I. Peric)



60 μm pitch, two fold read out nonlinear DEPFETs



4 x 512x512 modules (1Mpixel)

Wafer layout:

- 4 x 512 pixels
- Test structures

Radiation hardness / still optimizations

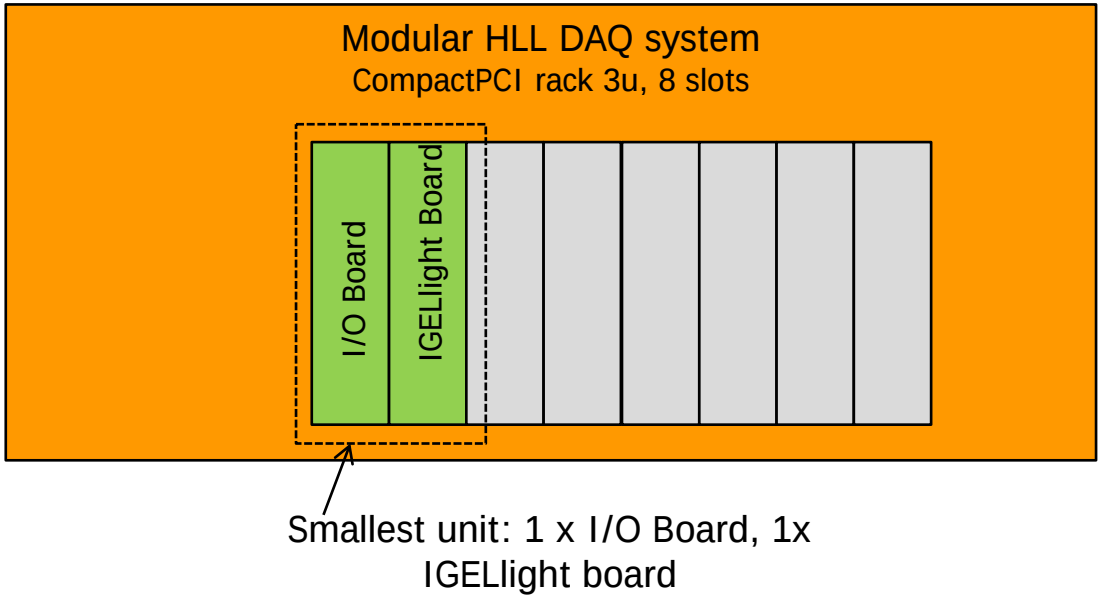
To be done to start sensor production:

- Definition of sensor thickness
- Matrix layout
- Periphery layout

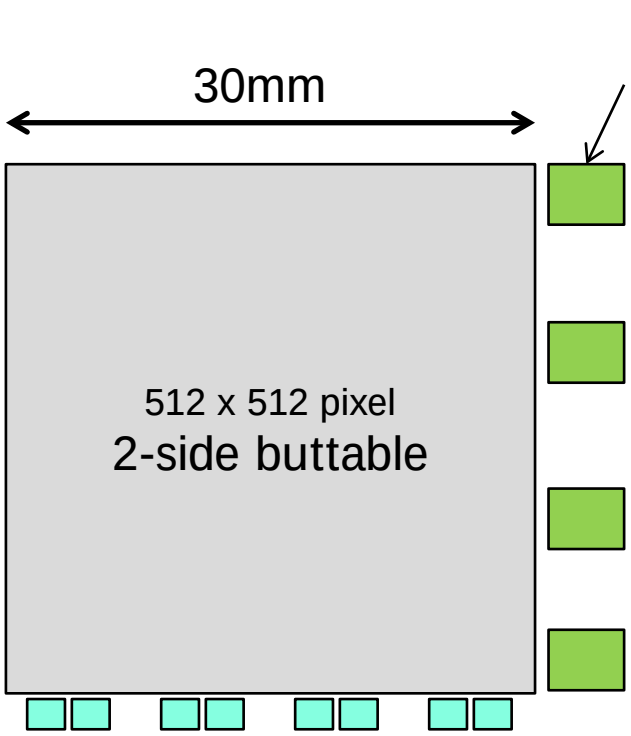
- Start SOI production by 1.06.14
- Start DEPFET processing by 1.10.14
- 8-10 wafers for 512 ?

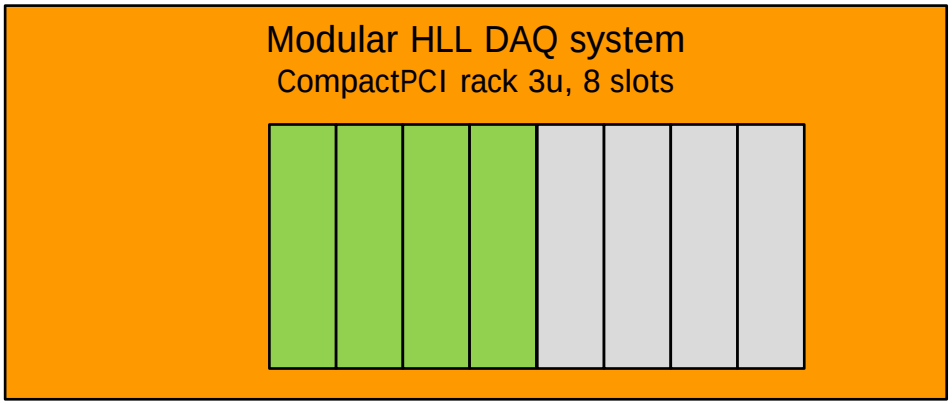
Modular HLL DAQ System

- A dedicated board (IGELlight) is used for all communication tasks
- The I/O synchronization Board is used for data acquisition and trigger processing
- The modular design allows the separation of different task to different FPGA firmware packages (easier to maintain the firmware versions)
- The prototype of the IGELlight board is already tested
- The I/O board is currently being developed



Direct Hit Detector – DH1k



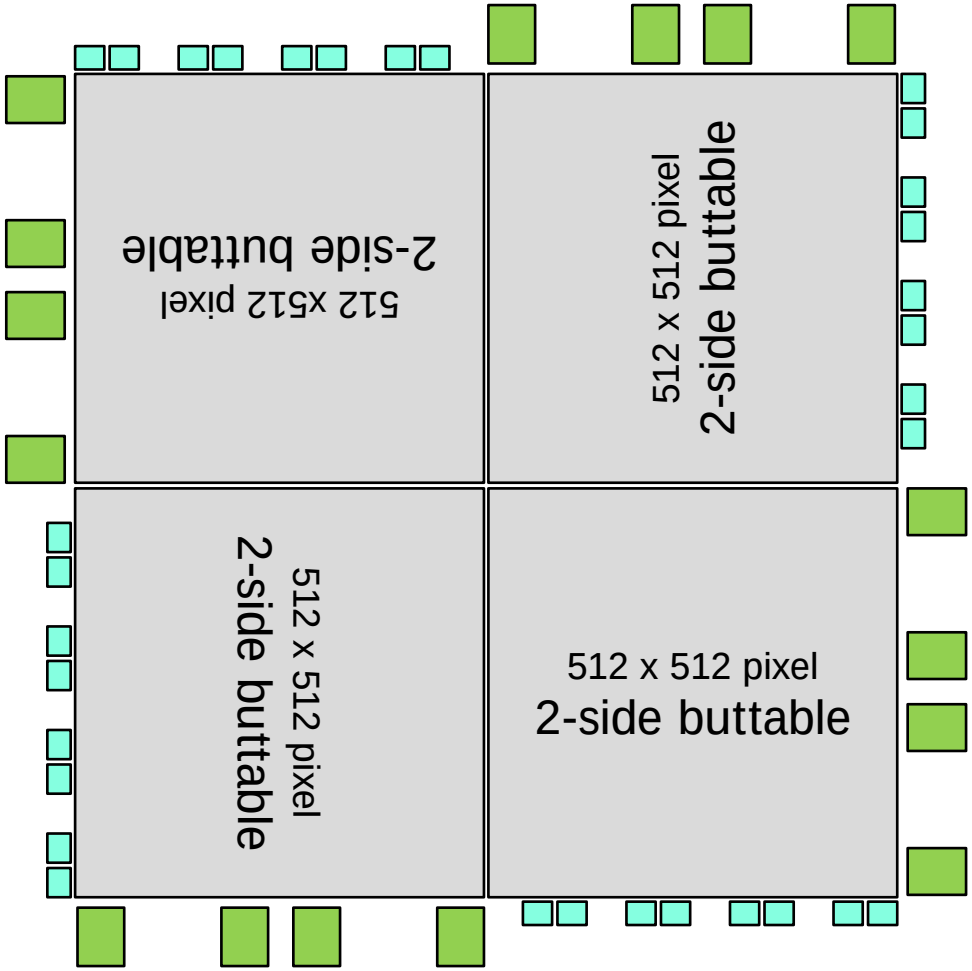


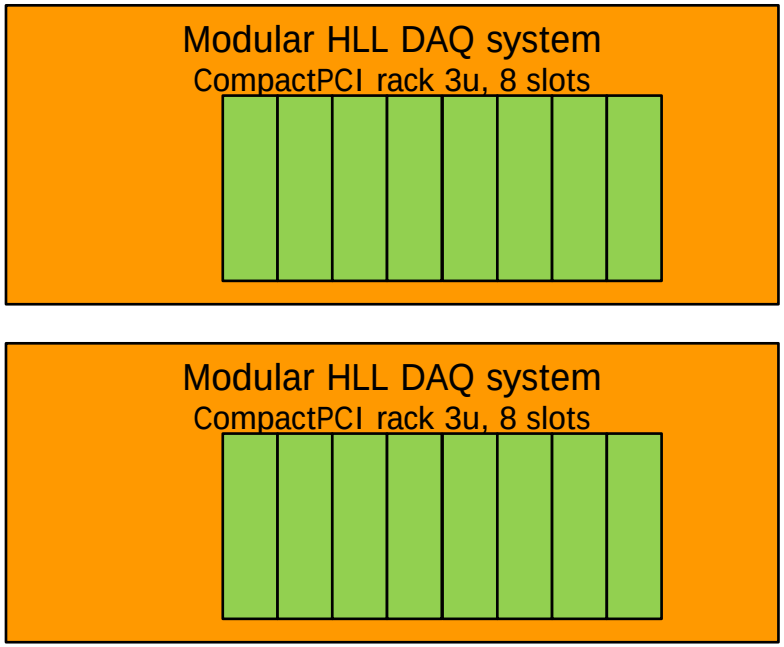
- 4 slots used for I/O and communication boards
- DAQ system includes trigger and time-stamping of the data
- Easily scalable by adding IO and communication boards

Decision on the two options:

- DCDEMCv1 +FPGA
- DCDEMCv2 +DMC

Direct Hit Detector – DH1k

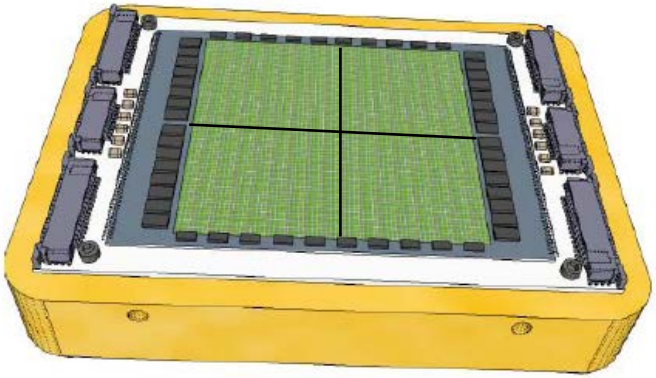


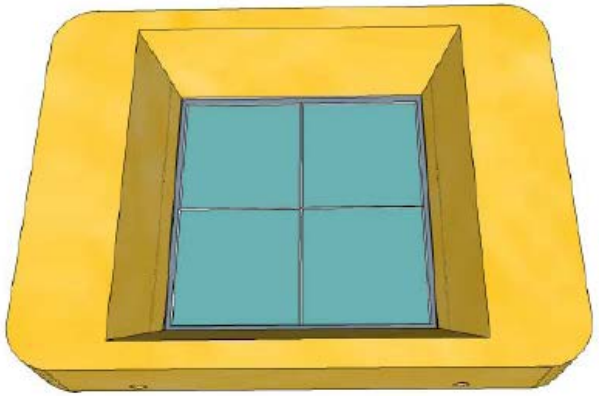


Large Direct Hit detector would need 2 compactPCI racks with 16 I/O and communication boards

Direct hit detector DH80K

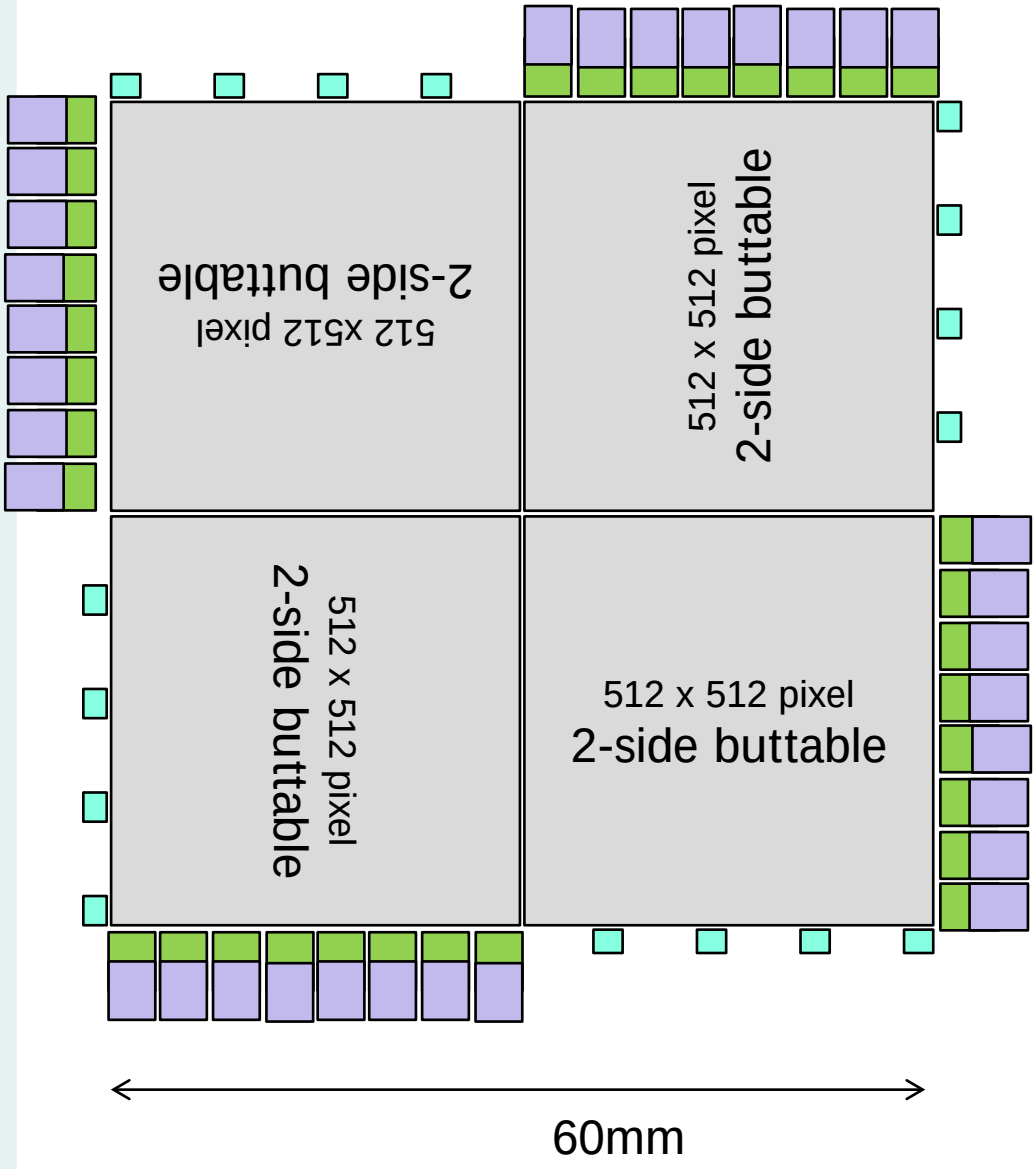
Sensor: use Belle-like DEPFET layout with 60 μm pixel size, and read out from both sides
1024x1024 pixels (bidirectional 4-fold readout)
Radiation hardness of the detector to be defined

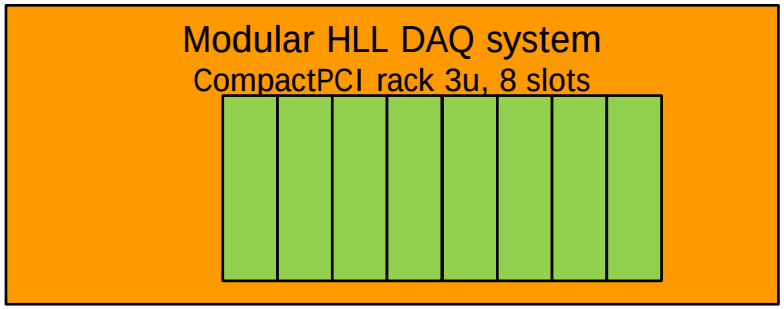


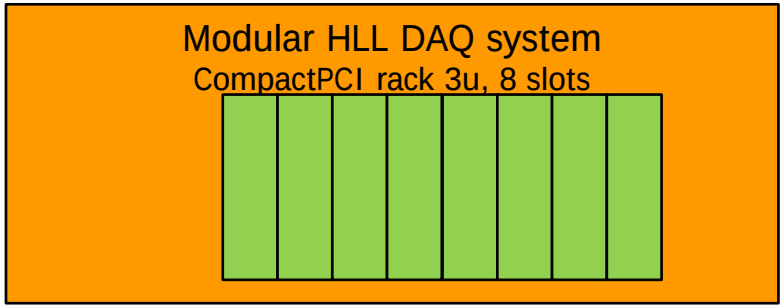


- 1Mpix, 60μm□DEPFET pixel, 4 quadrants, 6x6 cm² sensitive
- 20-50μm thin sensitive area
- Bidirectional 4-fold read out □frame rate: 100ns · 500/4 pixel = 12.5μs → 80kHz
- DCDB? + DMC (with memory to store 100 frames)
- Windowed mode operation?

Direct Hit Detector – FDH80k







Question to Sasha:

Can we allow to have some dead space

How much ?

- SOI production together with DH1k
- Start DEPFET processing by 1.01.15 ?
- 8 or 10 wafers?