

Needle card testing of DHPT 1.0

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- DHPT 1.0 bump connection
- Needle card test system
- First progress
- Issues

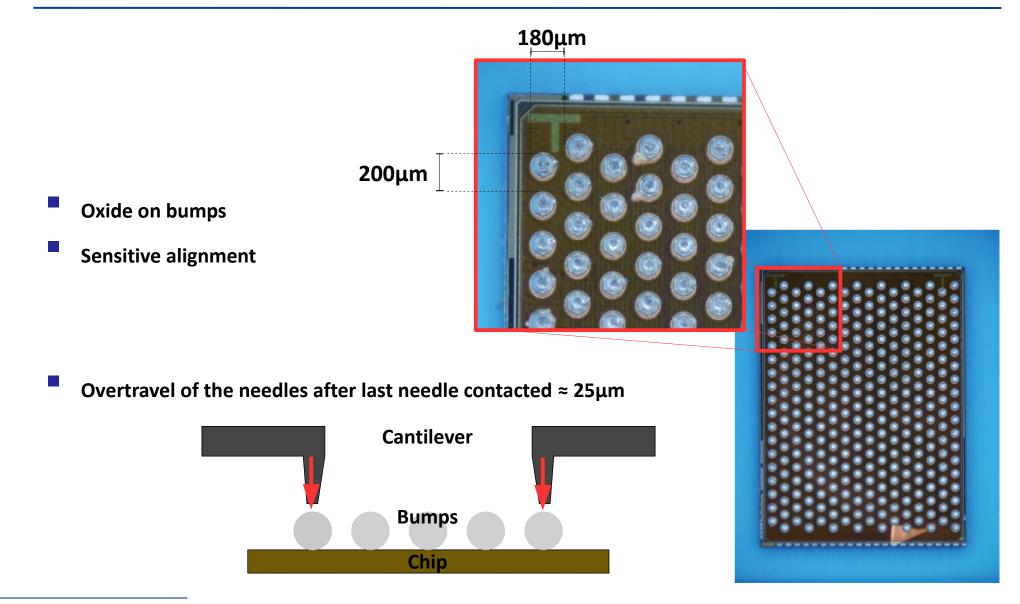


Bump mapping

- 158 of 296 (255 used) bumps connected
- Powering, JTAG DHH and DCD
- Data IO (DHH/DCD emulator)

DVD	DVDD		DVDD DCD CLK			P DVDD			DVDD		DVDD	DVDD DV		D	
DVSS	DVSS		DVSS		DVSS				DVSS		DVSS	. ~	DVSS	\sim	
VSS		VSS		VSS		VSS		VSS		VSS		VSS	Ĕ.	VS	
VDD	VDD		VDD		VDD		VDD		VDD		VDD		VDD		
DCD_T	0	VDD		VDD		VDD		VDD		DCD_C	LK	DCD_T	N S	DCD	TDI
VDD	VDD		VDD	D	CD_VRE	F	VDD	R	ow2_s	YNC		RST	Г <u>Ф_</u> Т	ак	
D00-	2	D01⊲	l>	D02<1	.>	D03<1	>	D04<1	>	D05<		D06-1	>	D07	1>
D00<0>	014		D02⊲		D03⊲		D04⊲0		D05⊲		D06⊲	_	I 07⊲0	-	
DI0-	>	D1~4:		DI2<4>		DI3<4>		DI4<4:		DI5<4:		DI6⊲	>	D17*	>
DI0<0>	N1<0:		DI2<0:		DI3<0:		DI4<0>		DI5⊲0:		DI6⊲0		[7<0>	_	
DI0<	>)1<3:	DI1<7:		DI2<7>	> DI3<3:	DI3<7>		DI4<7:		DI5<7:		DI6<	> [7<3>	~~	>
DI0<3>	>	> D1⊲s:	DI2<3:	> Di2⊲5:		> Di3<5:	DI4<3>	> Di4⊲5:	DI5<3:	> DI5<5:	DI6<3		12-		
DI0<1>	_)1<1:		/ DI2<1>		> DI3⊲1:		> Di4<1:		> DI5<1:		> Di6⊲1	\sim	> [7<1>	DI7<	>
DI0<1>		DI1<6:		DI2⊲6>		DI3<6:				DI5<6:		DI6⊲		DI7<	
DI0<2>	011<2:		DI2<2:		DI3<2:	0	DI4<2:		DI5<2		DI6<2	\sim	17<2:	\sim	r
DVI.	27	-	0.0	0.00	00.0		000		0.1		5.9 4			DVD	5
DVDD	DVDD		DVDD	\sim	DVDD		DVDD		DVDE	ັ	DVDE	<u> </u>	VDC	\sim	
DVS	\sim	DVSS		DVSS		DVSS		DVSS		DVSS		DVSS	Ľ	DVS	
DVSS	DVSS		DVSS		DVSS		DVSS		DVSS		DVSS		VSS	~	
VSS	_	VSS		VSS		VSS		VSS		VSS		VSS		AVS	
VSS	VSS		VSS		VSS		VSS		VSS		VSS		, Vss		
VDI		VDD		VDD		VDD		VDD		VDD		VDD		AVD	
VDD	VDD		VDD		VDD		VDD		VDD		VDD		VDD		
SW_C	K_N											RAME_S			AST
SW_CLK_P	0											DWW PL			
SW_FF	ME_N									D_IREF_		PAD_VEX		PAD_I	KTD
SW_FRAME_P	0											P			
SW_C	TE_N									DACTE			VIF P7	AD_VC	
SW_GATE_P										CML II	<u>v</u>				
SW_CLEAR P									смі, п	<u> </u>		P(LL_)150 P	U LVDS F		IKX
		VDD							QML_II				<u> </u>		IDY
TDO P	VSS		VSS		RST P		TRG_P		DES CL			K P	TMS P		1
VDDC		VDD C		voo a	~-	RST N		TRG N	<u> </u>	DES CL	-	SERICU	~-	TMS	N
SS CML	TX_P		VSS_CN		VDD_C		ESYNC	~-	REF_CLI		TCK_F	,	_ TDLP		
VSS_CN	11.	(TX_N	~	VSS_CIV	1	CRESET	в	FSYNC	N	REF_CLM	<u>(</u> N	TCK_N		τDL	N
				_		_		_		_					







- Xilinx XUPV5 Evaluation Platform (DHH emulator) A
- Needle card with DCD emulator B
- Power VDD = 1.2V, VDD_CML = 1.2V and DVDD = 1.8V *C*
- IGHz Oscilloscope D





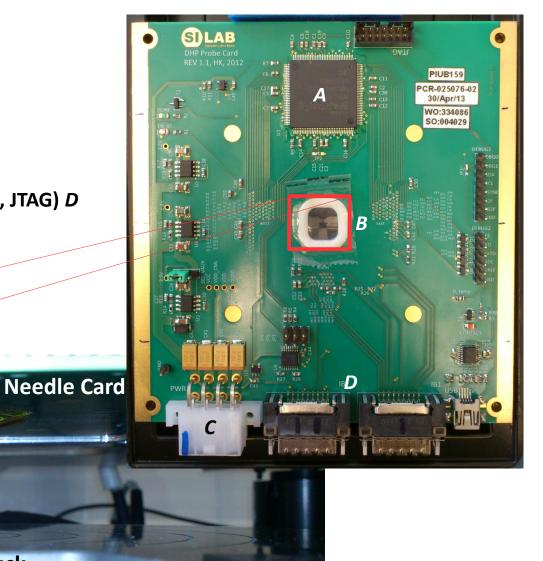


- Cantilever Needles B
- Power Connector C

Top view

Infini Band Connector to DHH emulator (Data, JTAG) D

Chuck





- Powering VDD (core), VDD_CML (serial link) and DVDD
 - Current consumption
- JTAG communication
 - DHH emulator
 - DCD emulator
- Serial link
 - GCK on chip?
 - PLL locked?
 - CML working (1.6 GHz output)
- Memory (write/read from DCD emulator) UART
- SW sequence UART

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Issues



- Contact with needle
- Oxide on bumps
- power consumption drops suddenly
 - VDD, VDD_CML or DVDD bumps disconnected?
- no GCK on chip
 - PLL, CML not working
 - Core not clocked
 - \rightarrow Core works if deserializer clock (e.g. 320 MHz) is used

BUT

- Test environment was not used for longer term \rightarrow Debugging
- Functionality of DHPT 1.0 already tested on Hybrid5



Thank you

