universität**bonn**

SI LAB
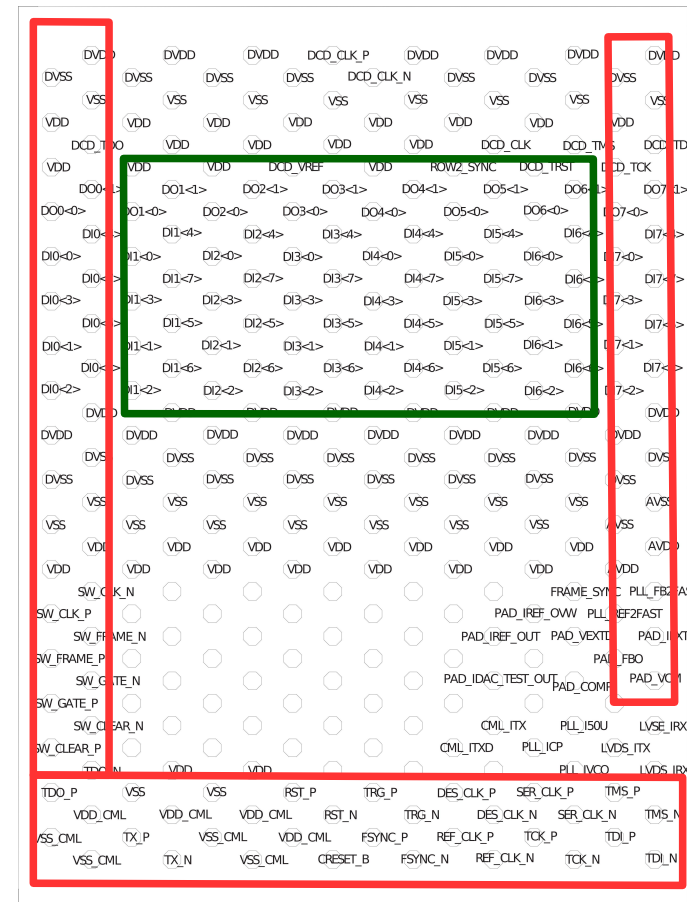Silizium Labor Bonn

Needle card testing of DHPT 1.0

Leonard Germic

University of Bonn
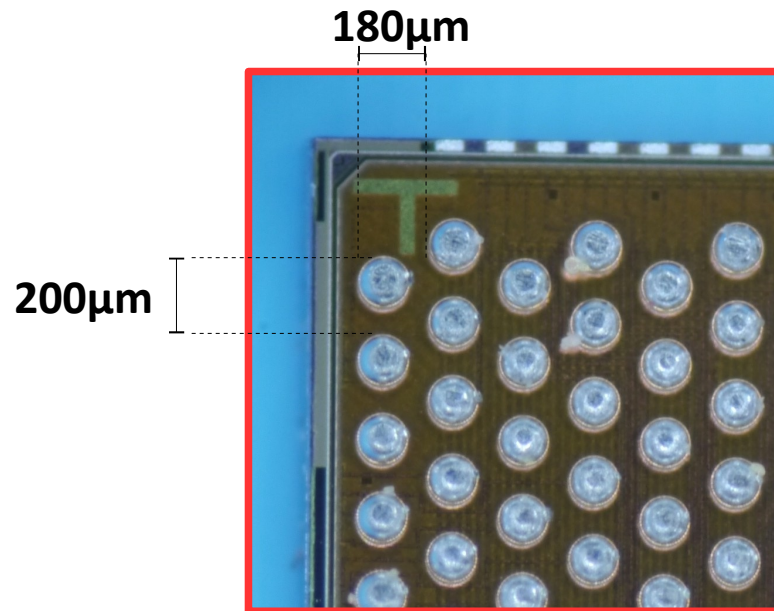
germic@physik.uni-bonn.de

Contents

- **DHPT 1.0 bump connection**

- **Needle card test system**

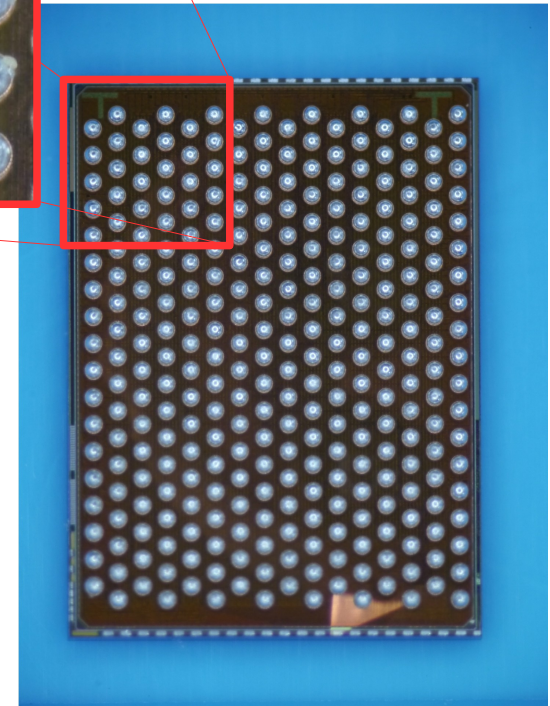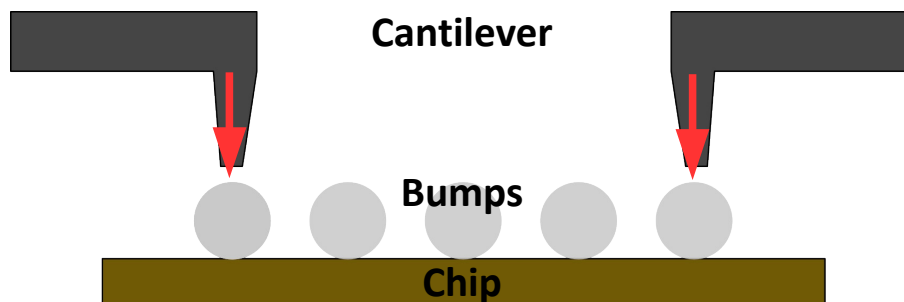- **First progress**

- **Issues**

Bump mapping

- 158 of 296 *(255 used)* bumps connected
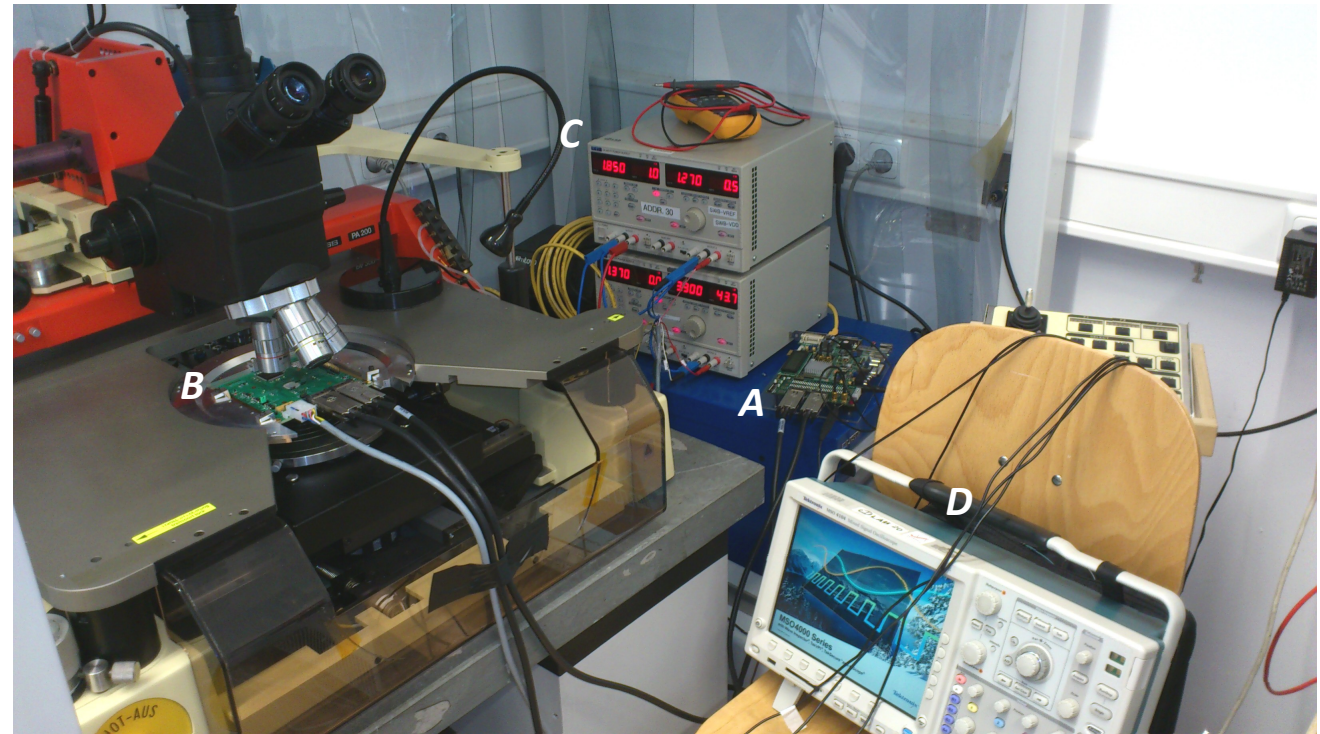
- Powering, JTAG DHH and DCD

- Data IO (DHH/DCD emulator)

180μm

200μm

- **Oxide on bumps**

- **Sensitive alignment**

- **Overtravel of the needles after last needle contacted ≈ 25μm**

Cantilever

Bumps

Chip

- **Xilinx XUPV5 Evaluation Platform (DHH emulator)** *A*

- **Needle card with DCD emulator** *B*

- **Power VDD = 1.2V, VDD_CML = 1.2V and DVDD = 1.8V** *C*

- **1GHz Oscilloscope** *D*

- **Xilinx Spartan 6 (DCDemulator)** *A*

- **Cantilever Needles** *B*

- **Power Connector** *C*

- **Infini Band Connector to DHH emulator (Data, JTAG)** *D*

Top view

Needle Card

Chuck

Side view
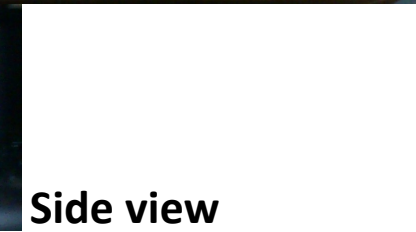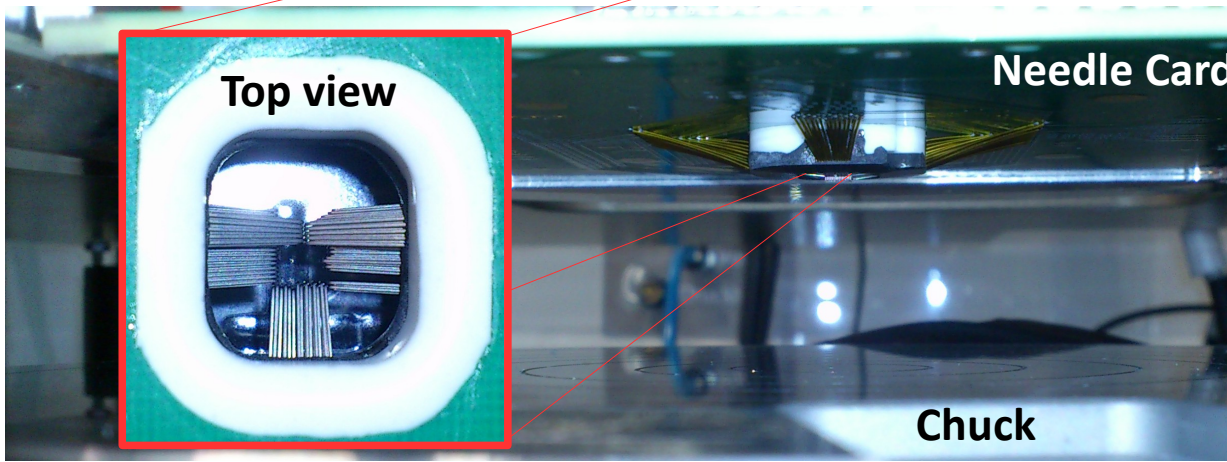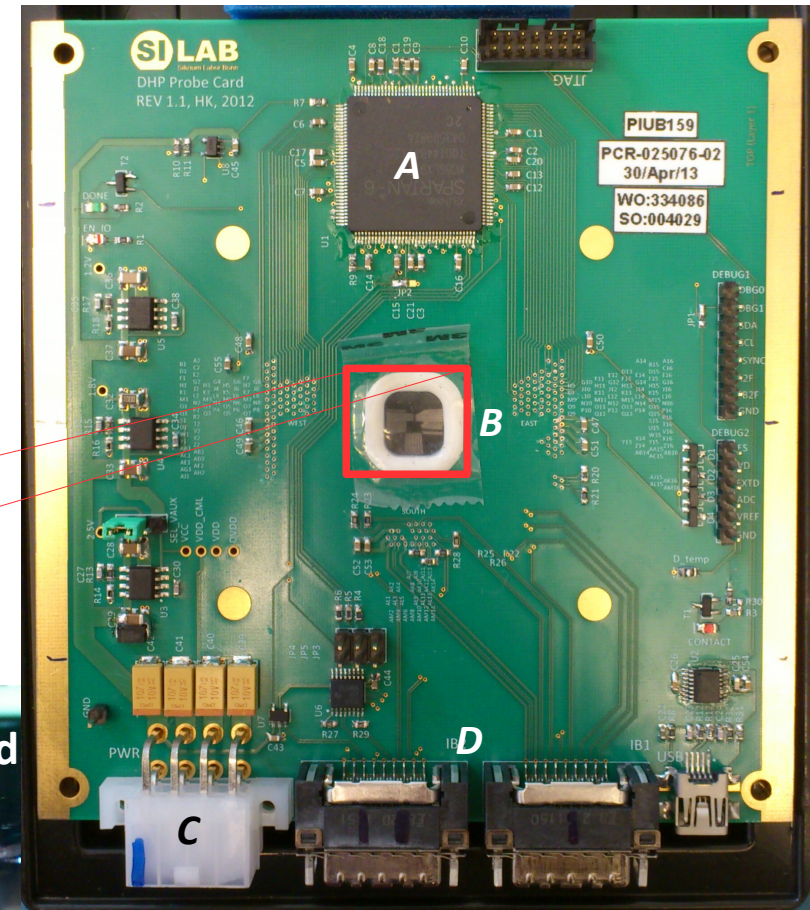
- **Powering VDD (core), VDD_CML (serial link) and DVDD**
  - **Current consumption**
- **JTAG communication**
  - **DHH emulator**
  - **DCD emulator**
- **Serial link**
  - **GCK on chip?**
  - **PLL locked?**
  - **CML working (1.6 GHz output)**
- **Memory (write/read from DCD emulator) - UART**
- **SW sequence - UART**
- **...**

- **<u>Contact with needle</u>**

- **Oxide on bumps**

- **power consumption drops suddenly**

  - **VDD, VDD_CML or DVDD bumps disconnected?**

- **no GCK on chip**

  - **PLL, CML not working**

  - **Core not clocked**

  → **Core works if deserializer clock (e.g. 320 MHz) is used**

  BUT

- **Test environment was not used for longer term → Debugging**

- **Functionality of DHPT 1.0 already tested on Hybrid5**

Thank you