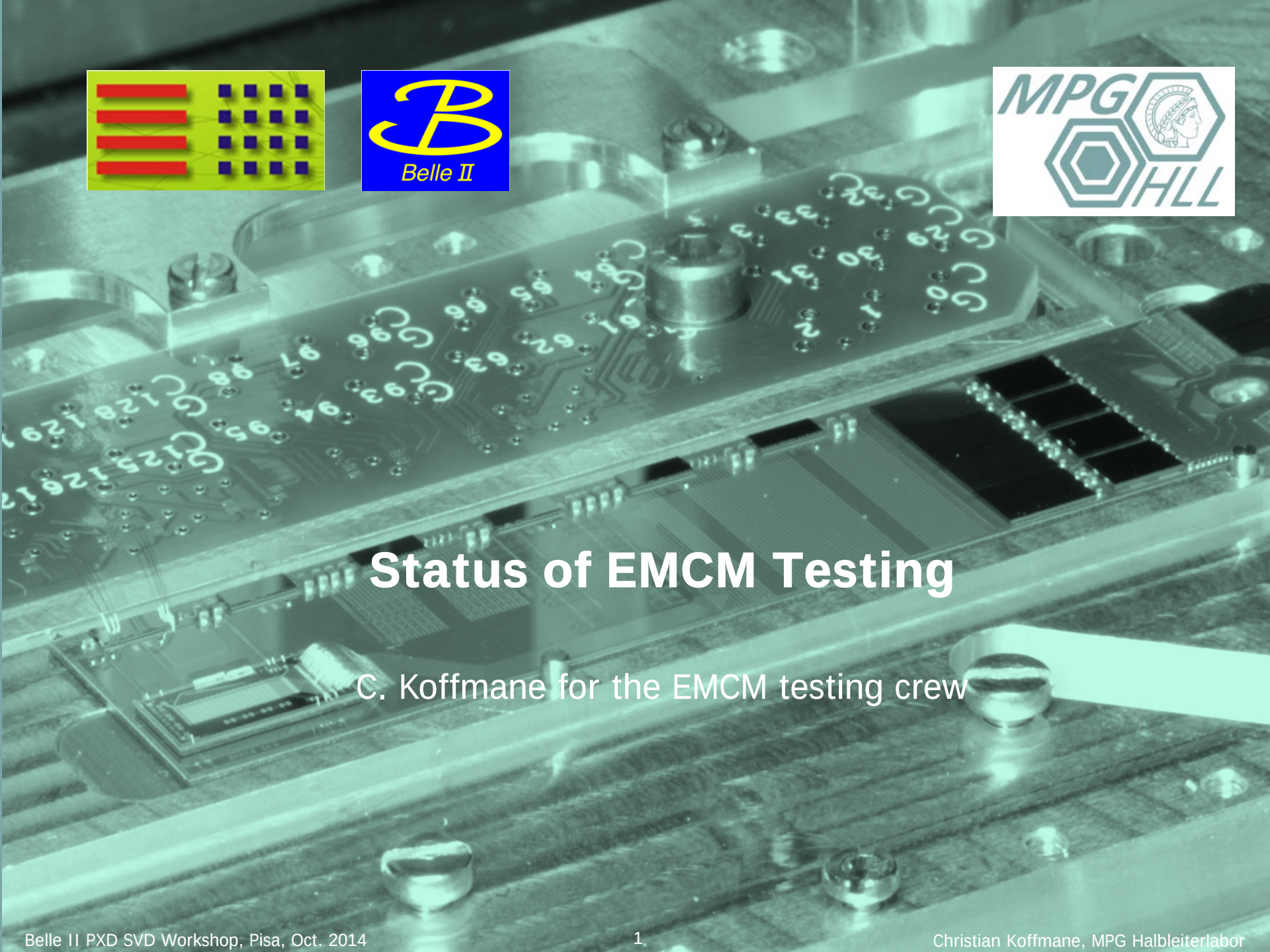
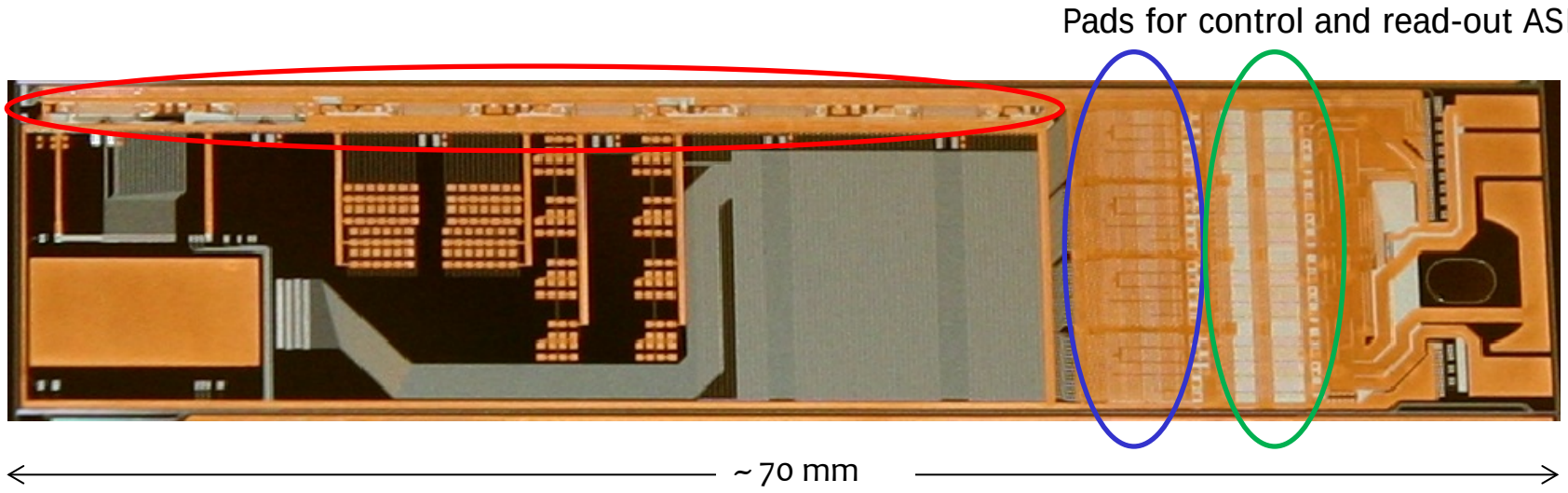


Status of EMCM Testing

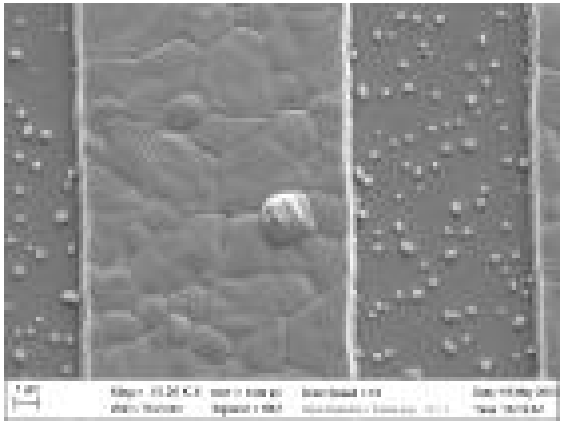
C. Koffmane for the EMCM testing crew

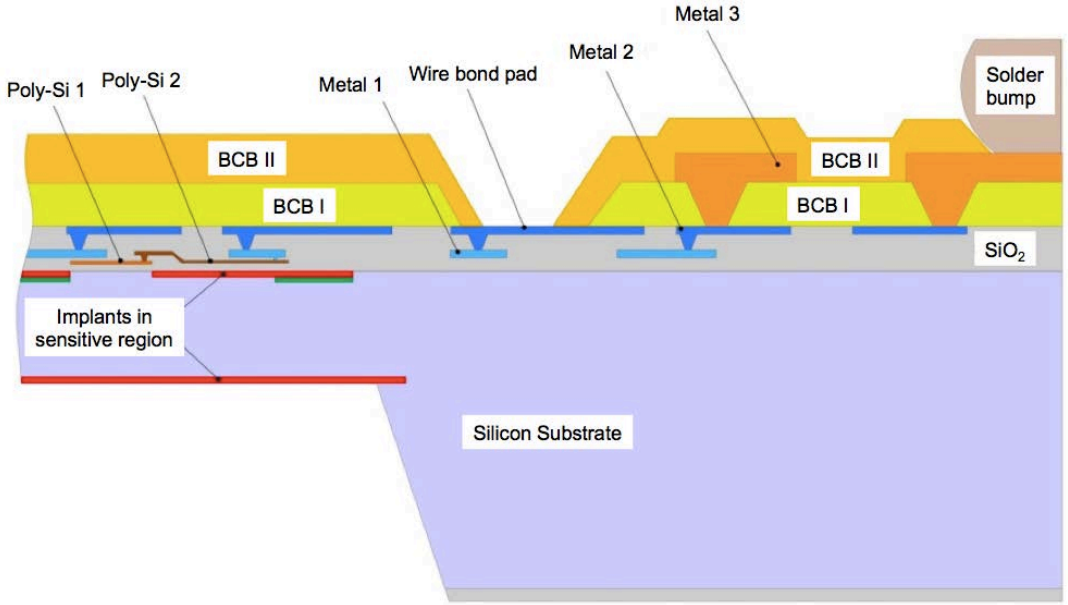
Electrical Multi-Chip Module – a reminder

- 3 metal layers on silicon substrate
- 2149 different electrical nets
- 4055 test pads (size down to 70µm x 70µm and 50µm x 100µm)
- ~15k vias connecting the metal system in 3D (10k aul1 to alu2, 5k alu2 to cu)



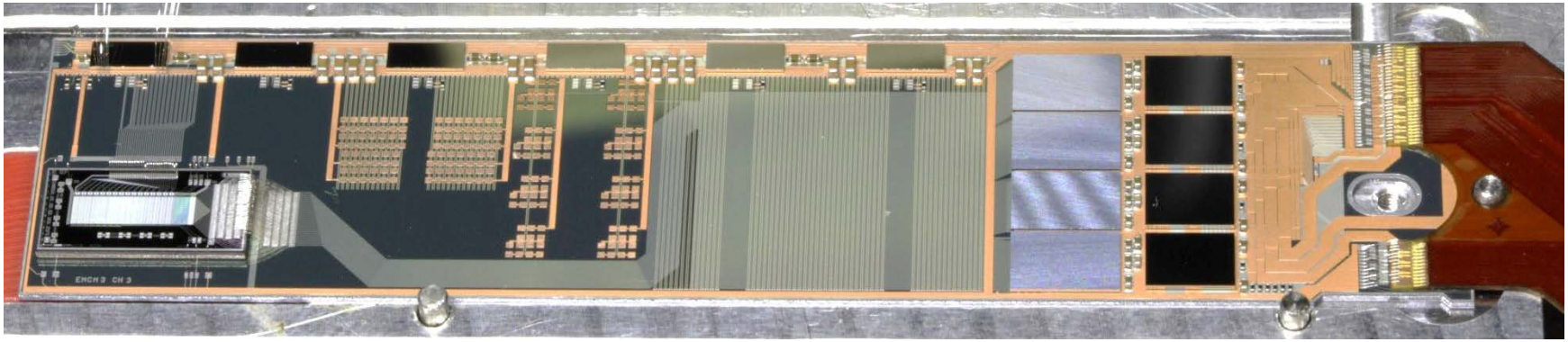
Electrical Multi-Chip Module – Substrate Testing





- Technology of the inter-metal dielectric chosen after EMCM3 wafer measurements
  - Open/short and breakdown structures (summary was given at the 18th B2GM June 2014 by Paola Avella)
- EMCM4 to verify the results from EMCM3
  - 5 Wafers have been finalized with Cu last week → wafer-level testing will take place in the next week
- EMCM3 wafers cut and modules used for the latest assemblies

EMCM as of today



EMCM http://www.hll.mpg.de/twiki/bin/view/DepfetInternal/ShoppingMall#EMCM

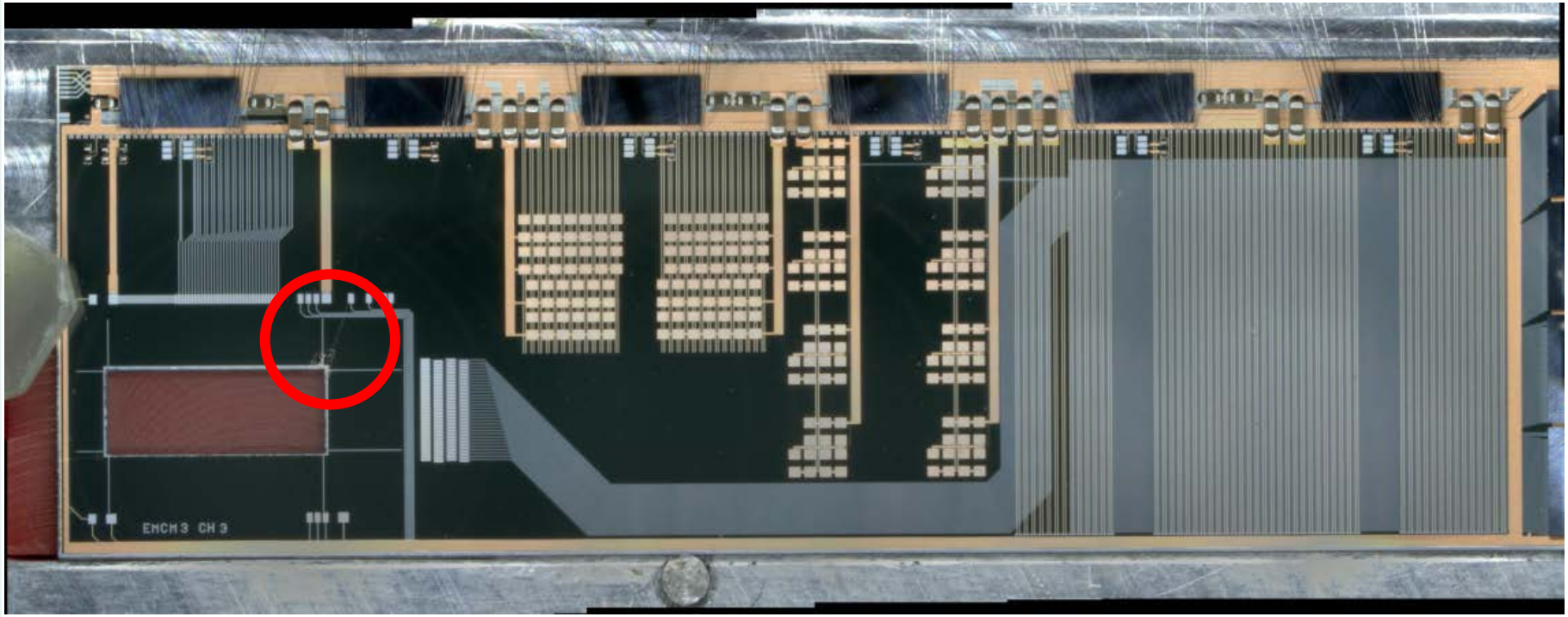
ID	Project	Status	Comment	DHP	DCD	Switcher	Location	last edit
P4-1	ZMI5	(fully populated)	http://www.hephy.at/hephydb/cakephp/hephydb/items/view/9486	4x DHP0.2	4x DCD-Bv2	6x Switcher-B18v1.0	HLL	2014/09/19
P6-1	EMCM_1	SWB: output signals don´t toggle after accident during probing (bond wires touching) DHP & DCD ok	http://www.hephy.at/hephydb/cakephp/hephydb/items/view/9515	1x DHP0.2	1x DCD-Bv2	1x Switcher-B18v1.0	MPP	2014/09/19
P6-2	EMCM_2	Clear to Source short -> not suited for PXD6 matrix	http://www.hephy.at/hephydb/cakephp/hephydb/items/view/9515	1x DHP0.2	1x DCD-Bv2	1x Switcher-B18v1.0	HLL	2014/09/19
W9-1 (Wq-1)	EMCM-2-2	term resistor shorted	corner is broken (where PXD6 could be assembled)	1x DHP0.2	1x DCD-Bv2	6x Switcher-B18v1.0	HLL	2014/09/19
W9-2 (Wq-2)	EMCM-2-2	SWB (all SWB assembled)	1 missing pad in DCD	1x DHP0.2	1x DCD-Bv2	6x Switcher-B18v1.0	HLL	2014/09/19
W17-3	EMCM-3-2	crack in Si-Substrate, not suited for small PXD matrix		4x	4x DCD-Pipeline	6x Switcher-B18v2.0	HLL	2014/09/19
W17-4	EMCM-3-2	Probe Card			4x DCD-Pipeline	6x Switcher-B18v2.0	HLL	2014/09/19
W18-3	EMCM-3-2	PXD6 matrix E07 Wafer22 mounted			4x DCD-Pipeline	6x Switcher-B18v2.0	HLL	2014/09/19

Three samples fully populated with latest ASICs (DCDPipeline, DHPT, SwitcherB18v2)

EMCM3 W17-3

- DCDPipeline 1-4 and DHP 1-4 can be configured and read out
- SWB5 and SWB6 not functional (crack in Si-substrate – from the corner of the hole for the small PXD6 matrix)

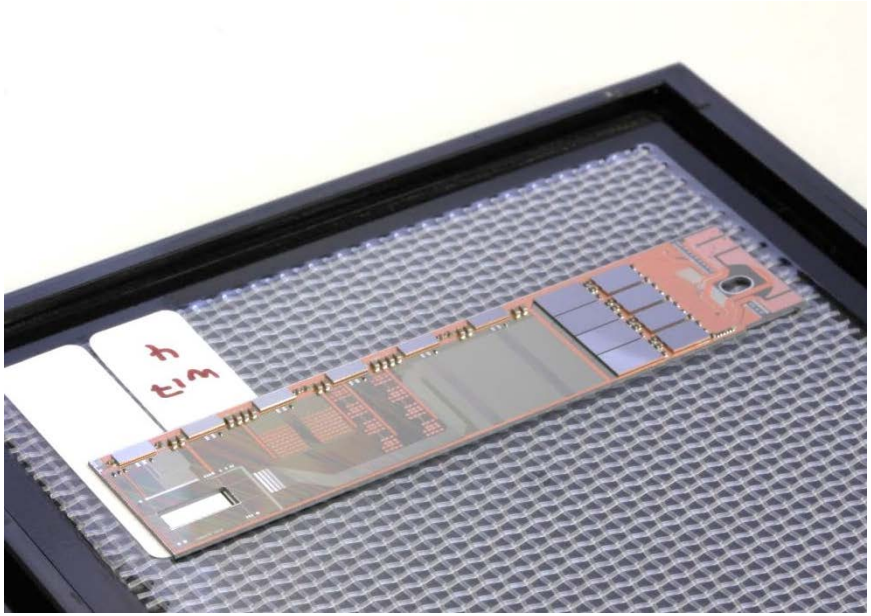
SWB6 SWB5 SWB4 SWB3 SWB2 SWB1



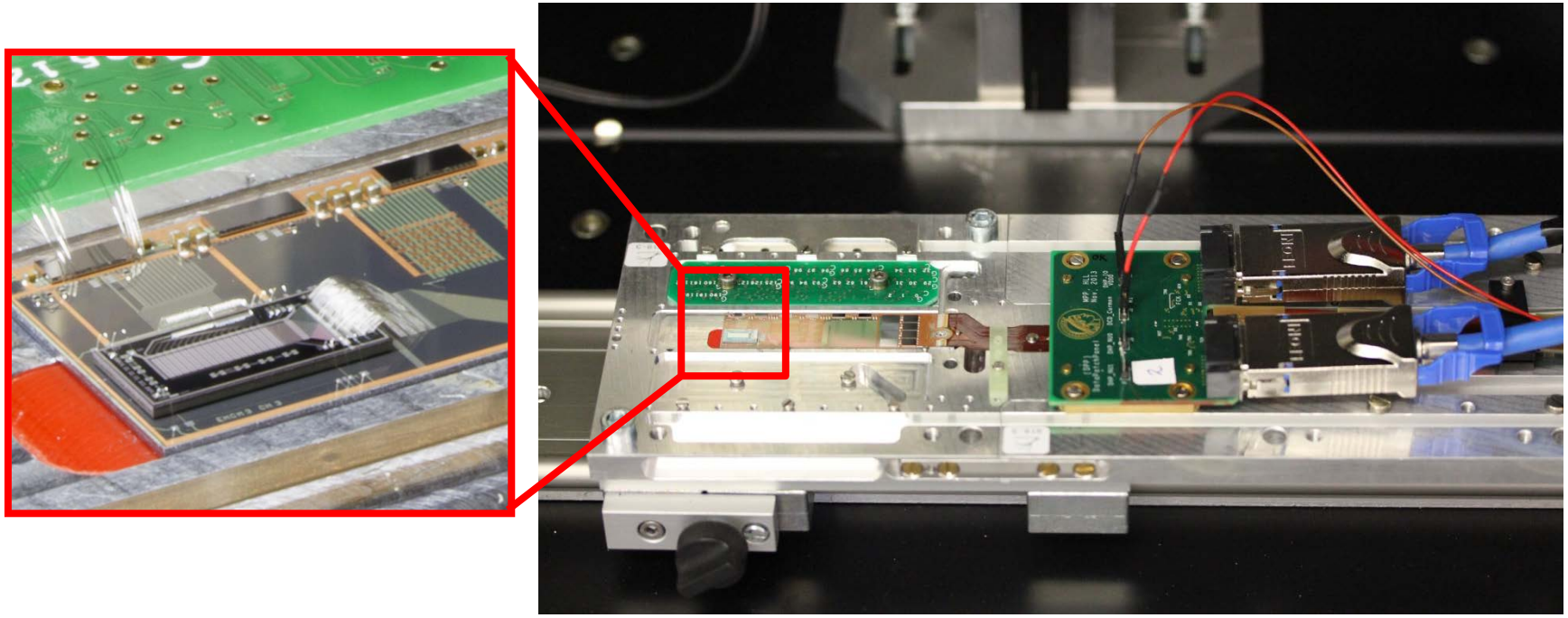
EMCM3 W17-4

- Fully assembled with DCDPipeline, DHPT, SwitcherB18v2
- Dedicated for EMCM probe card setup

- Probe card Setup is in preparation by Marca Boronat at the HLL
  - since last week all components (DHH, LMU Power Supply, mechanical holder for probe card) are available
  - Integration is ongoing (help from DHH and power supply experts needed)



EMCM3 W18-3



- All ASICs can be configured and read out, SWB outputs ok!
- Small PXD6 matrix (Wafer 22, E07, standard design 50 x 75 µm², short gate length 4µm) connected to (½) DCDPipeline
- EMCM connected to short (10 cm) Kapton, Data Patch Panel, Infiniband cables

What do we want to learn from the EMCM?

- Technology, backend assembly processes (ASICs, passives, Kapton), Signal and power integrity of the cables/PCBs

- JTAG programming of all ASICs (incl. Boundary Scan of the digital IOs)
- Stable operation of the 4 high speed links from DHP to DHH
- Low noise of all 1000 DCD channels **at 320MHz**
- Stable Switcher outputs on a fully assembled EMCM
- PXD6 operation on the EMCM

What do we want to learn from the EMCM?

- JTAG programming of all ASICs (incl. Boundary Scan of the digital IOs)

→ JTAG programming of all ASICs done (see talk Dmytro Levit)

→ Boundary Scan:

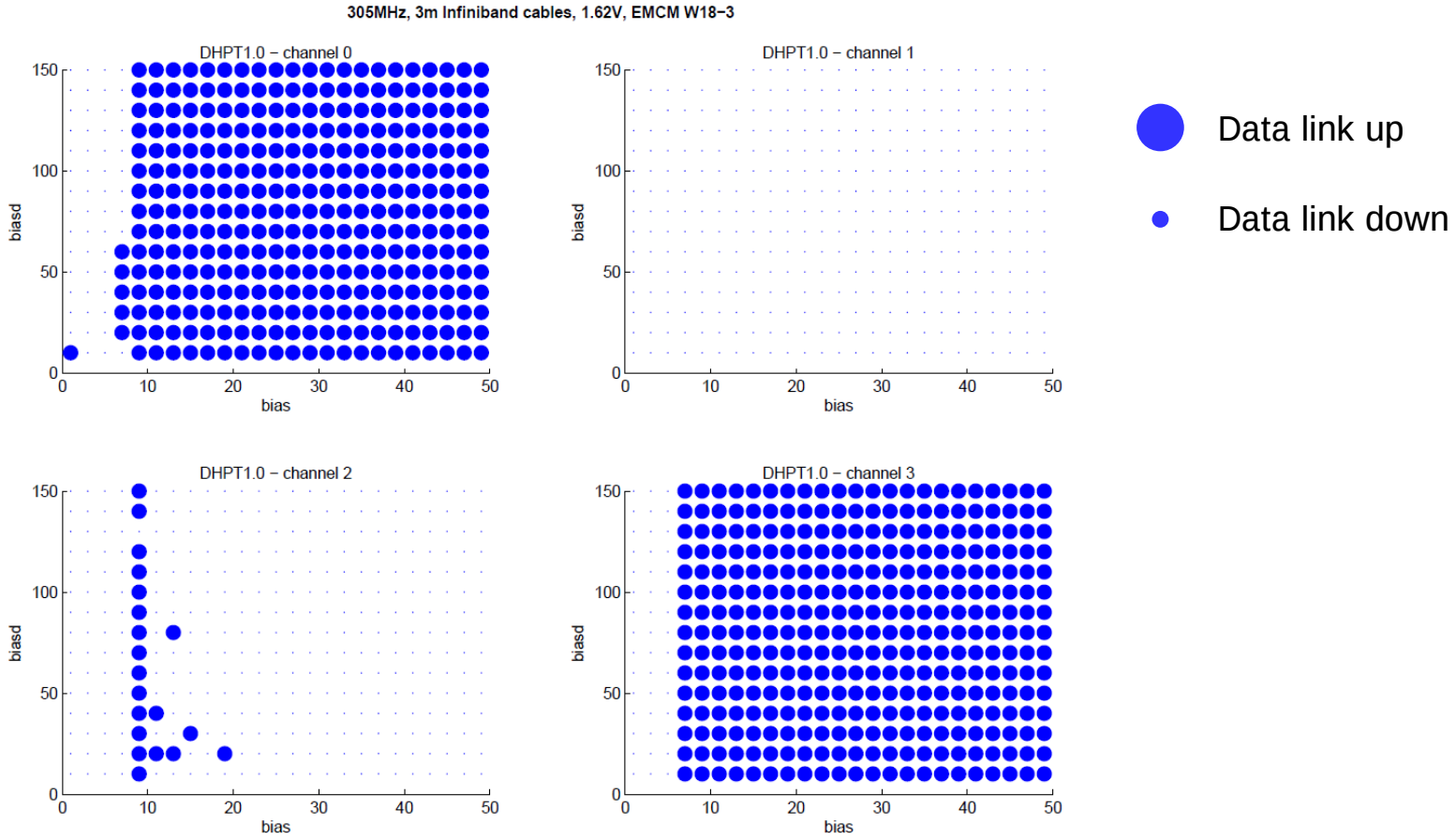
  → Manual scanning of single links possible (e.g. SWB control lines)

  → Systematic scanning using dedicated hardware and software is not done yet

  (Philipp Leitl, Master Student @ MPP, started to work on that)

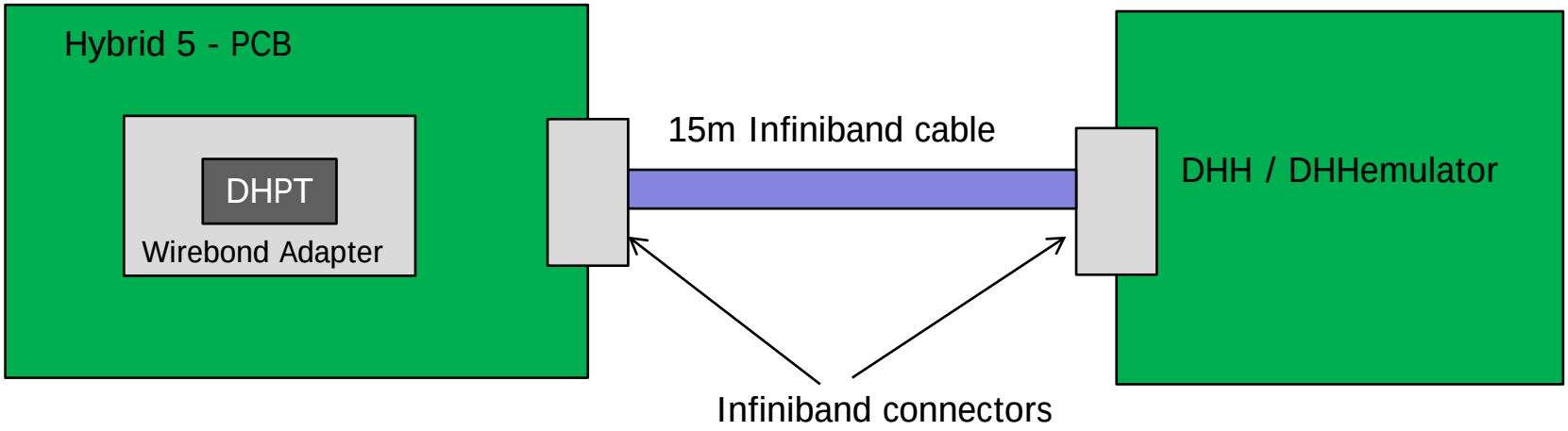
What do we want to learn from the EMCM?

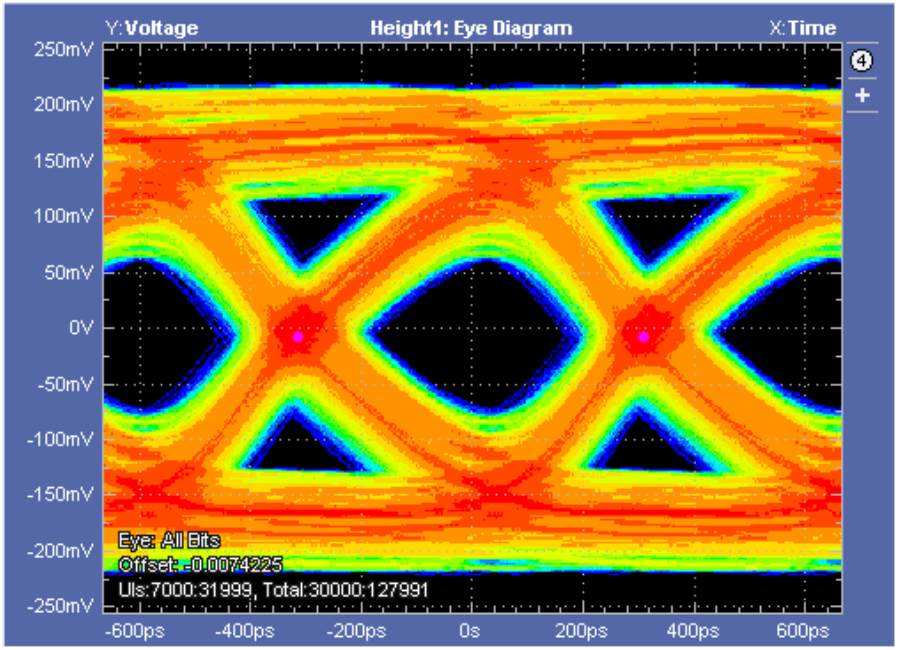
- Stable operation of the 4 high speed links from DHP to DHH



Scan of DHPT output driver parameters of the 4 DHPTs assembled on the EMCM

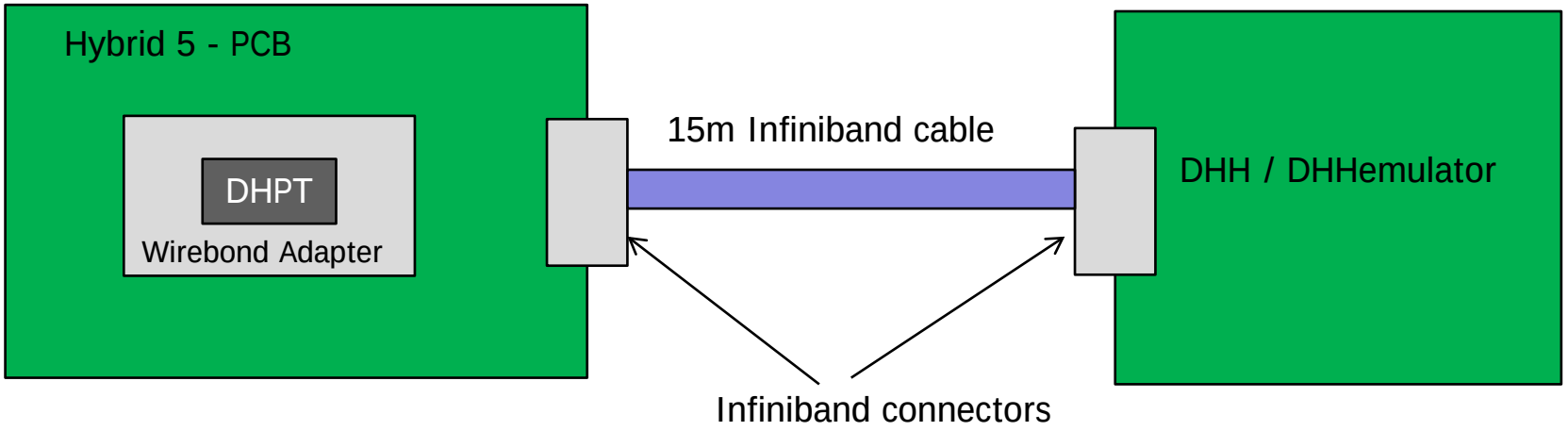
DHPT Output Driver on Hybrid5

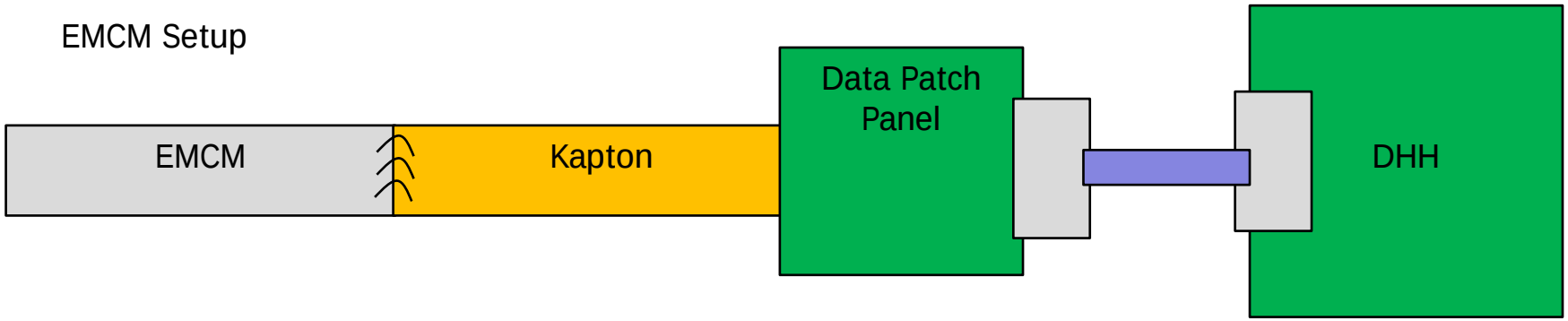




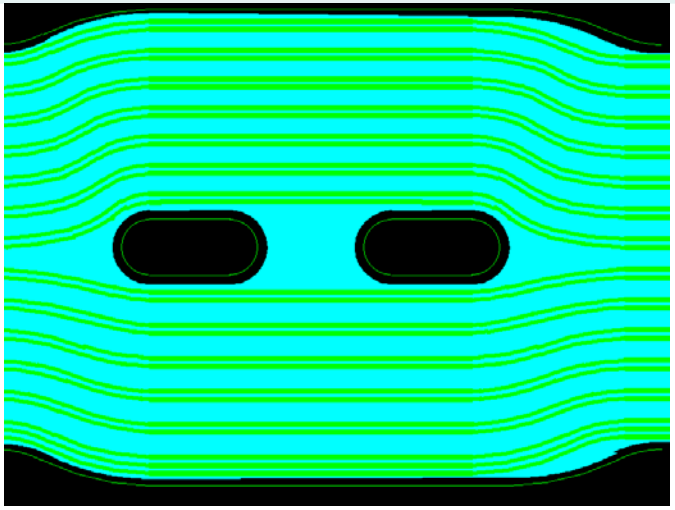
DHPT link tested by Leonard Germic (Uni Bonn) with 15m cable ok!

Difference in the link





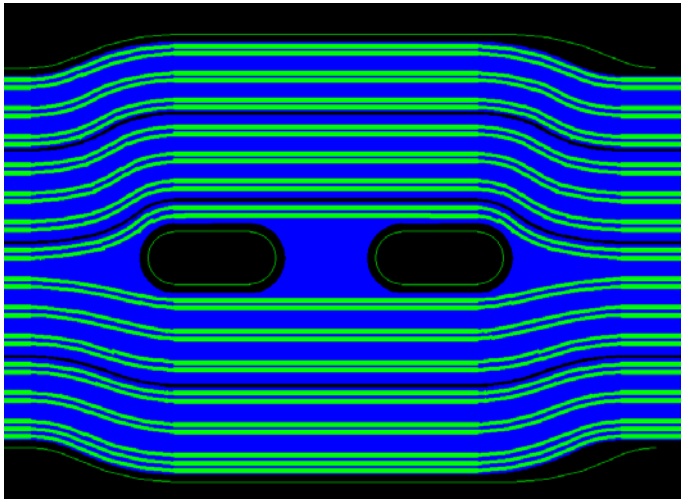
Short Kapton



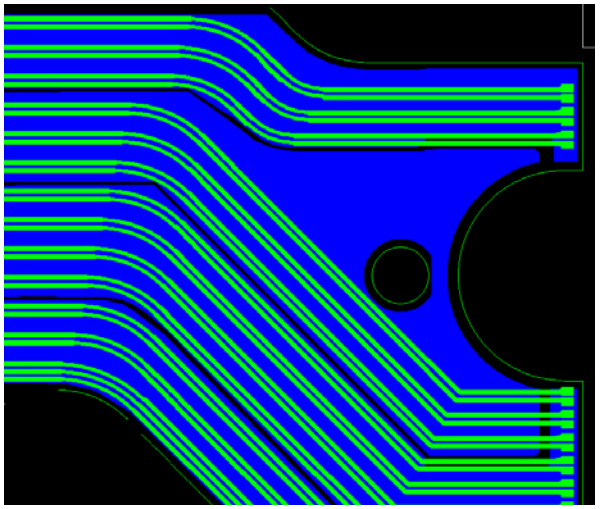
Signal layer vs. layer 2 (no split plane)

- Layout of high speed links better (in terms of impedance control) compared to the long kapton
- Still some lines are too close at the edge

EMCM Testing is system testing!



Signal layer vs. layer 4



What do we want to learn from the EMCM?

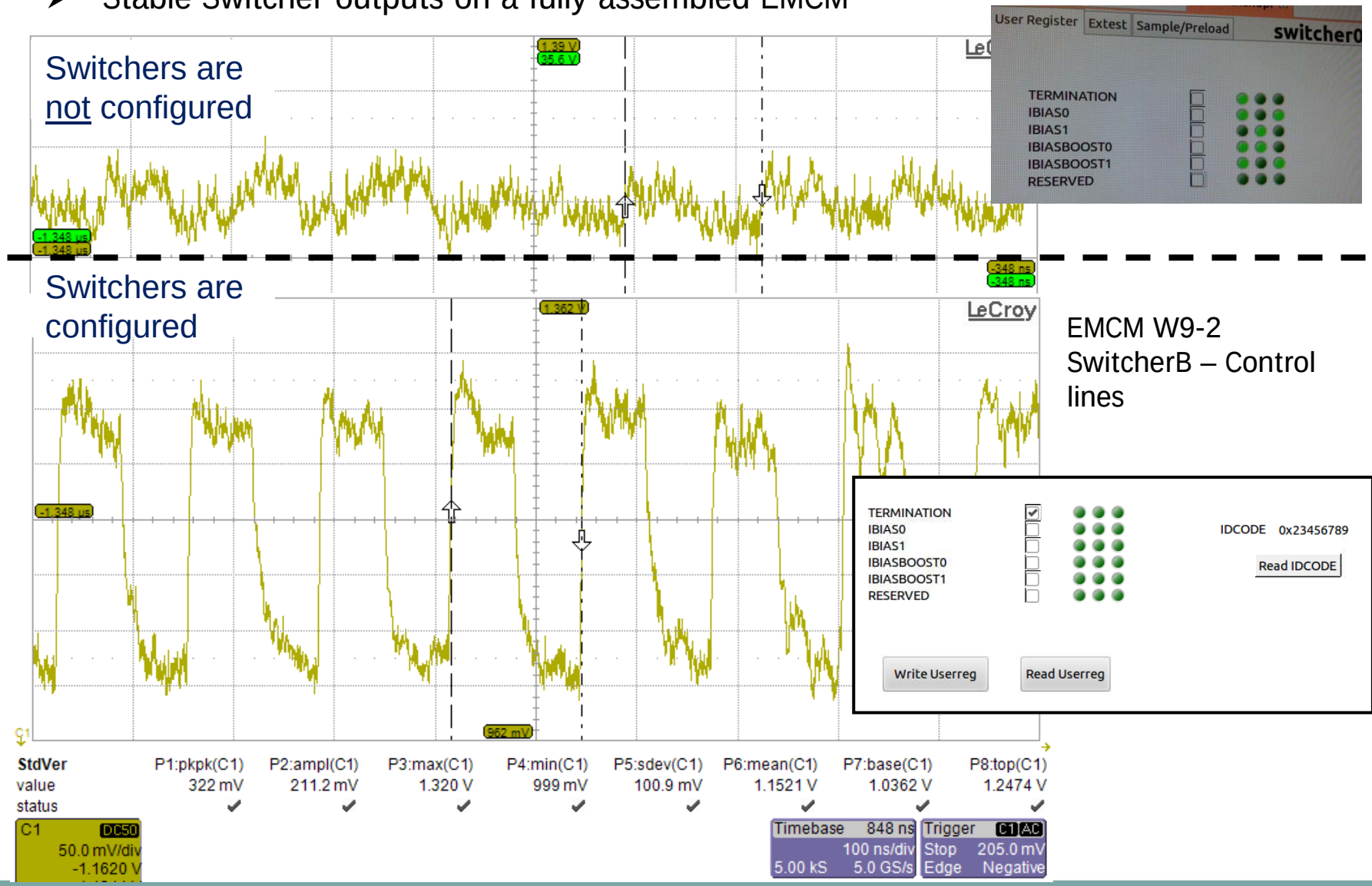
- What do we want to learn from the EMCM?
  - Low noise of all 1000 DCD channels **at 320MHz**

→ New firmware for DHH available which allows the reduction of DHPT data rate to 800Mbit/s (instead of 1.6Gbit/s) while keeping the nominal frequency for DHPT/DCDPipeline

→ To be investigated!

What do we want to learn from the EMCM?

- Stable Switcher outputs on a fully assembled EMCM



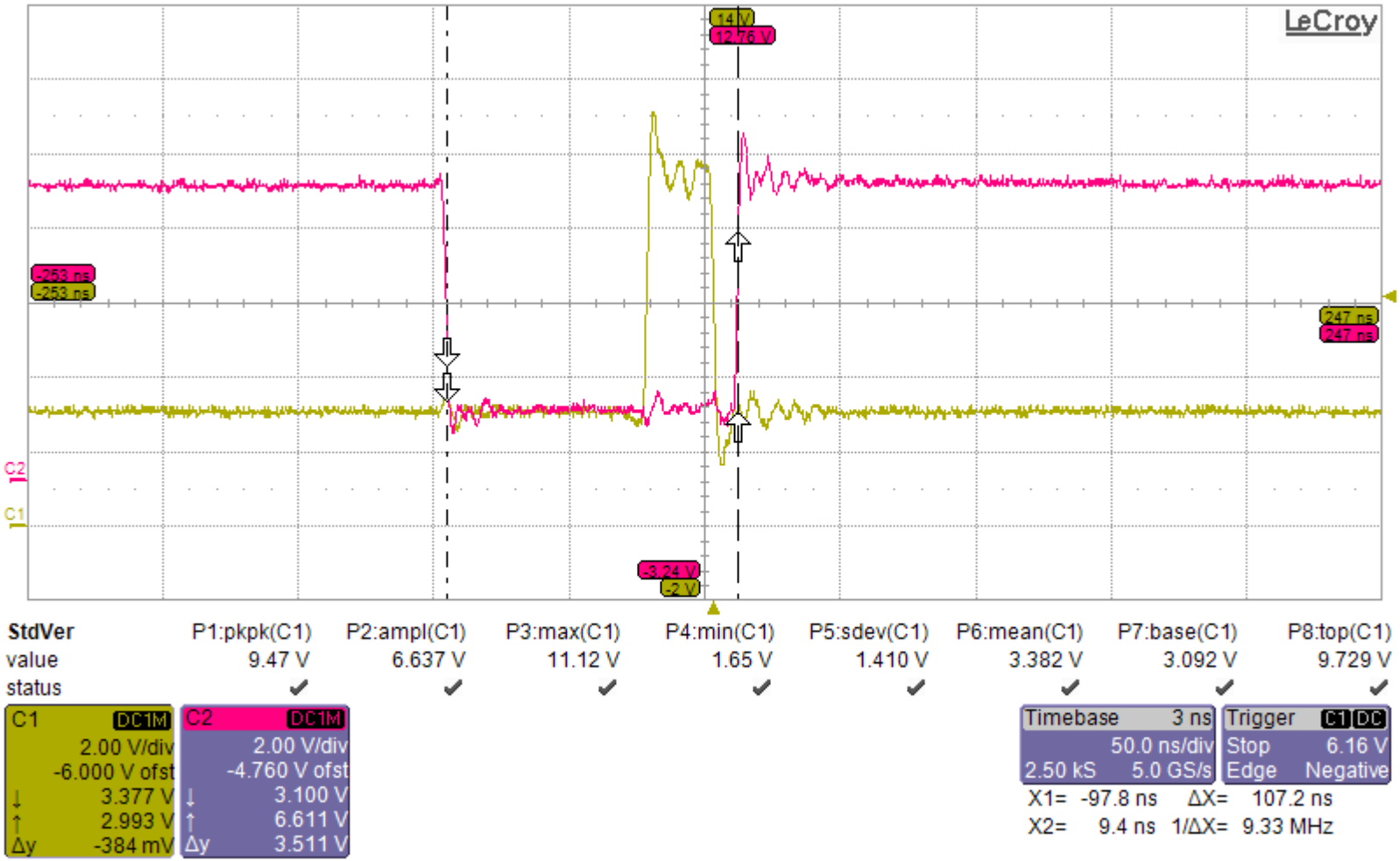
EMCM W9-2
SwitcherB – Control lines

EMCM W9-2 SwitcherB – Gate Outputs

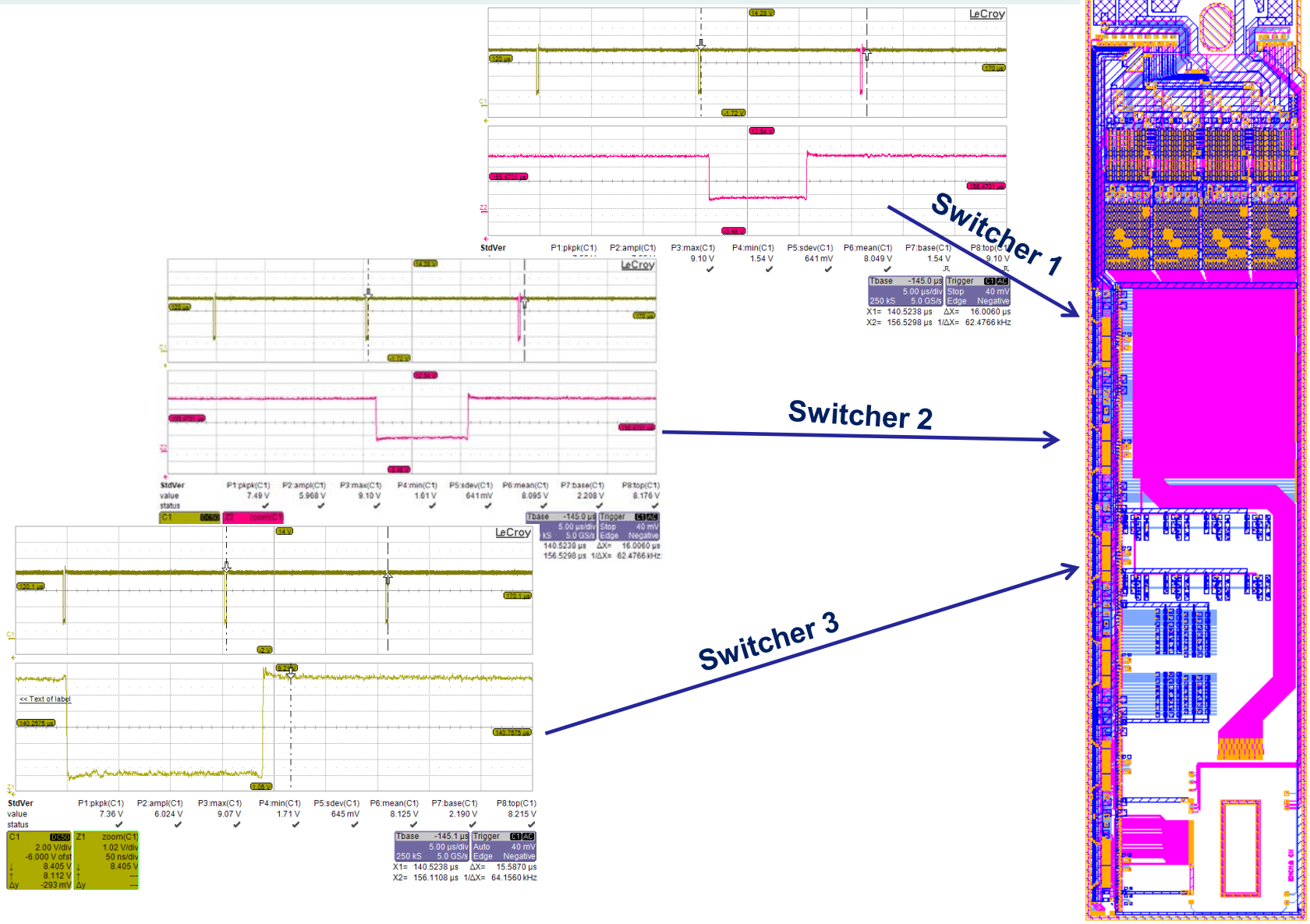
Switcher (5): Output of 3 consecutive Gates (190, 191, 192)

EMCM W9-2 SwitcherB – Gate & Clear Outputs

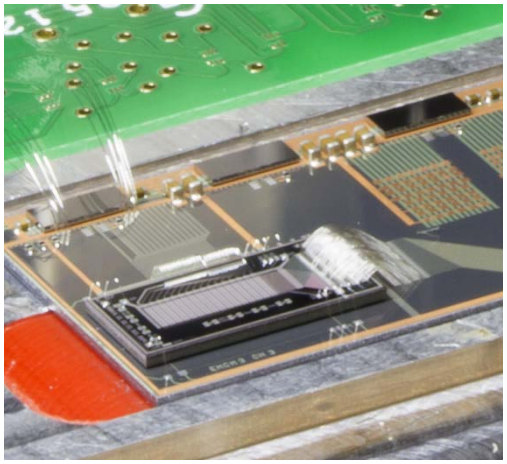
Switcher (5): Output of Gates & Clear, Channel 191

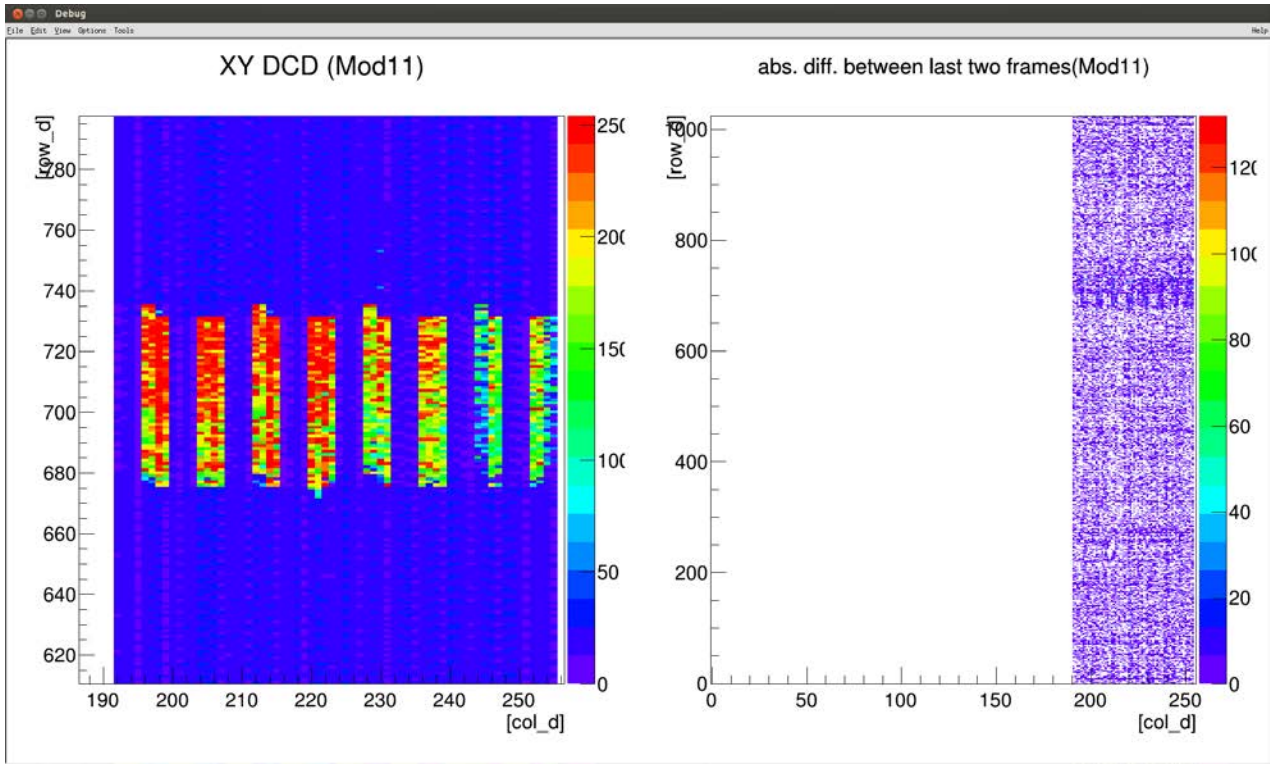


EMCM W9-2 SwitcherB – Gate & Clear Outputs



EMCM3 W18-3 first glimpse on PXD6 matrix



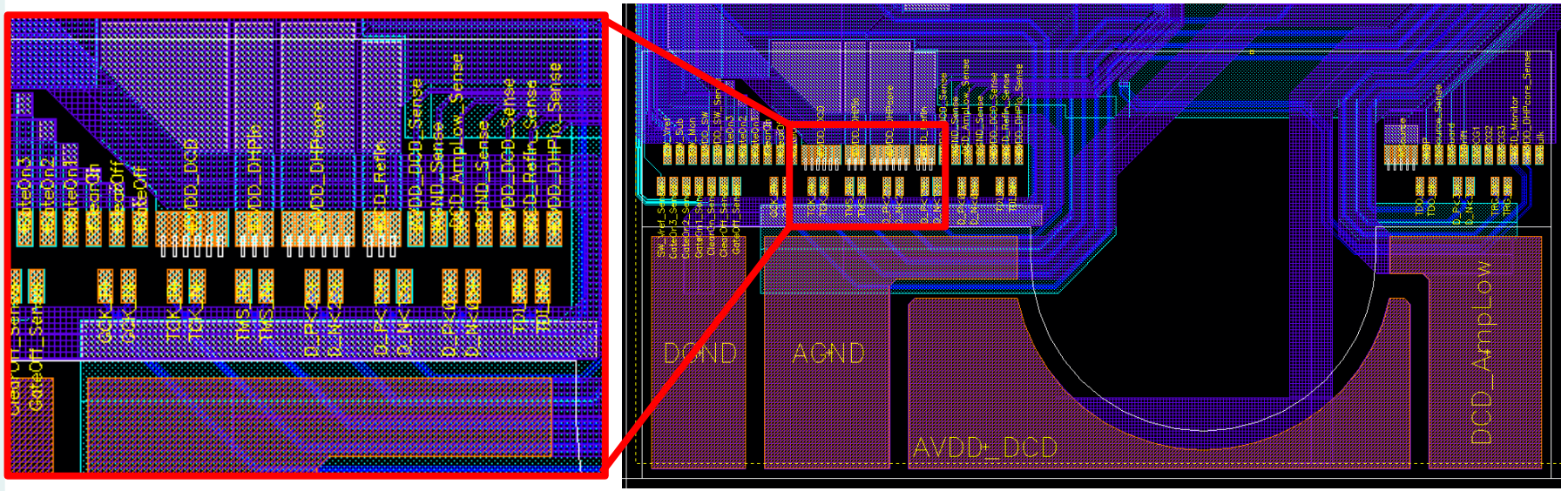


- Very first glimpse on PXD6 standard design, short gate length 4µm (assembled 25th Sept. 2014) read out by DCDPipeline and DHPT @ 305 MHz
- Mapping in Online Monitor must be adapted
- Pedestal distribution, noise, laser and source tests to be done/analyzed

  ... and Gated-Mode

Changes to PXD9 Layout (done by Christian Kreidl)

- Remove not used differential lines (not needed by DHPT anymore)
- Re-size the wirebond pads for several voltages
  - ▷ DHPCore ca. 700mA -> 6bonds = 117mA/bond
  - ▷ DHPIO ca. 220mA -> 3bonds = 73mA/bond
  - ▷ DCD_DVDD ca. 720mA -> 6bonds = 120mA/bond
  - ▷ RefIn ca. 200mA -> 3bonds = 67mA/bond
- Increase trace width of differential lines to 30µm
- Increase spacing of the termination resistors to 200µm
- Increase width of the power routing on copper

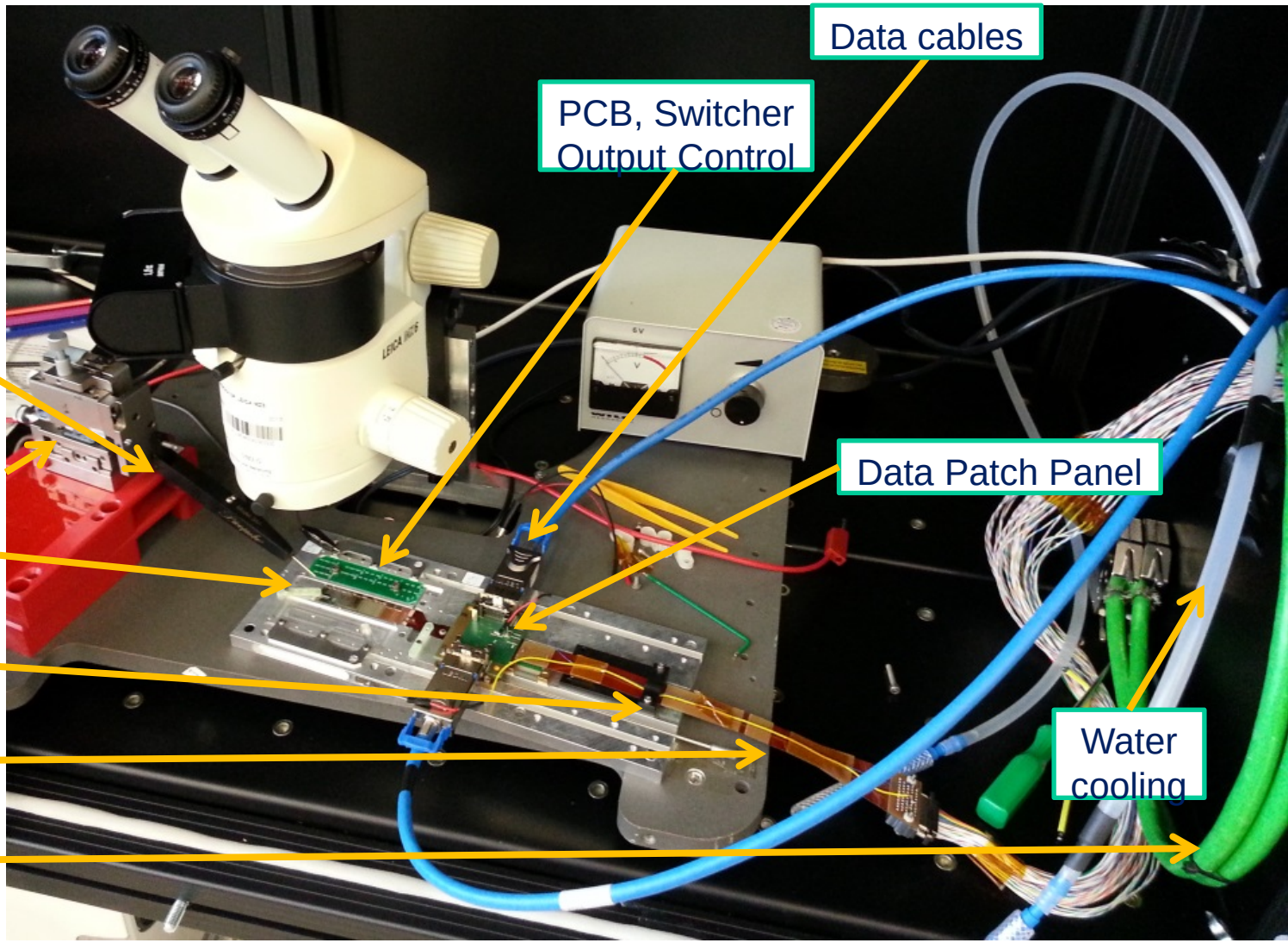


Summary and Next Steps

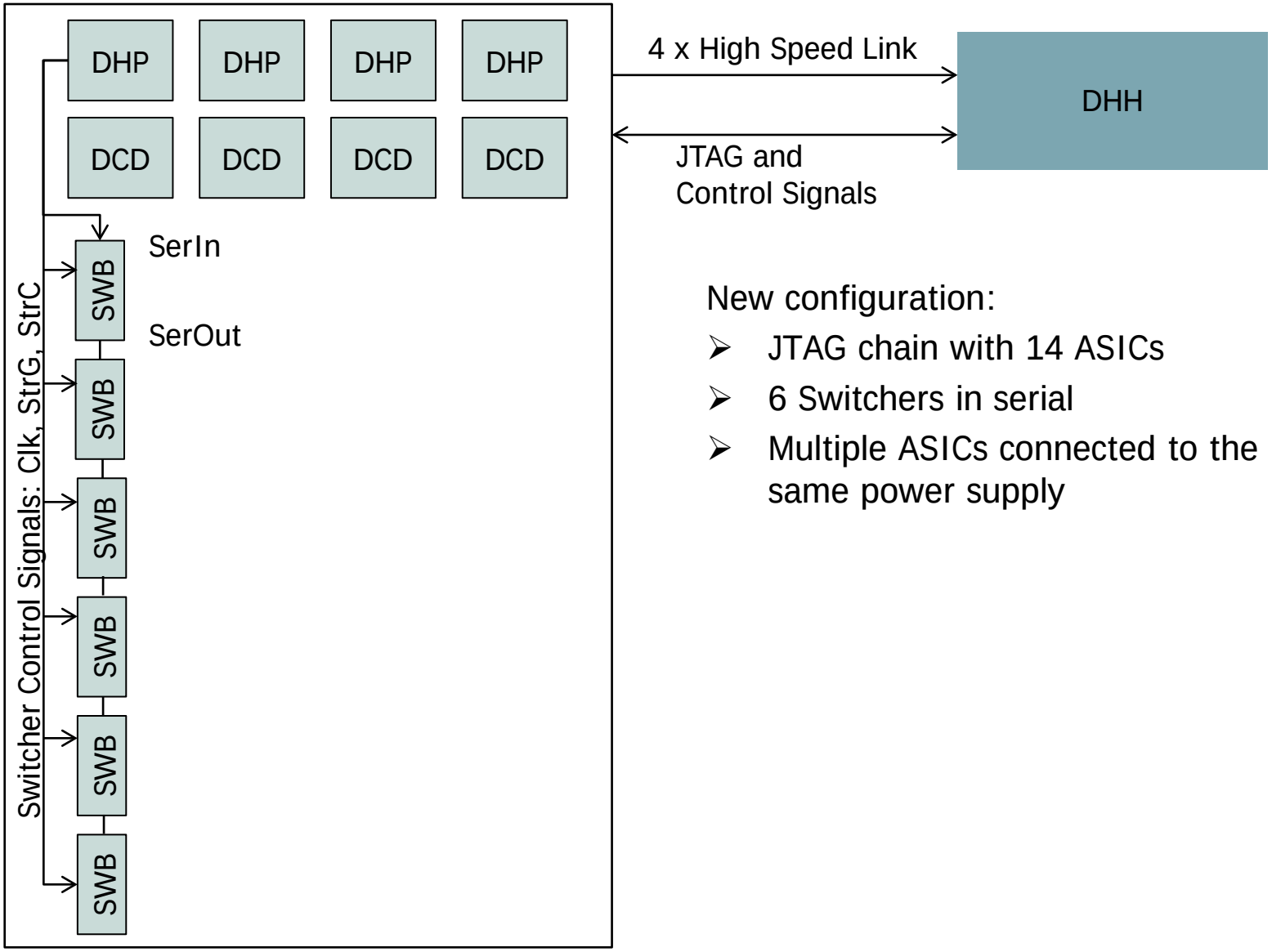
- EMCM4 wafer-level testing to confirm technology
- Studying DCDPipeline performance at full-speed (using new DHH firmware)
- PXD6 matrix on EMCM → mapping of pixel in Online Monitor, pedestal distribution, noise, laser and source tests, gated-mode
- Discussion on the further PXD9 processing ...
  - Start with PXD9 production (2-3 hot wafers) + several metal “only” Wafer (PXD9 layout)
  - Question: When to continue with further PXD9 wafer production?

Thank you for your attention!

Setup


Data cables
PCB, Switcher Output Control
Pico Probe
Micro Manipulator
EMCM
Power Patch Panel
Power cable
LMU Power Cable
Data Patch Panel
Water cooling

Fully Assembled EMCM



New configuration:

- JTAG chain with 14 ASICs
- 6 Switchers in serial
- Multiple ASICs connected to the same power supply

- EMCM W18-3, 3m cable, 250MHz, V_DHP_Core 1.42 V

Aurora Links – DHH0

up
down

250MHz, 3m Infiniband cables, 1.42V, EMCM W18-3