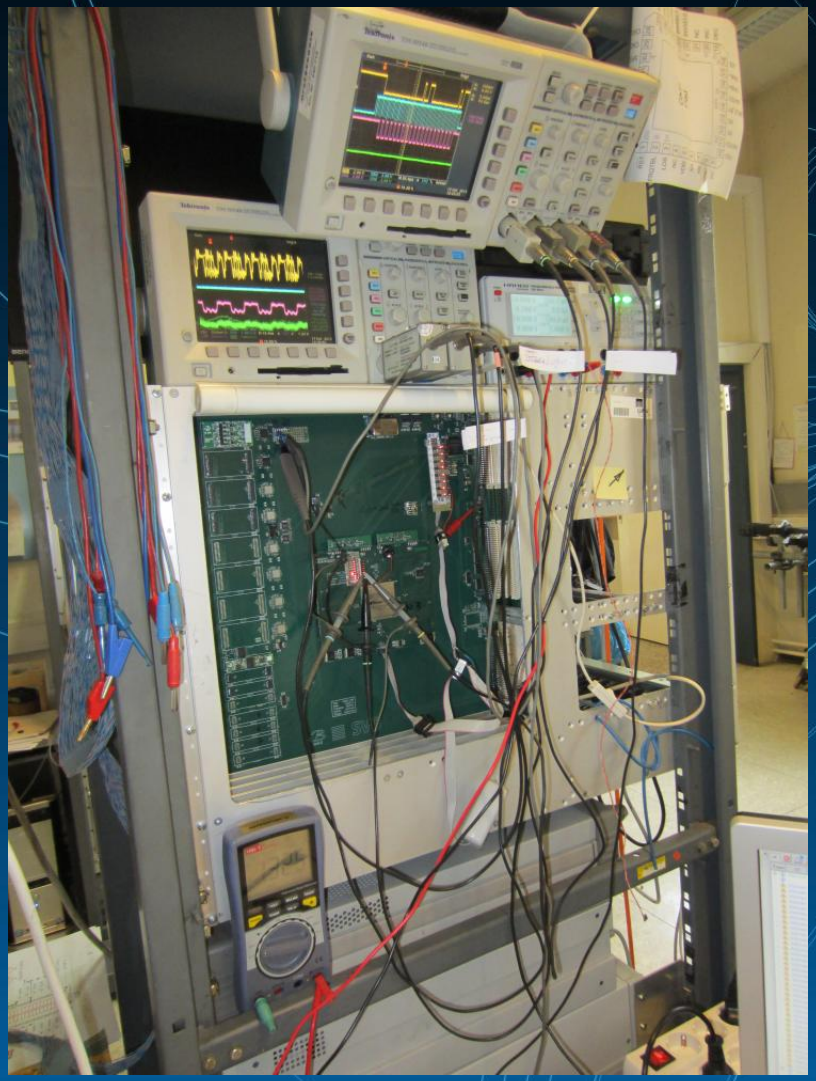
HEPHY Institute of High Energy Physics

OAW Austrian Academy of Sciences

Belle II

SVD



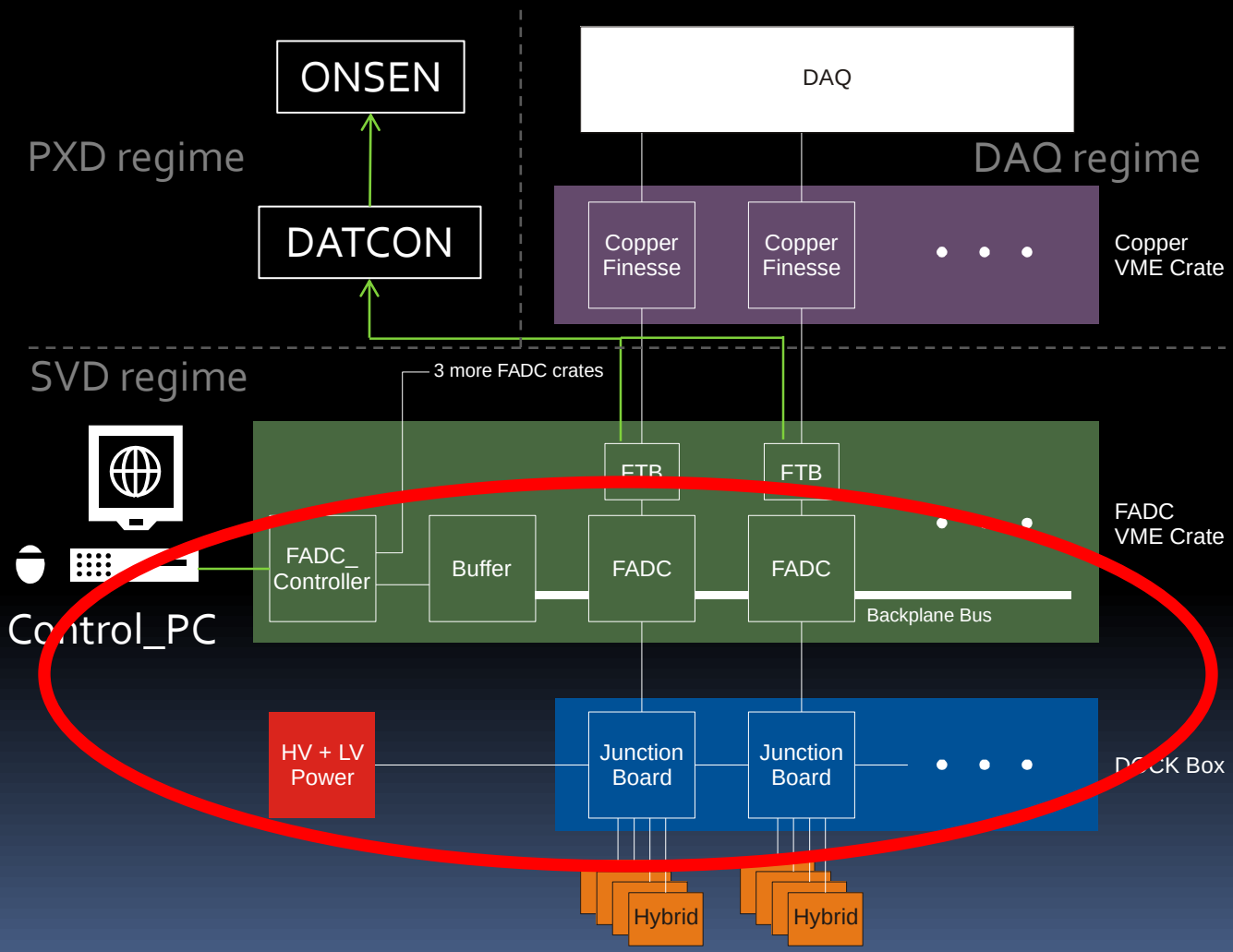
Belle II 6th VXD workshop

2014-10-02

SVD Electronics and Firmware Status and Schedule

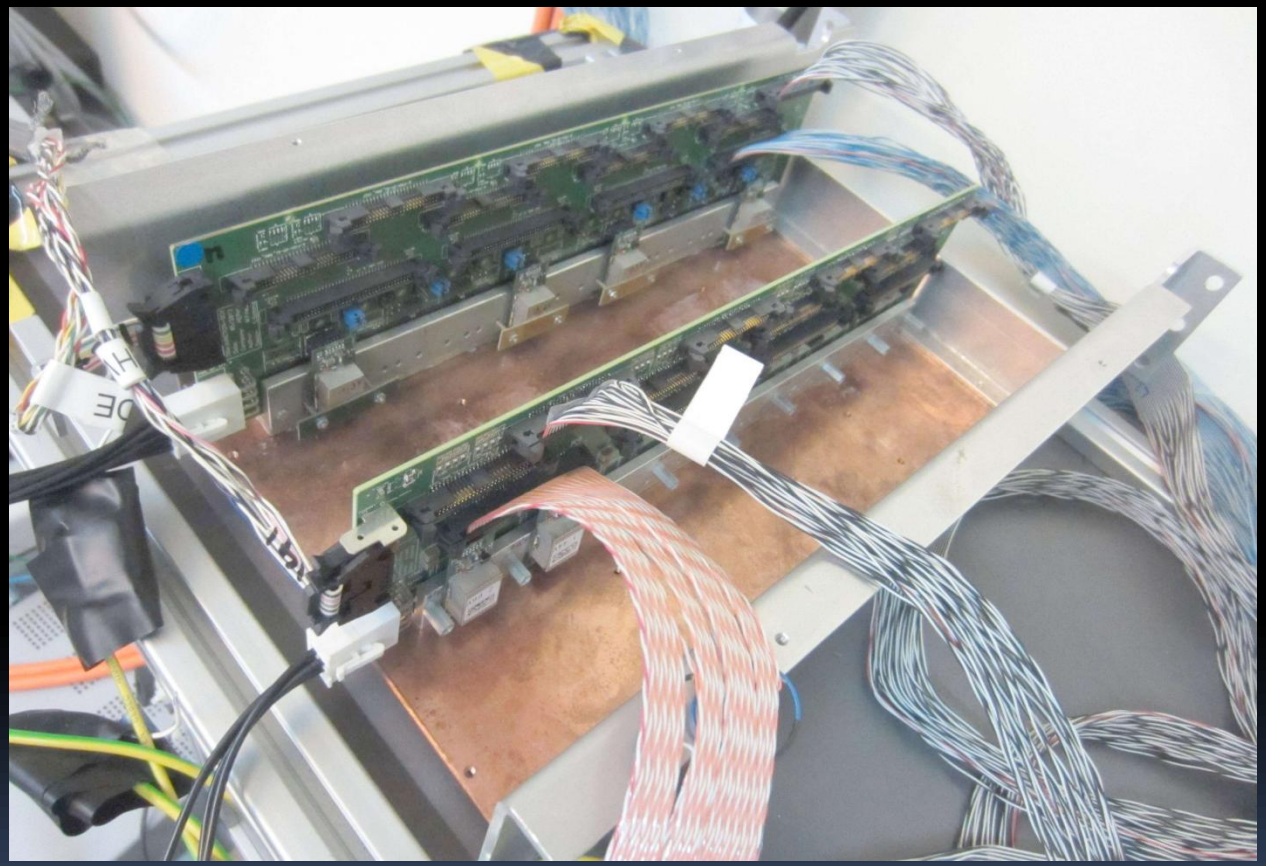
Richard Thalmeier (HEPHY Vienna)

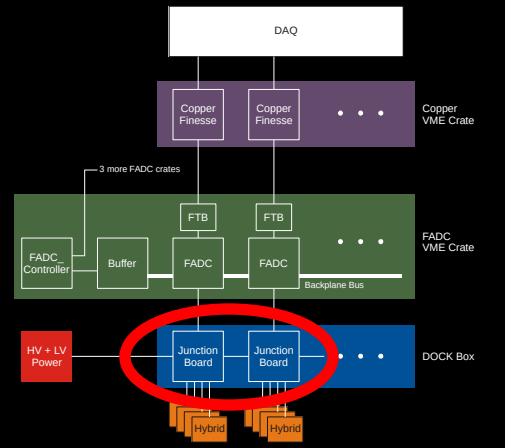
System Overview



- DAQ: PC Farm
- COPPER: common readout platform
- FADC system with optical link to COPPER
- DOCK box with DC/DC
- Front-End

Junction Boards



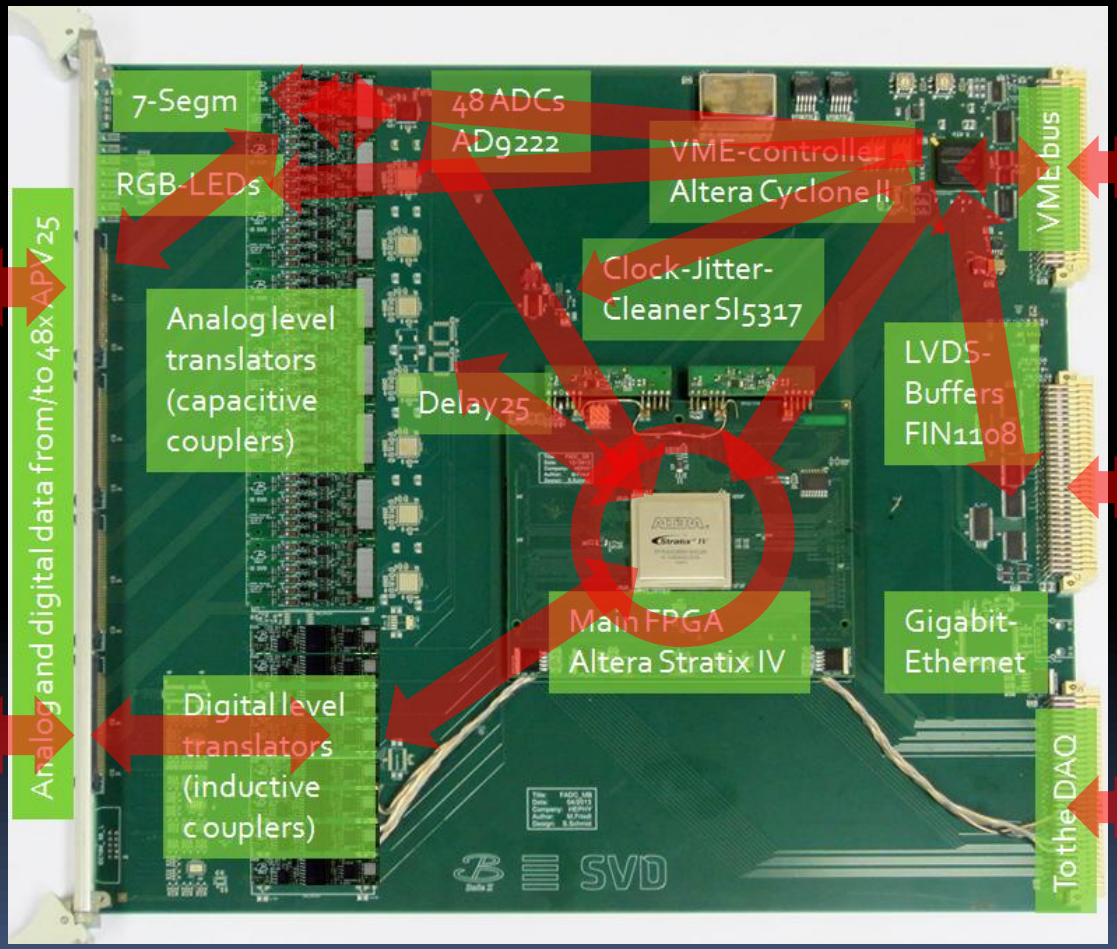


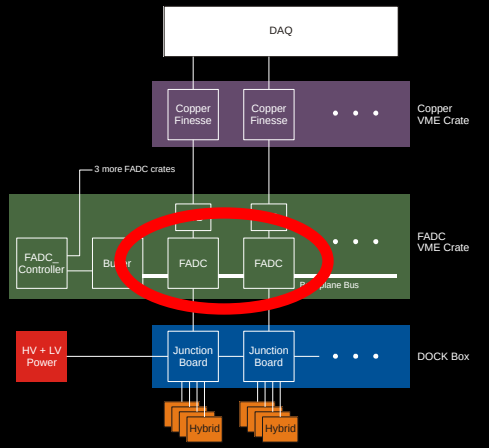
Version 2 Prototypes:
Ready and Tested.

Some of the changes:

- New DC/DC-Converters (rad-hard, from Cern)
- Temperature Sensors (read out by the FADCs)
- DC/DC-Enables and Power-Good-Readout

FADC V1 – Status

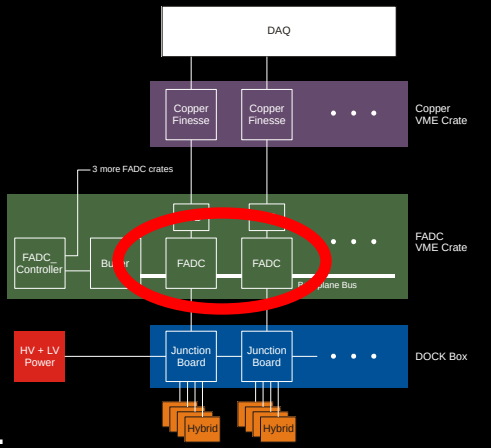




- VME-bus-interface in the Cyclone
- Communication Cyclone ⇔ Stratix (Serial LVDS)
- Protocols VME ⇔ Cyclone ⇔ Stratix
- 7-Segment-Display (SPI-interface)
- RGB-LEDs (SPI-interface)
- Delay25 (I^2C-interface)
- Readout of the 48 ADCs (Serial LVDS interface)
- APV25 configuration (I^2C-interface)
- reading out realtime APVdata to VME
- Reordering of the APV25 data
- CRC16 calculation
- Common Mode Correction
- Zero Suppression
- Pedestal Control
- Data Output Formatting
- U, I, ϑ, PowerGood-, … – Monitoring

Everything is implemented and tested, except of…

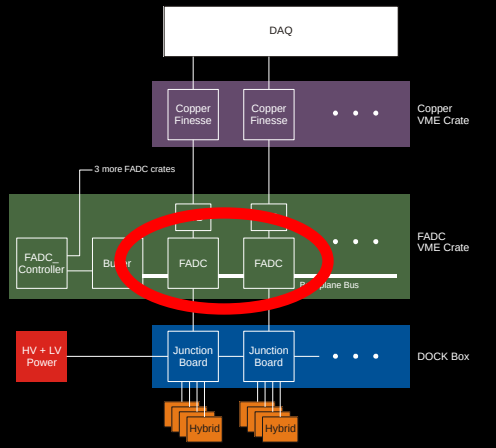
FADC V1 – Firmware Status



Not done yet:

- **Hit Time finding.**
  - The concept and some research is done (neuronal networks).
  - The implementation into the configuration software (as well as the parameter finding system) is in progress right now (Hao Yin).
  - If the FADC Firmware adaption and Hardware debuggings of FADC V2 do not provide any problems, maybe I have the time to implement the Hit Time Finding into the FADC-Firmware before the November Beamtest.

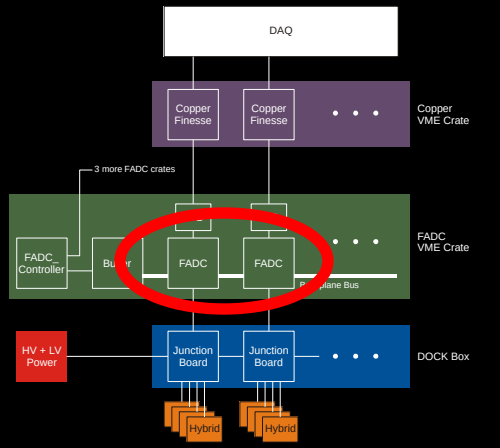
FADC V1 – Firmware Status



Not done yet:

- **Hit Time finding.**
- **FADC-Controller-FPGA-Flashing confuses the FADCs.**
  - The Clock for the FADC comes from the FADC Controller.
    When the FADC-Controller-FPGAs are flashed while the FADC is running, the High-Speed-Serial-Connection between the two FPGAs on the FADC seems to get killed permanently until a re-flash of the FADC-FPGAs.
  - Possible workaround: reset-circuit for the cyclone on FADC Hardware V2 for reprogramming from eeprom (for example by watchdog, or by VME command).
  - Not relevant for Beamtest, cause we can flash them in the right order via jtag).

FADC V1 – Firmware Status

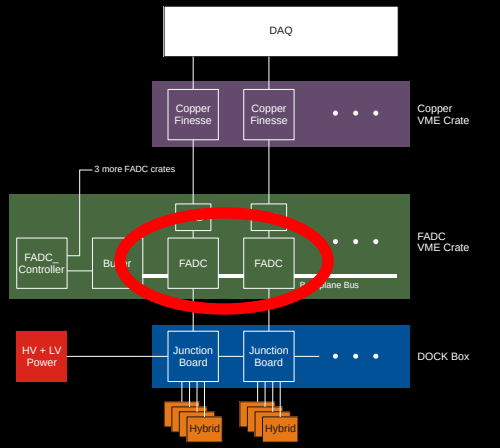


Not done yet:

- **Hit Time finding.**
- **FADC-Controller-FPGA-Flashing confuses the FADCs.**
- **Gigabit Ethernet.**

  I tried extensively to get it running without the Quartus "Nios II" processor (on which all other implementations I found rely on), but did not get some valid response from a connected PC running wireshark…
  Not relevant for november beamtest, cause its not used yet.
  I will try again later, but probably with "Nios" CPU, which could fit into the new stratix which we get in January 2015.

FADC V1 – Firmware Status

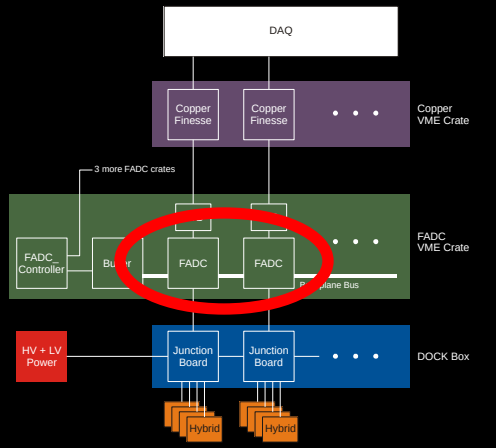


Not done yet:

- **Hit Time finding.**
- **FADC-Controller-FPGA-Flashing confuses the FADCs.**
- **Gigabit Ethernet.**
- **Flashing of the Stratix** via fast-passive-parallel-x8 by VME via Cyclone.

I implemented several different approaches using Single- and Blockread, and extensively tested them e.g. with signaltap and oscilloscopes; it should work on my opinion, but it terminates with a CRC-error-signal after a fixed size of up to several hundred kbytes depending on the firmware binary...
Also not relevant for the November Beamtest, cause we can flash them via JTAG.
Probably there is just some very minor thing wrong... binary-file-generating/conversion-flag, or something like that, but I am out of luck yet getting the right combination...

FADC V1 – Firmware Status



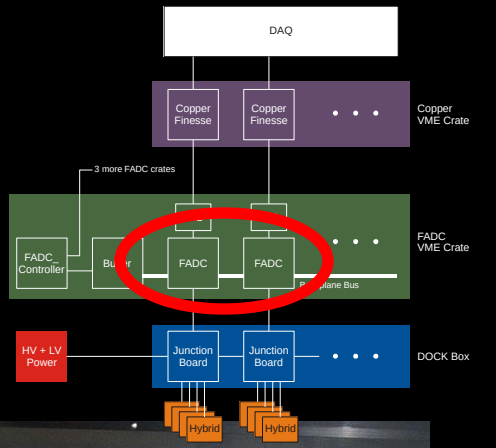
Not done yet:

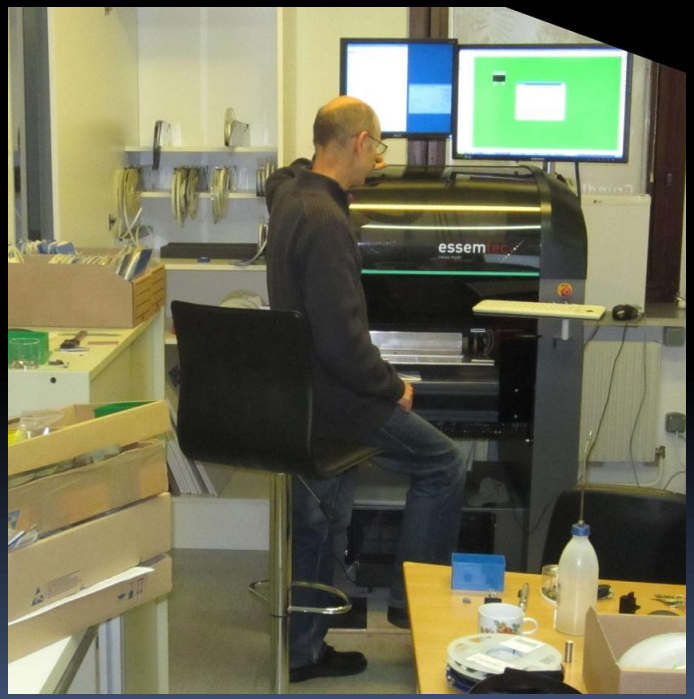
- **Hit Time finding.**
- **FADC-Controller-FPGA-Flashing confuses the FADCs.**
- **Gigabit Ethernet.**
- **Flashing of the Stratix** via fast-passive-parallel-x8 by VME via Cyclone.

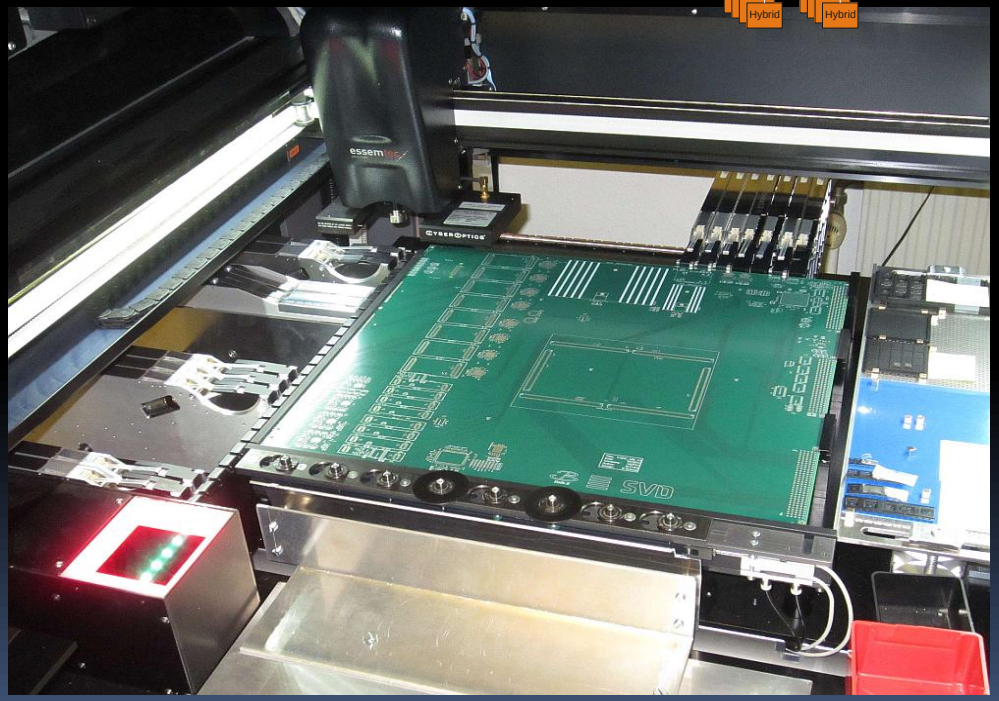
My problem with the latter two is that there are closed-source-IPs ("black boxes") involved; there are lots of possible combinations of various parameters, and they is not really any useful documentation…

FADC V2 – Hardware Status

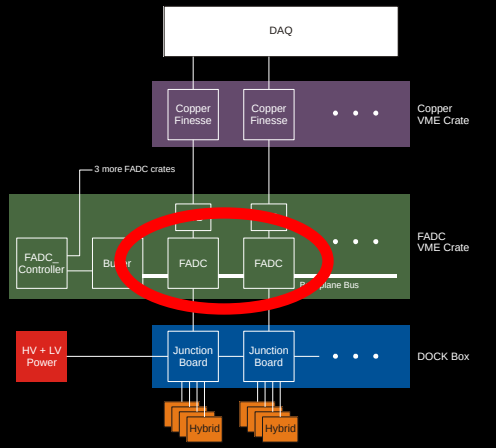
- The new FADC V2 Hardware is hopefully available right after this meeting; Josef is populating the boards right now.







FADC V2 – Hardware Status

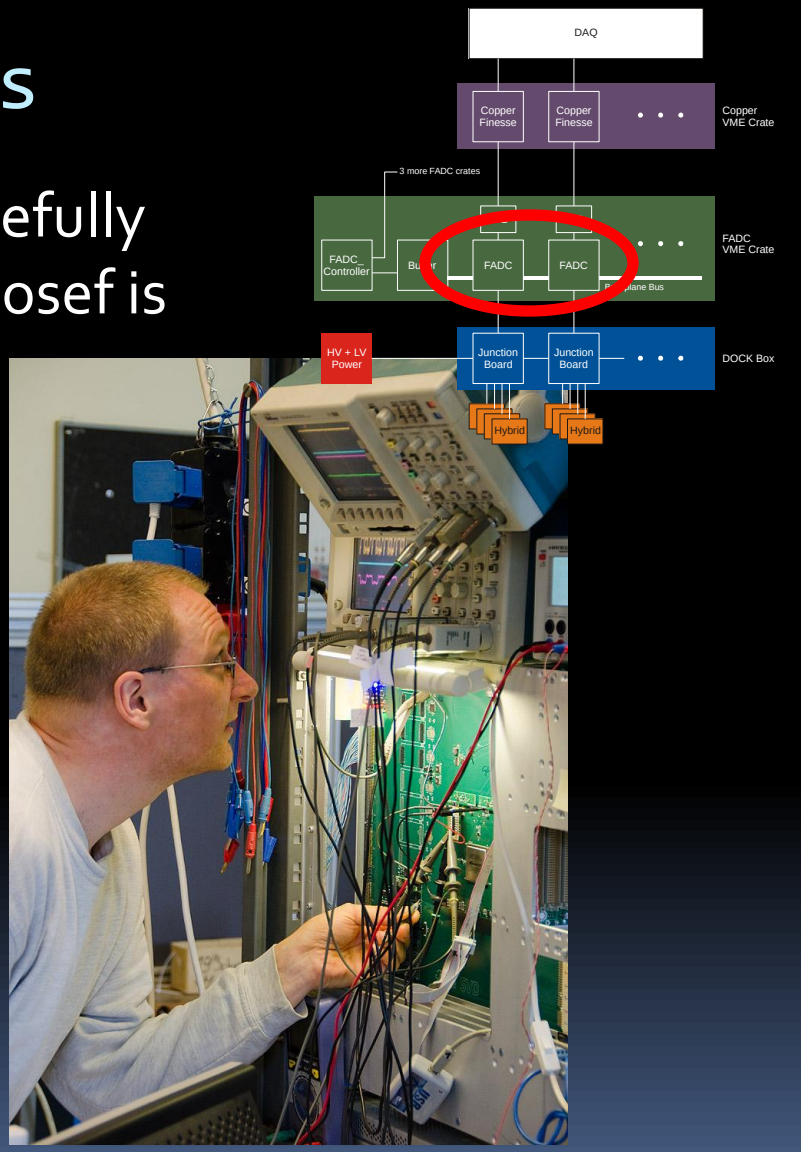


- The new FADC V2 Hardware is hopefully available right after this meeting; Josef is populating the boards right now.
- Lots of Hardware Changes.

  Some examples:
  - Component optimizations (Rs, Cs, ADCs, ….)
  - Cyclone-Self-Reset-Circuit
  - New JTAG connection system
  - Vastly improved ADC voltage support
  - APV Voltage Offset between HV and APV_GND
  - Changed a lot of the Cyclone-pinouts to fit the new connections
  - And of course fixing of all bugs found in FADC V1

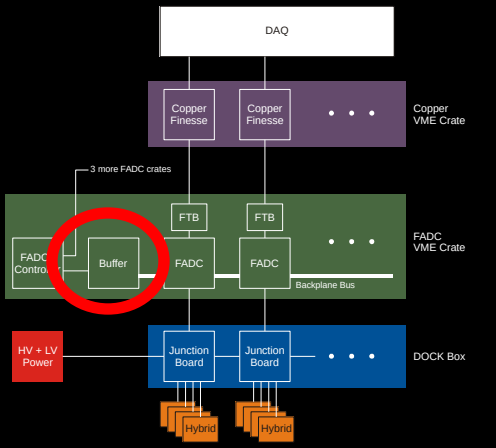
FADC V2 – Hardware Status

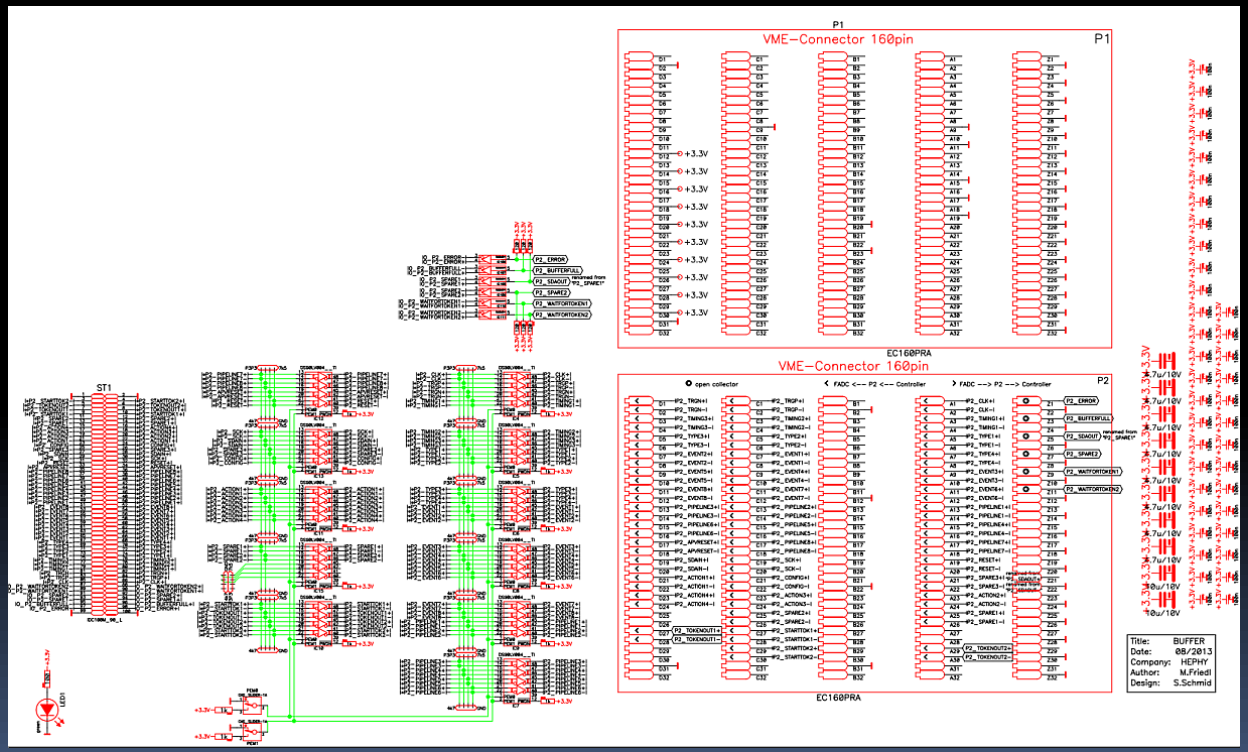
- The new FADC V2 Hardware is hopefully available right after this meeting; Josef is populating the boards right now.
- Lots of Hardware Changes.
- ToDo: Firmware adaption and Hardware/Firmware testing. Will be done right after this workshop.



Buffer Boards

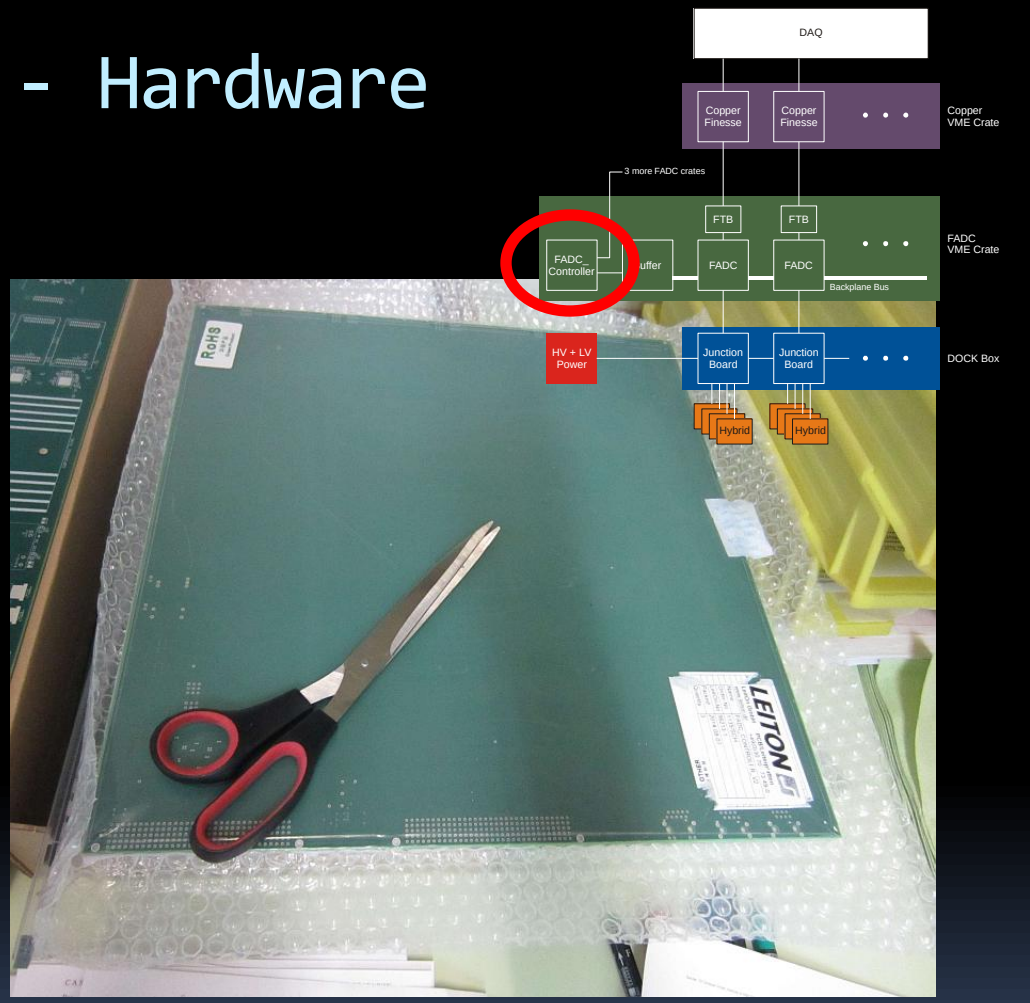
- Tested and OK.
- No changes from last version.



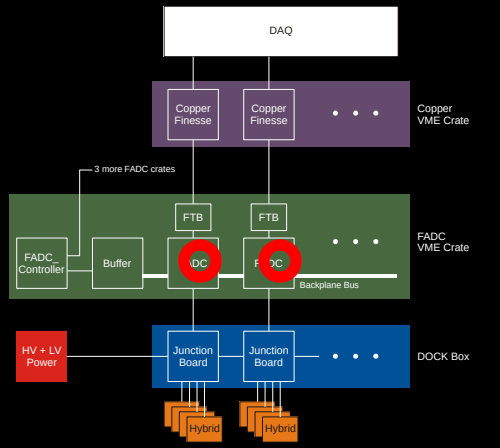


FADC-Controller V2 - Hardware

- The PCB is at Hephy
- Will be readily populated and tested until November Beamtest
- Some of the Hardware changes:
  - Jitter cleaner removed
  - Delay25 added at the NIM connectors
  - Cyclone-self-reset-circuit
  - Complete rework of the passive components



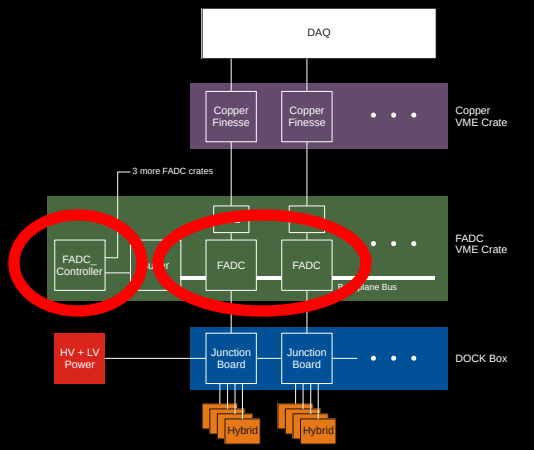
Stratix IV Daughterboards V2



- Only minor modifications
  - Upgrade from Stratix IV GX 180 to Stratix IV GX 360 (pin compatible)
  - EEPROM with higher capacity to fit the new Stratix
  - Stratix-configuration-data-source (JTAG, fast-passive-parallel) is now controllable via cyclone (msel-pins connected to cyclone via buffer IC)
  - Rework of the passive components (e.g. 0402 => 0603)
  - JTAG-connector to the mainboard (and from there to the front panel)
- FPGAs are ordered, they shall be delivered in January 2015

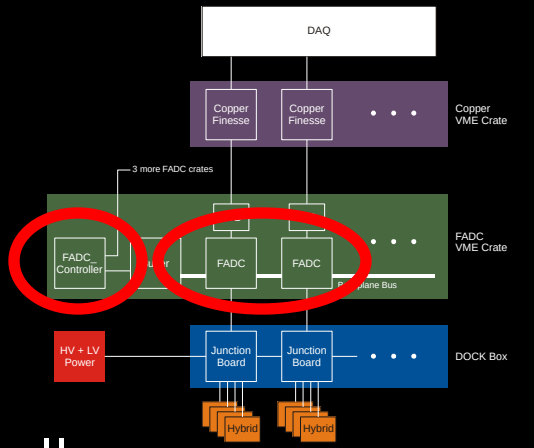
Component Testing Systems

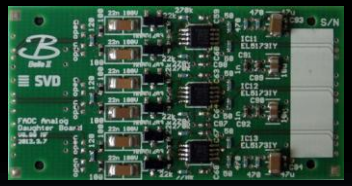
- Special test board derived from the FADC mainboard is under development



Component Testing System

- Special test board derived from the FADC mainboard is under development
- The system shall be able to check the functionality of each daughter board individually



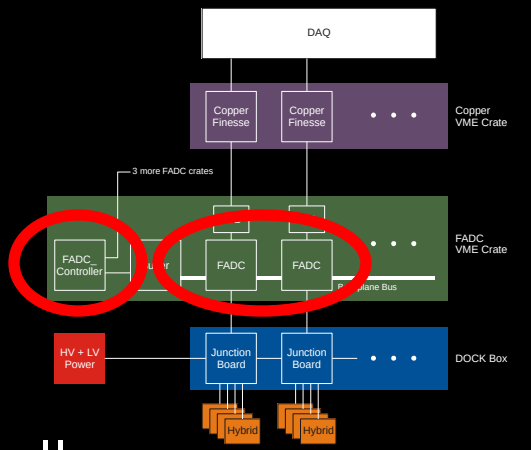


Analog Daughterboards

Digital Daughterboards

Stratix Daughterboards

Component Testing Systems



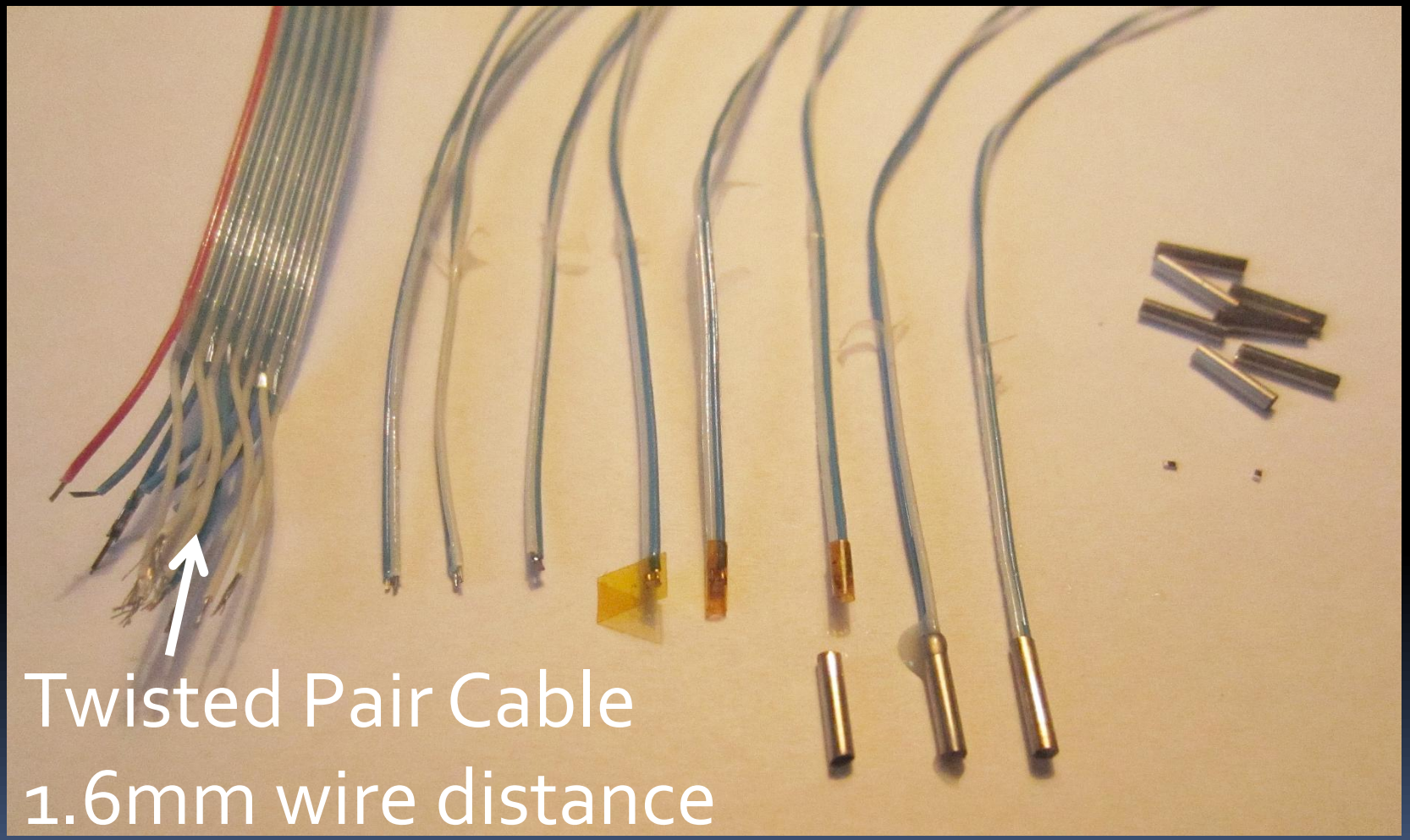
- Special test board derived from the FADC mainboard is under development
- The system shall be able to check the functionality of each daughter board individually
- Examples:
  - Checking of the electrical function and the HV isolation for analog and digital daughterboards
  - Socket for an FPGA-Daughterboard to test all used I/Os

SVD Temperature Sensors

Requirements:

- NTC with 100kΩ
- Length: max. 15mm
- Diameter: max. 1.6mm
- Connected to the twisted flat cable (= hybrid cable), if possible without additional connectors
- Mechanically protected
- Electrically insulated
- Radiation hard

SVD Temperature Sensors (first prototype)



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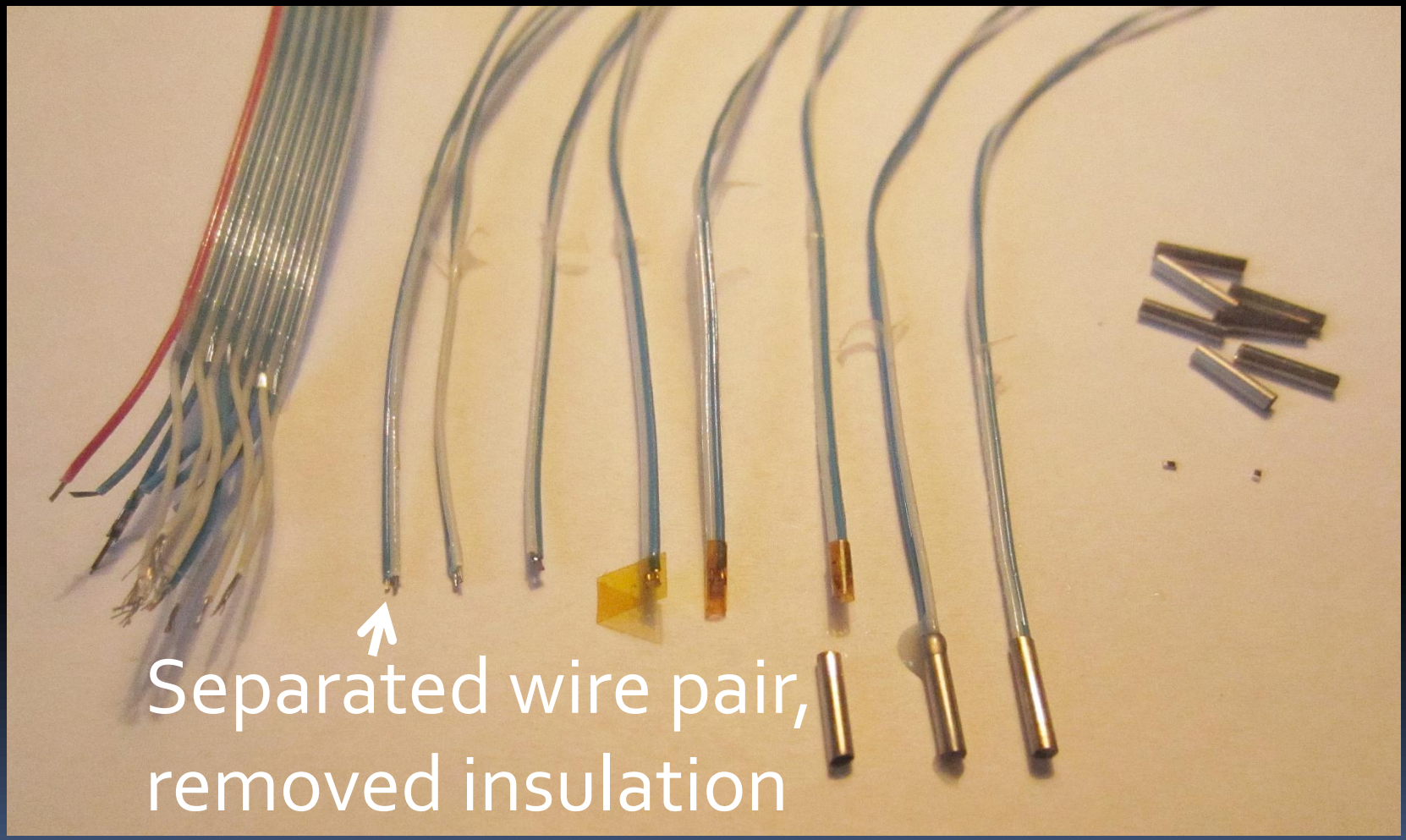

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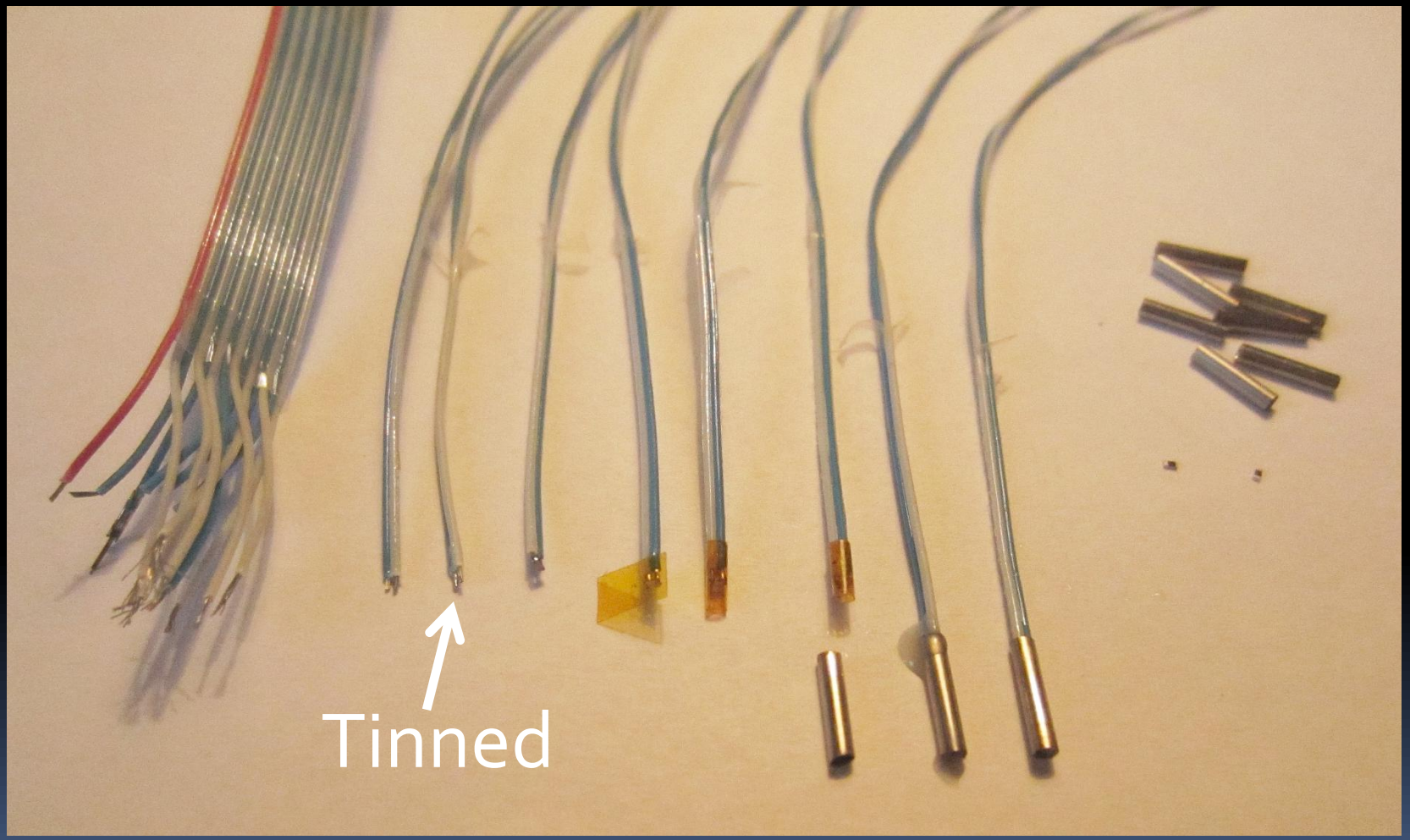

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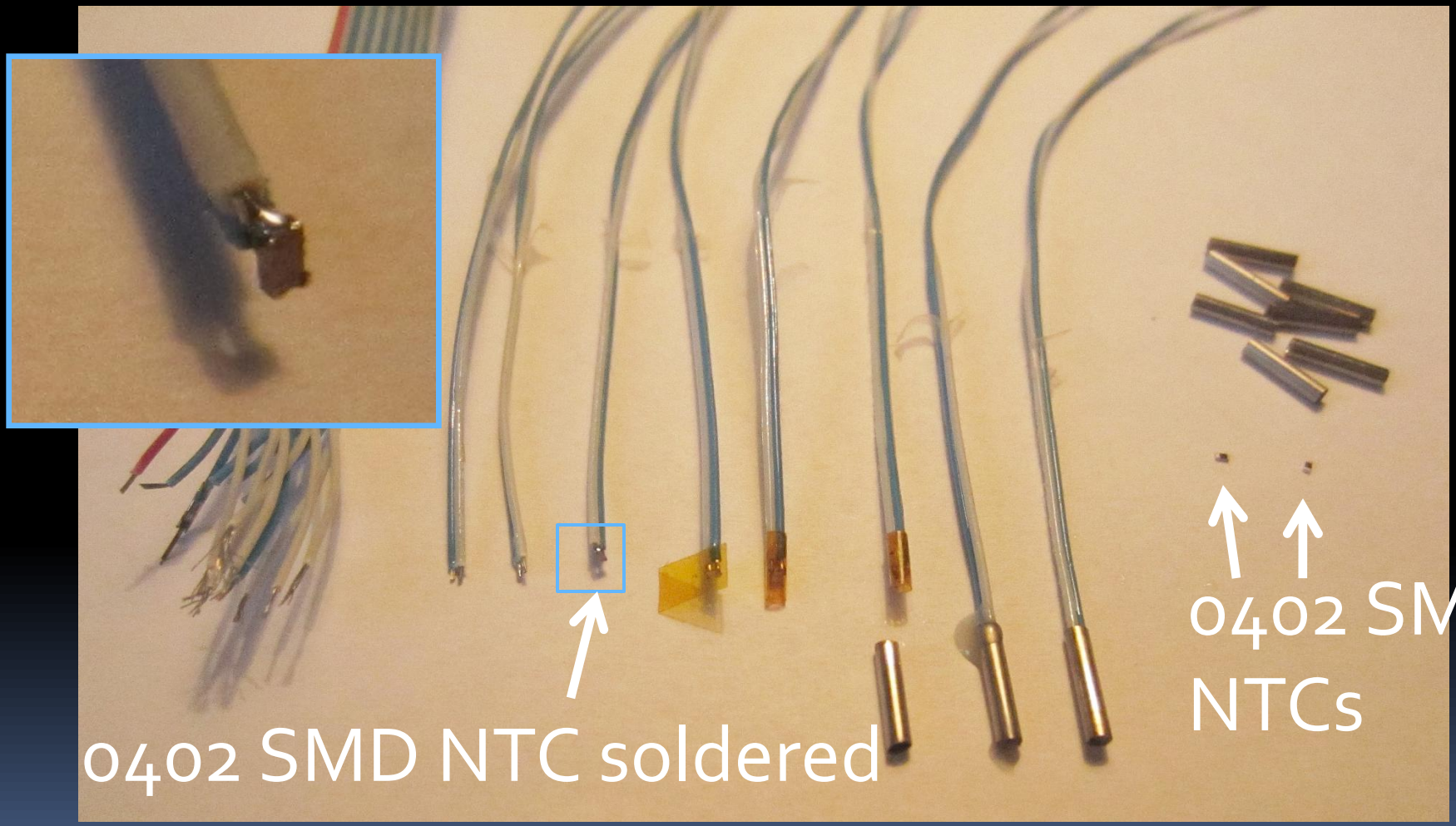

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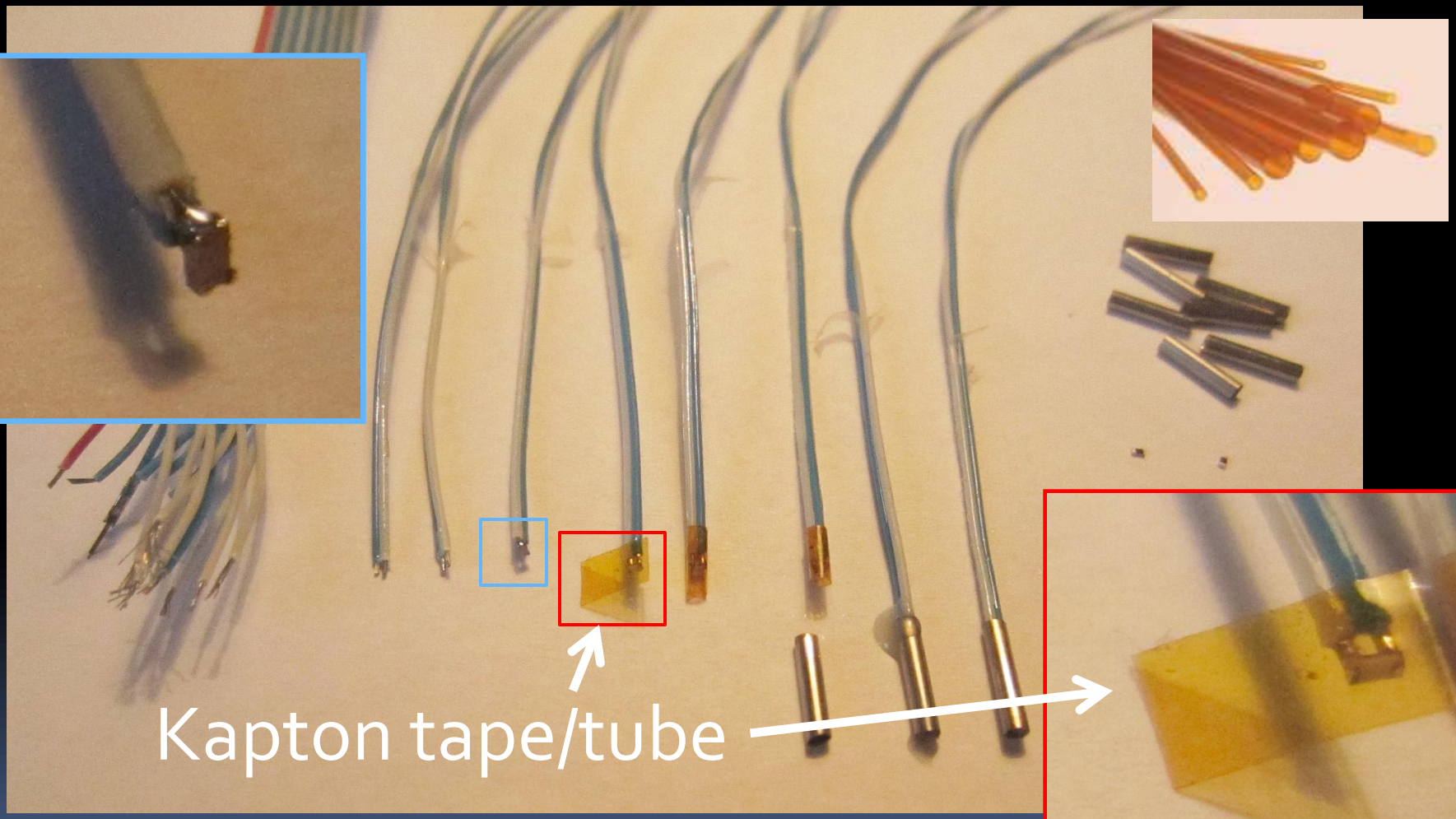

SVD Temperature Sensors (first prototype)

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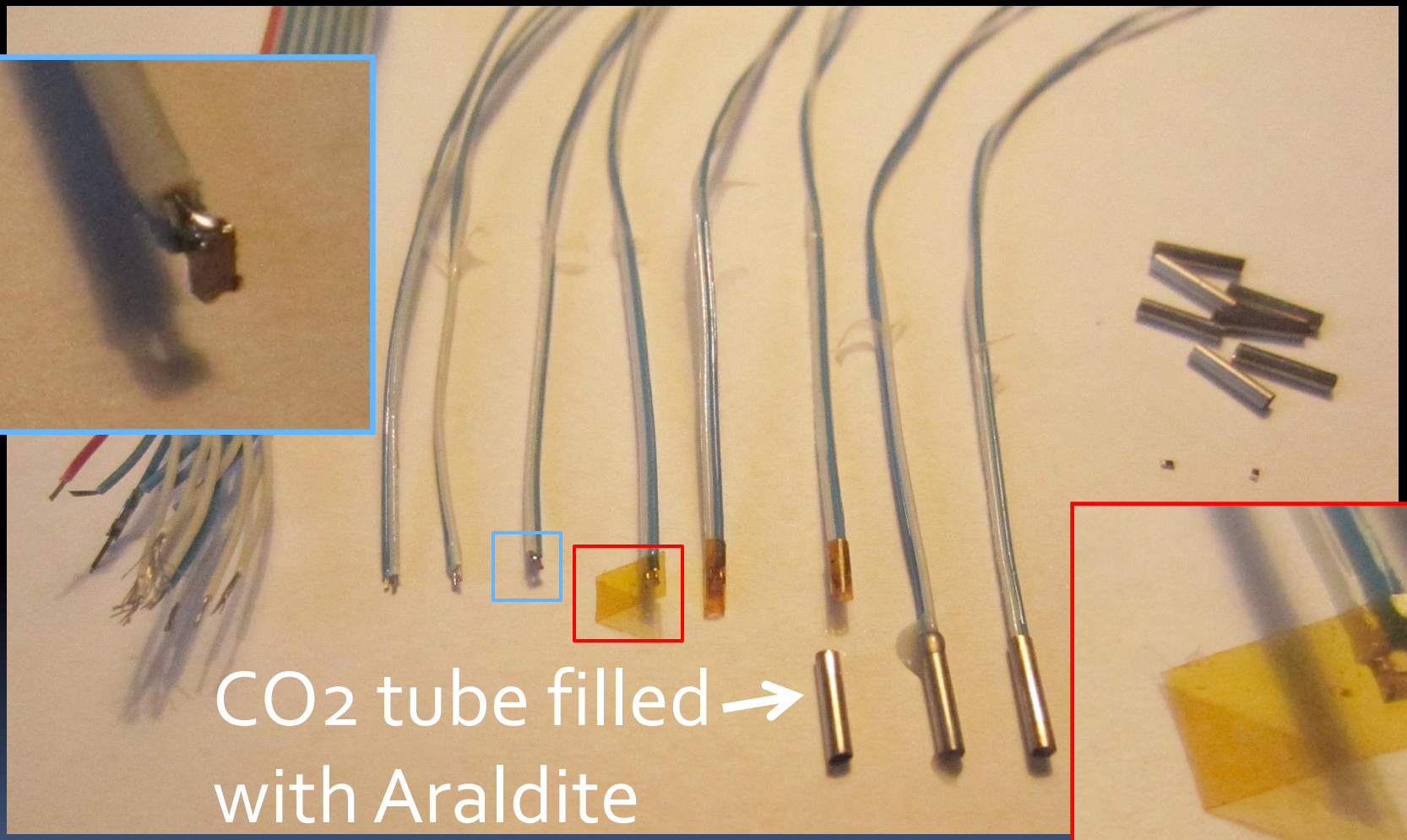

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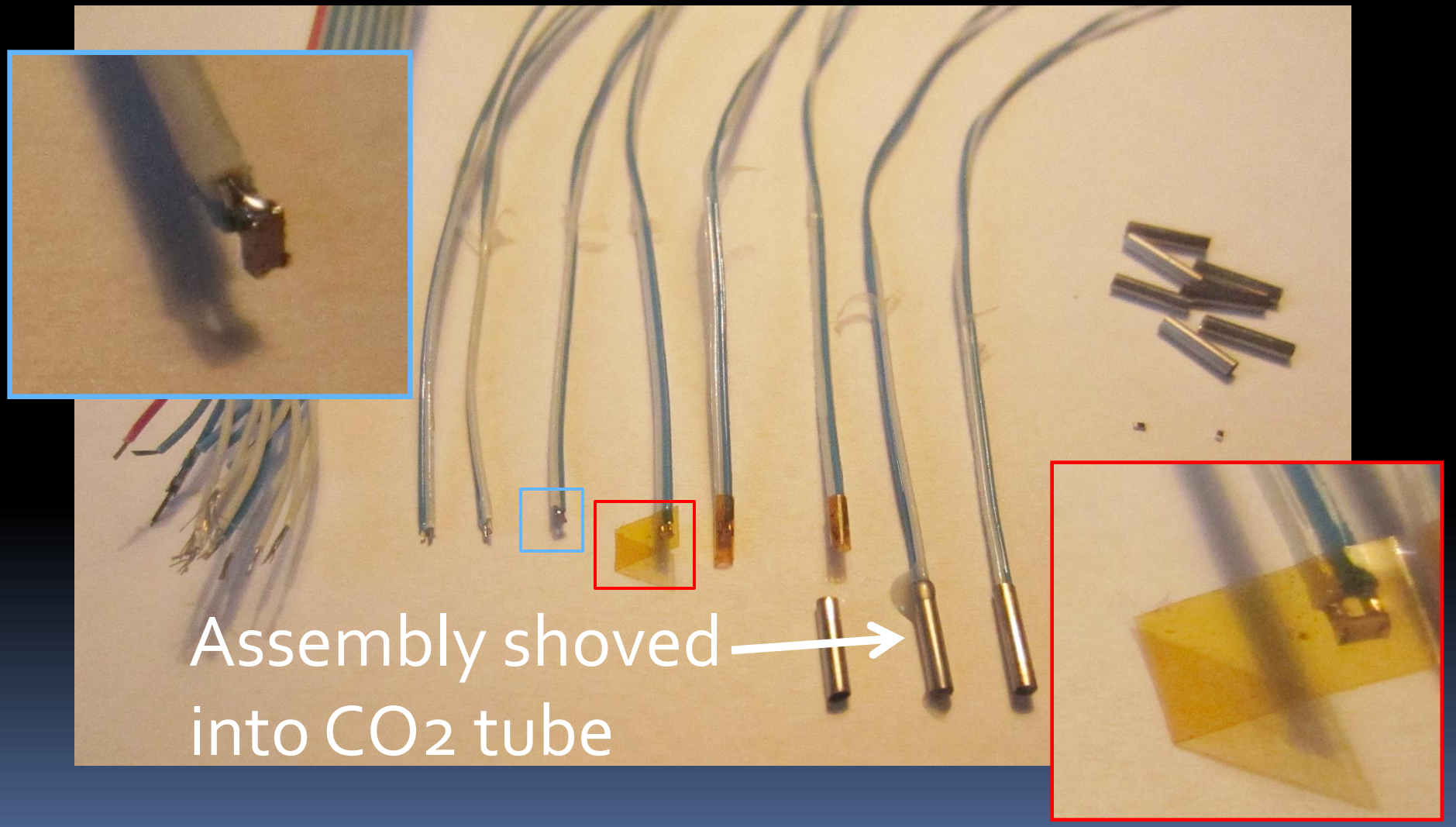
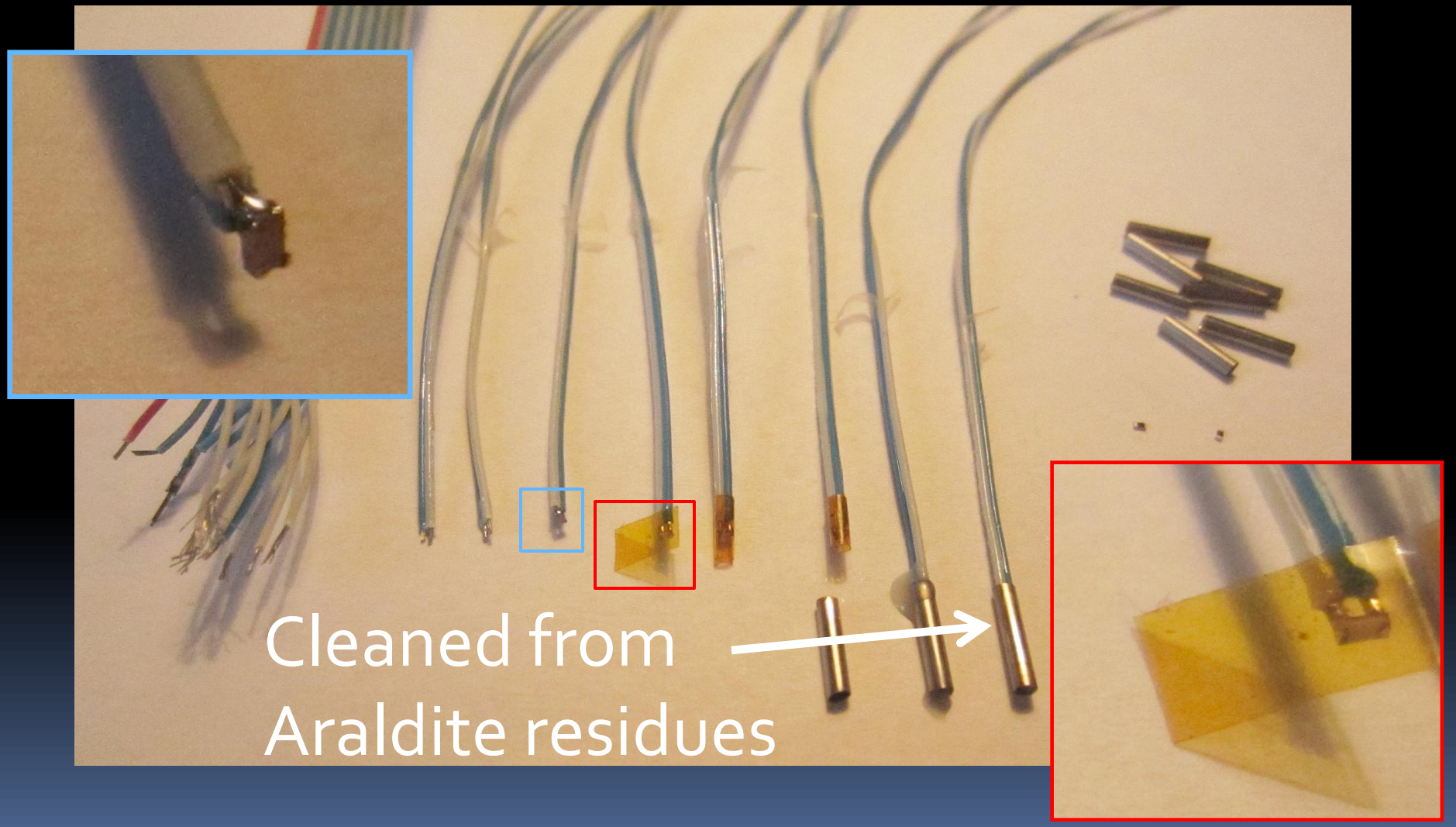


SVD Temperature Sensors (first prototype)



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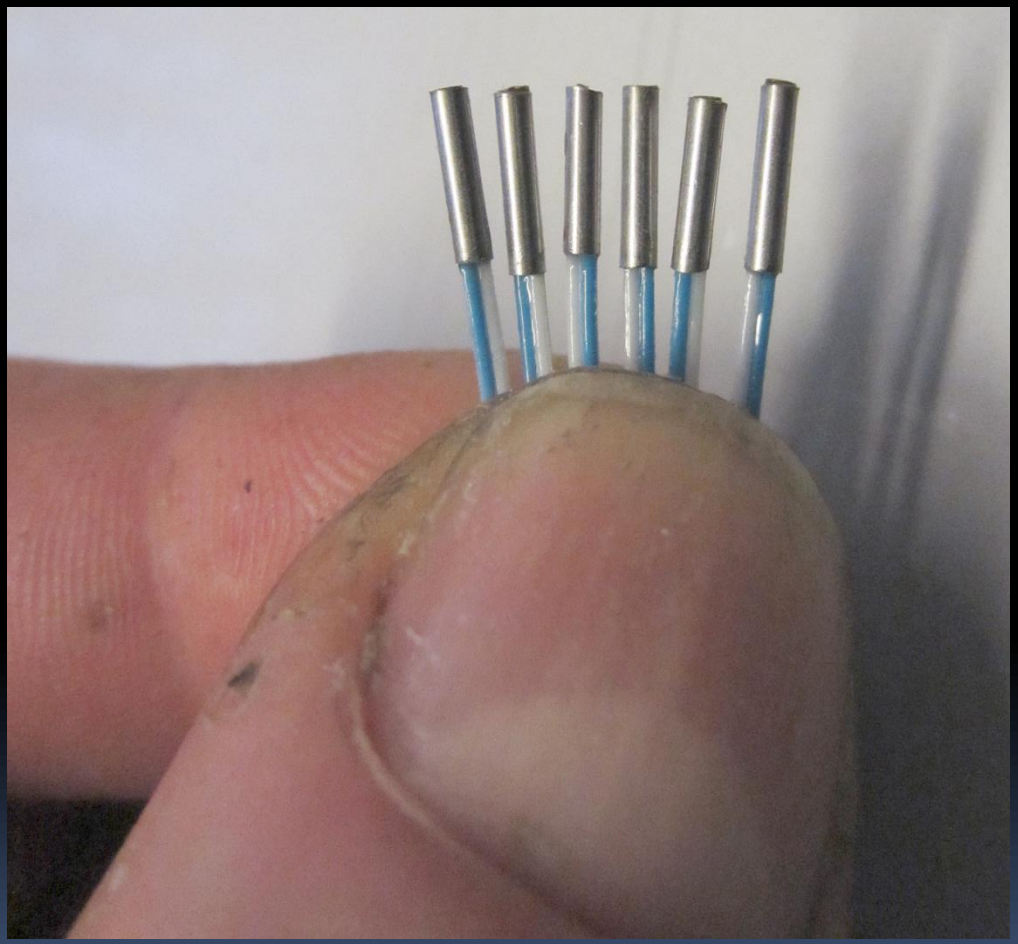


Summary / Outlook

- Hardware:
  - FADC V2 Prototype should be available at the beginning of next week
  - FADC Controller V2 is planned to be ready for the november beamtest
  - Stratix IV GX 360 will be delivered in january 2015
  - Design of the Hardware Test Systems is ongoing

- Until November Beamtest, I plan to:
  - Adapt the firmware to the FADC Hardware V2
  - Test and (hopefully not necessary :-)) debug the new hardware
  - Maybe Hit Time Finding

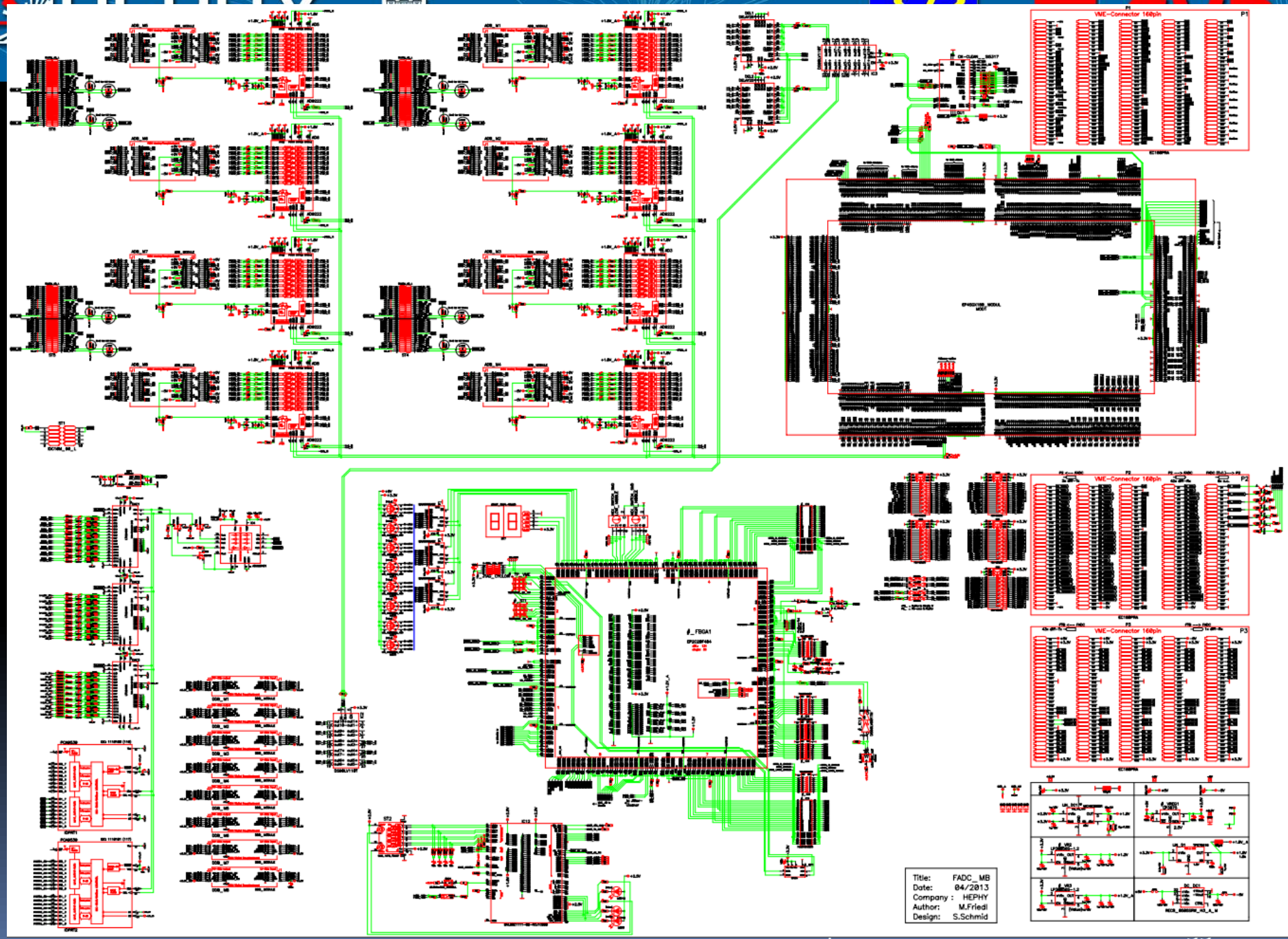
- Afterwards:
  - Firmwares for the Hardware mass production Testsystems
  - Unresolved Firmware issues: (Can anyone help me on Gigabit and Stratix-Configuration-by-Fast-passive-parallel-x8?)
  - Mass production of hardware to start in Q1/2015 (although this could be somewhat relaxed in view of the global schedule)

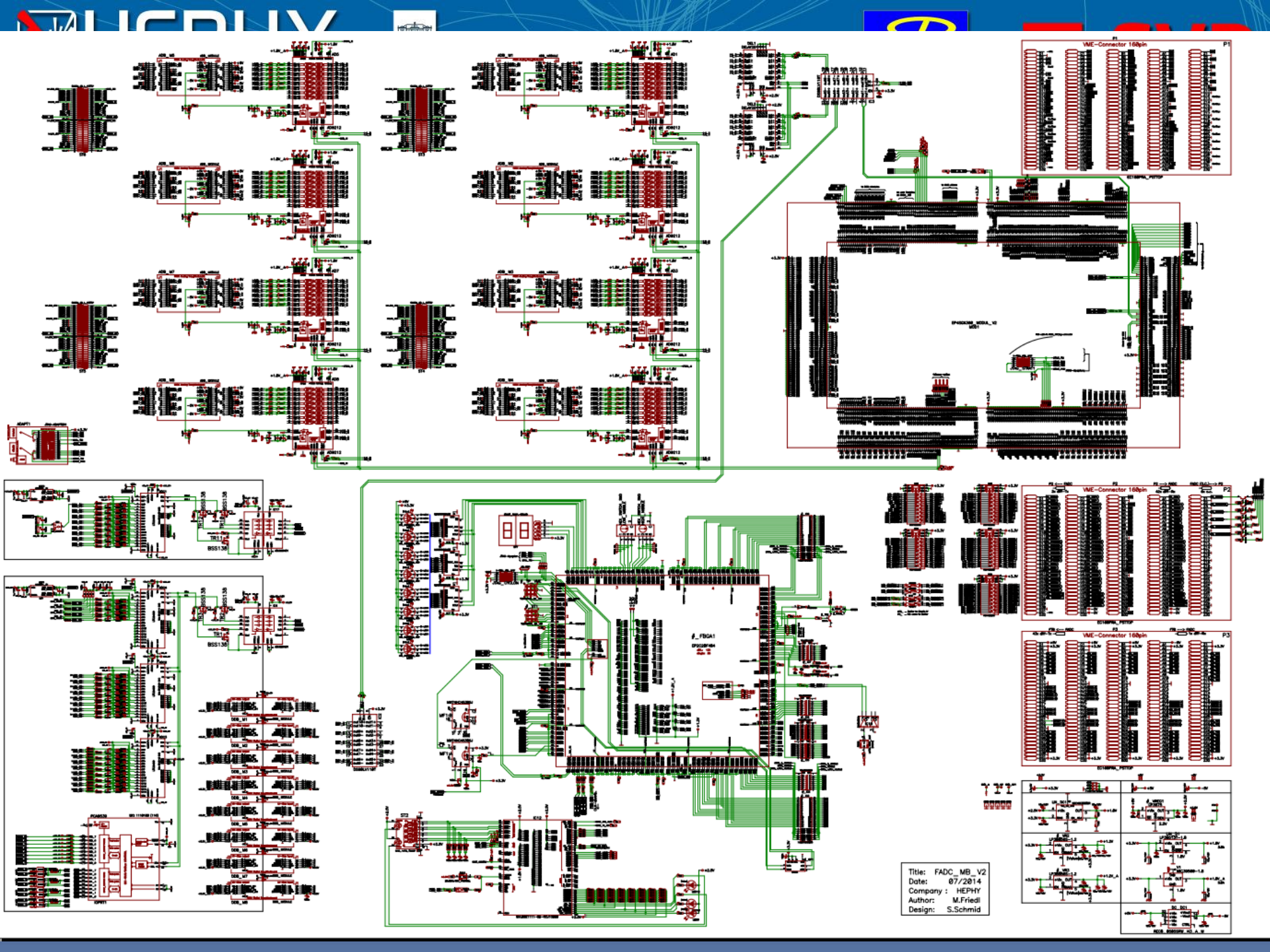
The End...

... for now.

There is still a lot of work to do until the November Beamtest at Cern, but I am really looking forward to it ☺

BACKUP SLIDES ...


VME-Connector 160pin
P1
VME-Connector 160pin
P2
VME-Connector 160pin
P3
Title: FADC_MB
Date: 04/2013
Company : HEPHY
Author: M.Friedl
Design: S.Schmid


VME-Connector 160pin
P1
VME-Connector 160pin
P2
VME-Connector 160pin
P3
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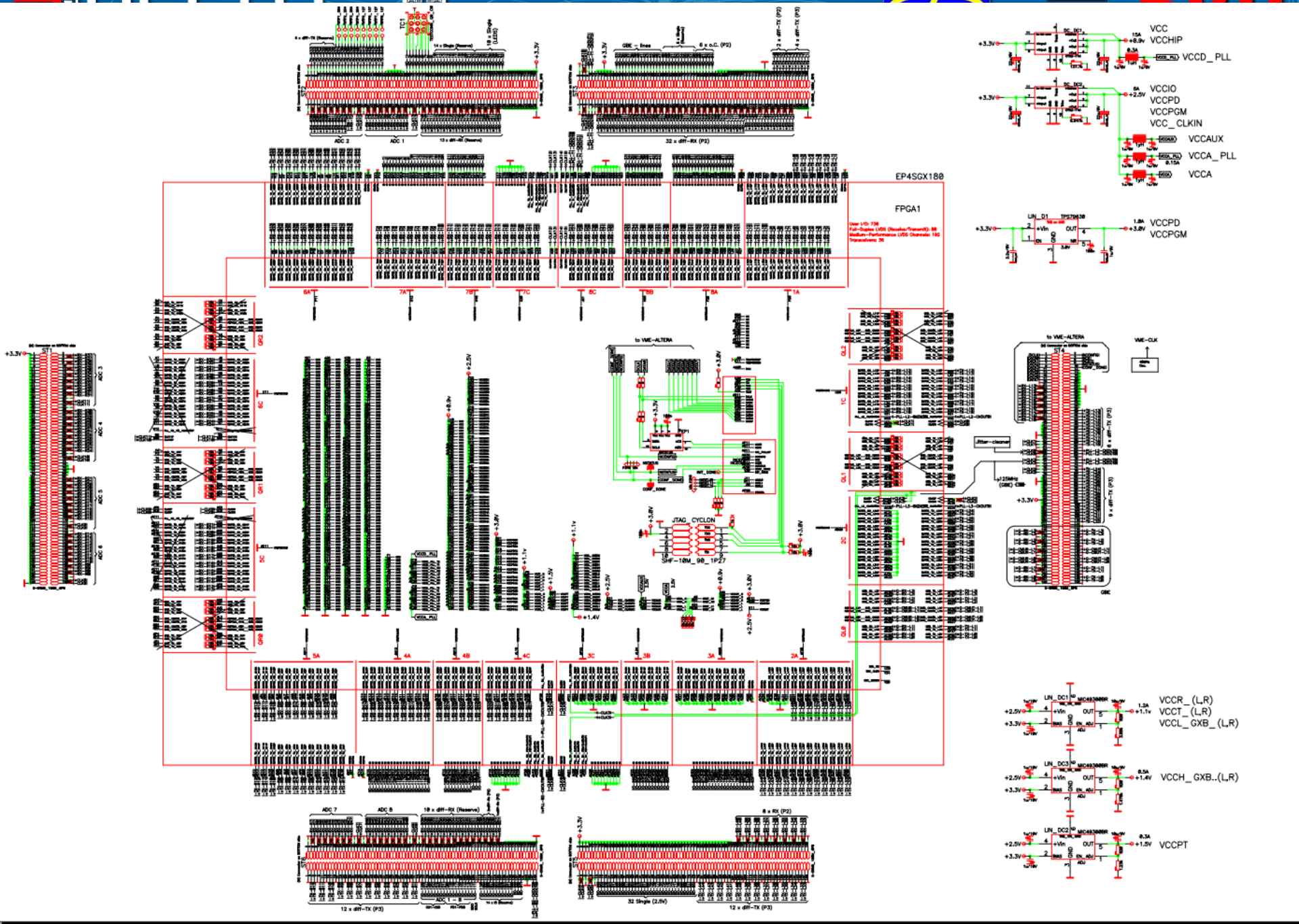
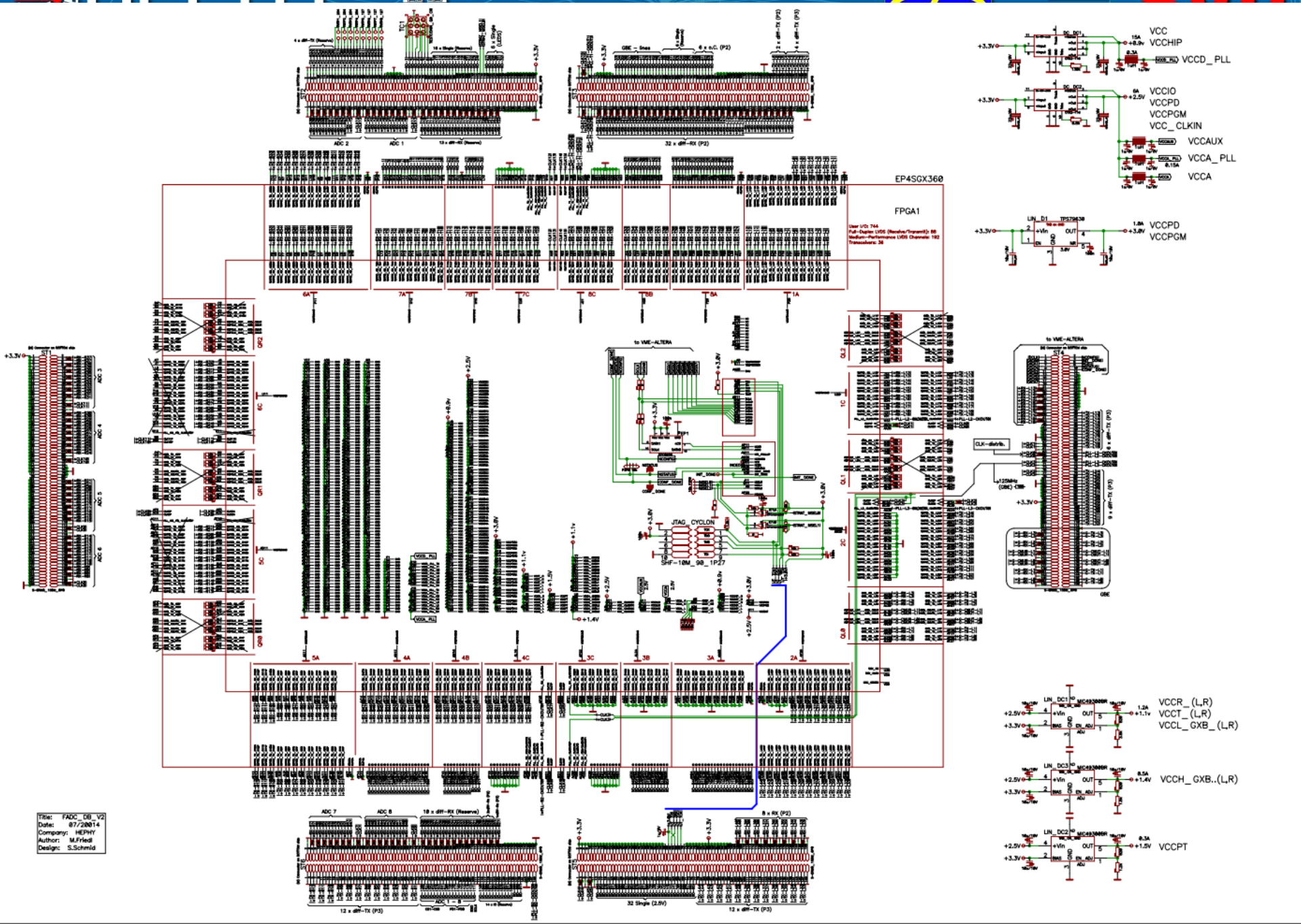
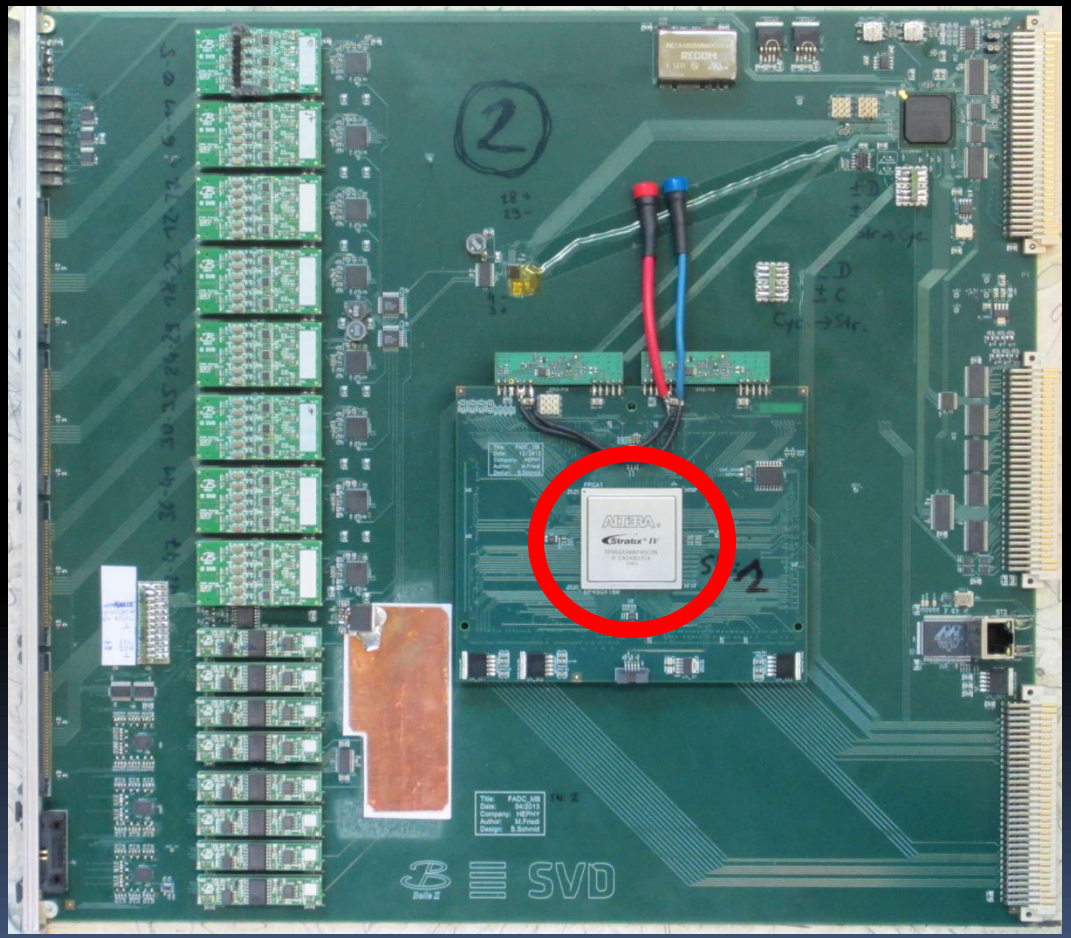
Date: 07/2014
Company : HEPHY
Author: M.Friedl
Design: S.Schmid


EP4SGX180
FPGA1
VCC
VCCHIP
VCCD_PLL
VCCIO
VCCPD
VCCPGM
VCC_CLKIN
VCCAUX
VCCA_PLL
VCCA
VCCPD
VCCPGM
VCCR_(L,R)
VCCT_(L,R)
VCCL_GXB_(L,R)
VCCH_GXB..(L,R)
VCCPT
JTAG_CYCLON
to VME-ALTERA
VME-CLK

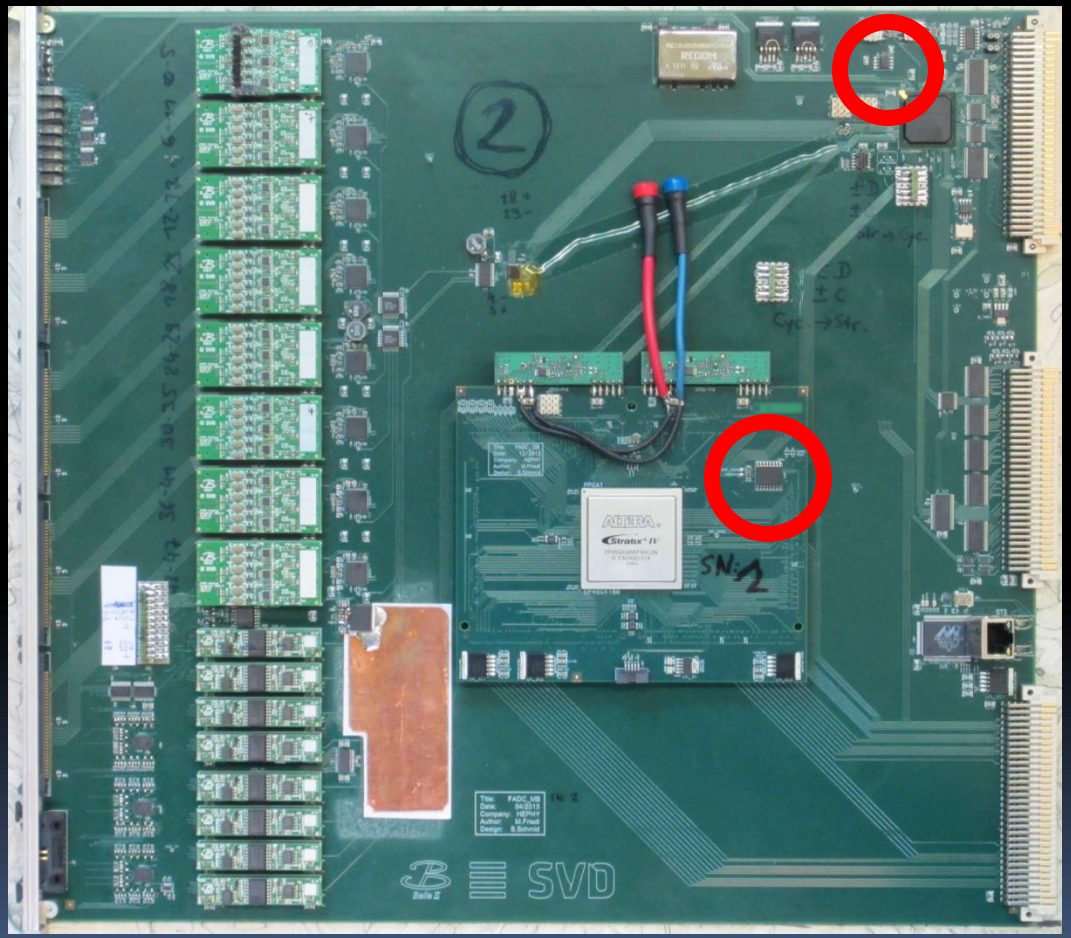

EP4SGX360
FPGA1
VCC
VCCHIP
VCCD_PLL
VCCIO
VCCPD
VCCPGM
VCC_CLKIN
VCCAUX
VCCA_PLL
VCCA
VCCPD
VCCPGM
VCCR_(L,R)
VCCT_(L,R)
VCCL_GXB_(L,R)
VCCH_GXB..(L,R)
VCCPT
JTAG_CYCLON
Title: FADC_DB_V2
Date: 07/2014
Company: HEPHY
Author: M.Friedl
Design: S.Schmid

FADC: Recent activities



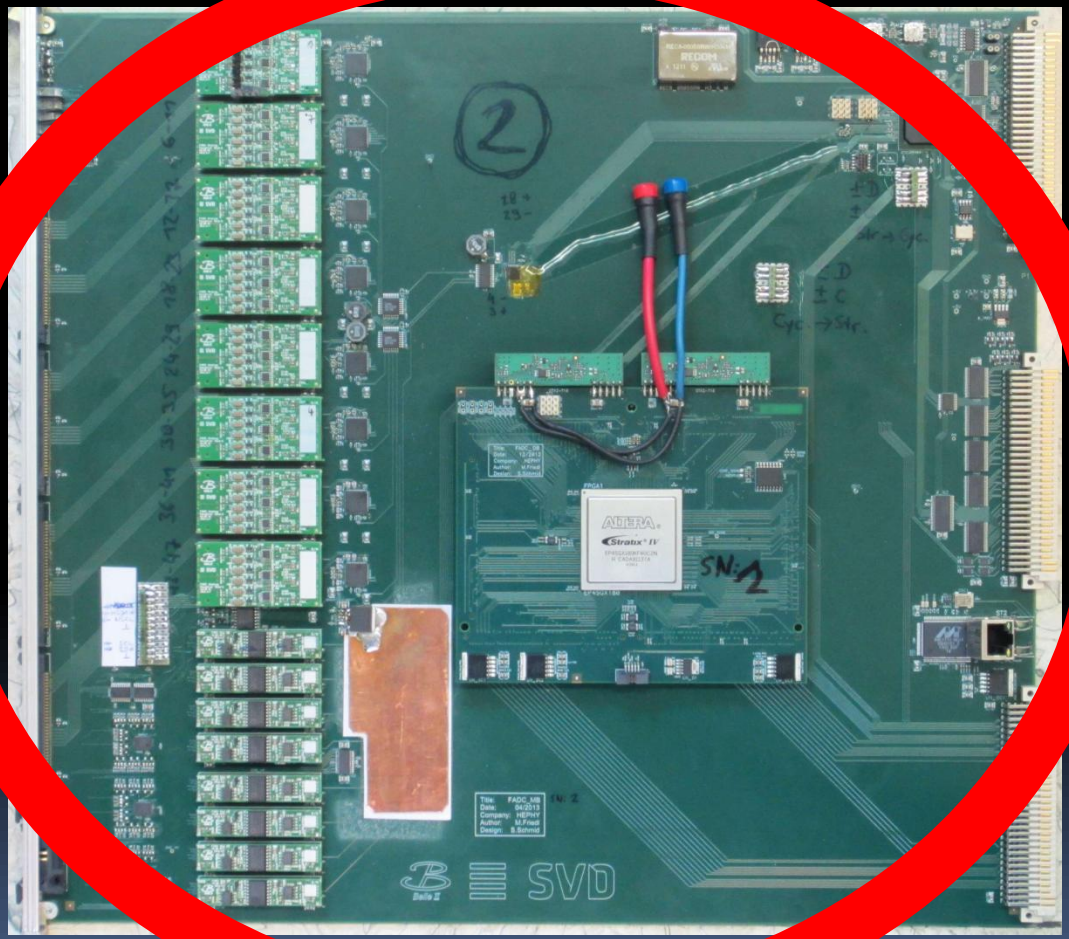
- Selection of the final FPGA:
  Stratix IV GX 360, Speed Grade 2,
  which will be sufficient in mightiness
  while not overly expensive.
  (we are waiting for one pending offer,
  but they will be ordered very soon).

FADC: Recent activities



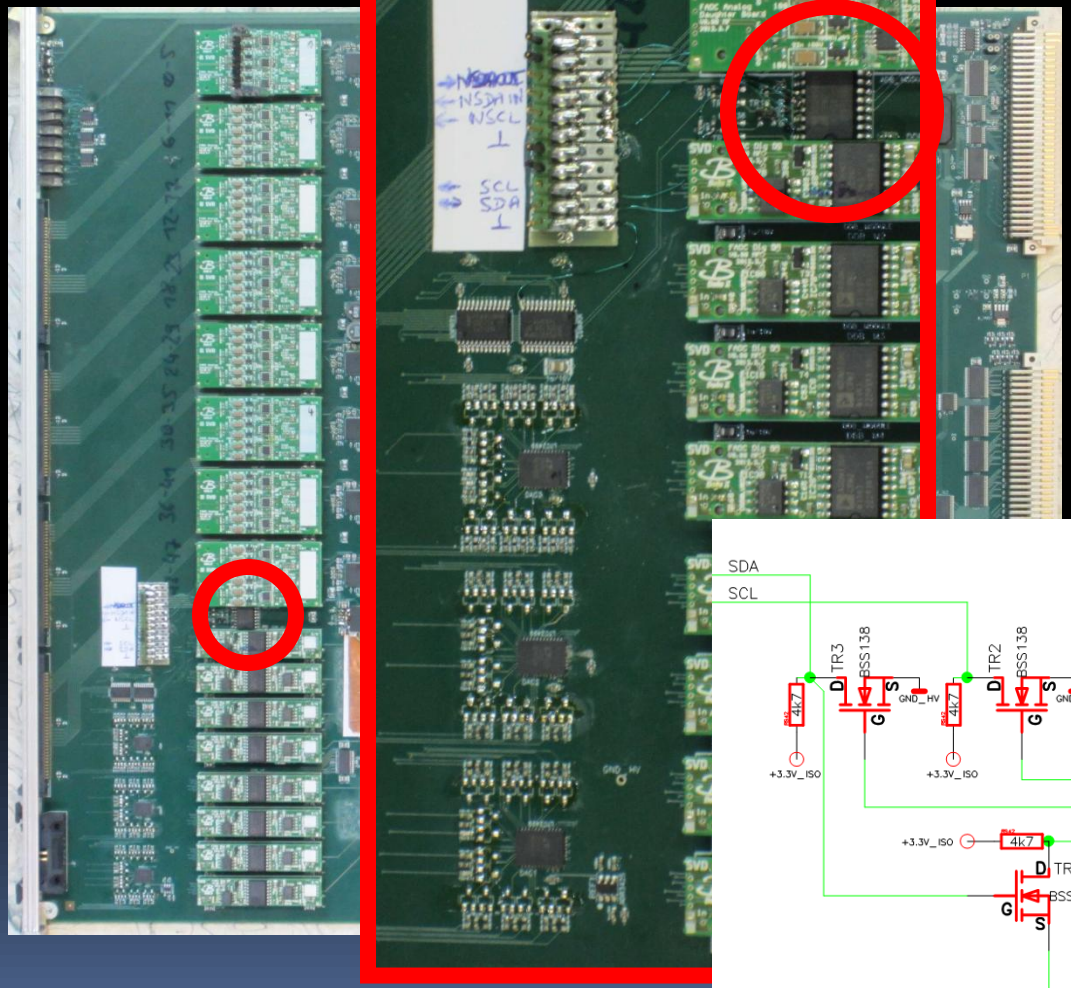
- Selection of the final FPGA: Stratix IV GX 360, Speed Grade 2
- Investigation of various FPGA configuration methods (still to be finally decided, but will probably be programming of FPGA-configuration-EEPROMS via VME).

FADC: Recent activities

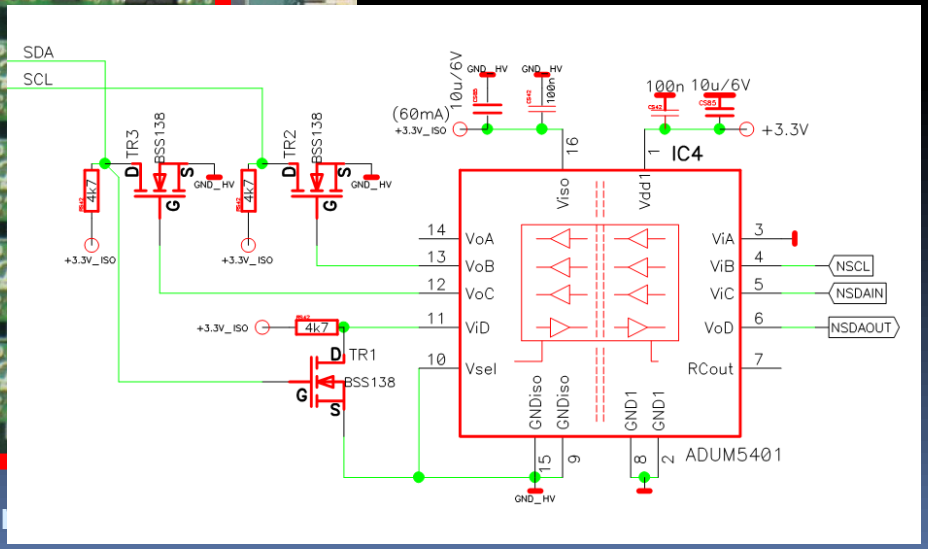


- Selection of the final FPGA: Stratix IV GX 360, Speed Grade 2
- Investigation of various FPGA configuration methods
- Revision of all the passive components of the whole board (also of the FADC controller) to minimize the amount of different parts while improving the system reliability (together with Sigi)

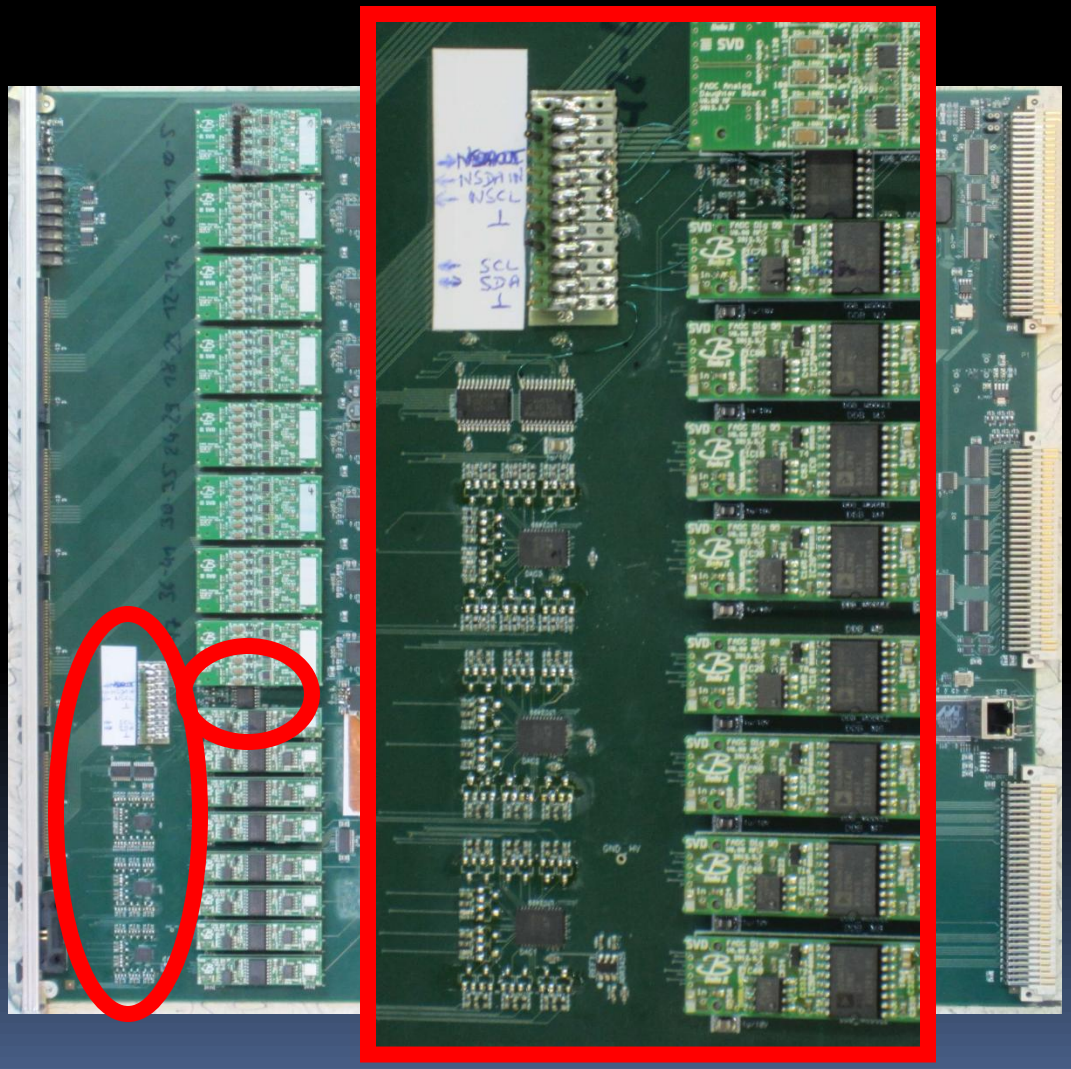
FADC: Recent activities



- Selection of the final FPGA: Stratix IV GX 360, Speed Grade 2
- Investigation of various FPGA configuration methods
- Revision of the passive components
- Slow-Control:
  consists of ADCs and digital I/Os, controlled by an I2C bus which is electrically insulated from the other circuits by DC/DC-data-converters,

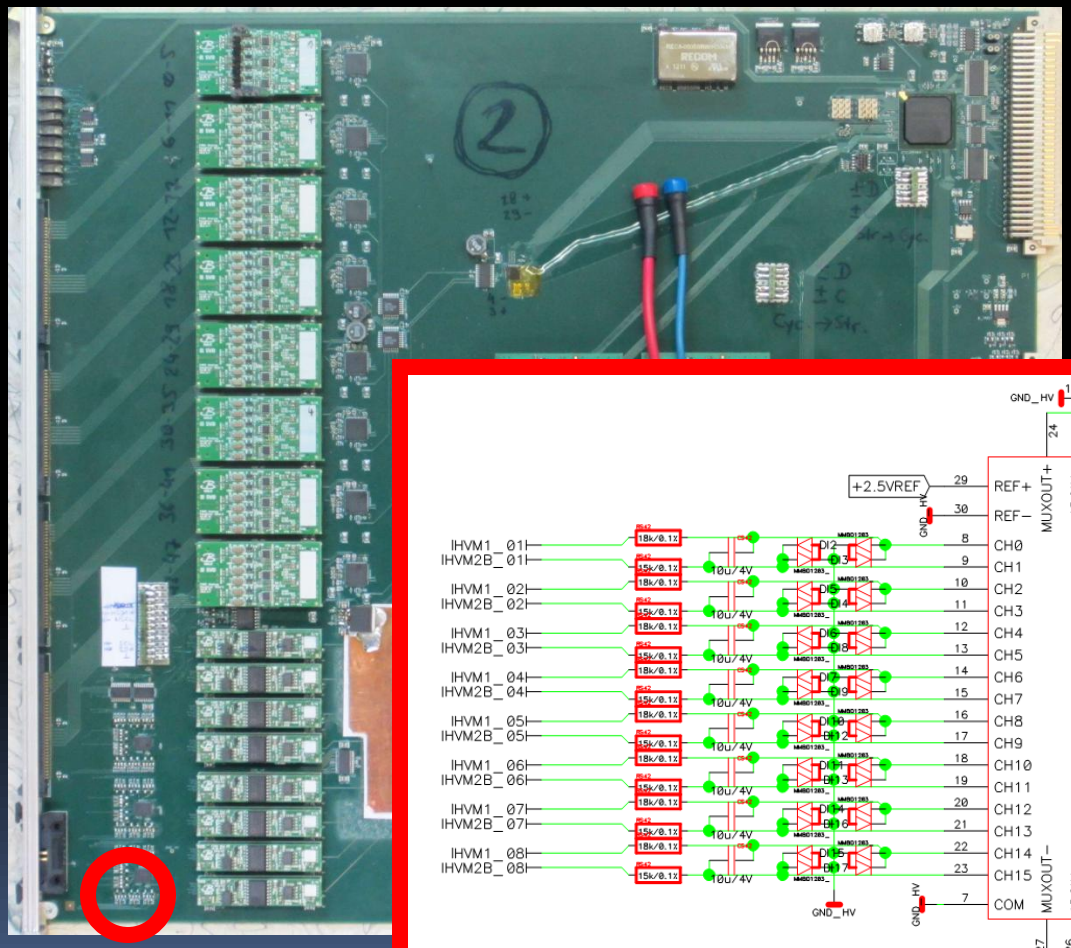


FADC: Recent activities



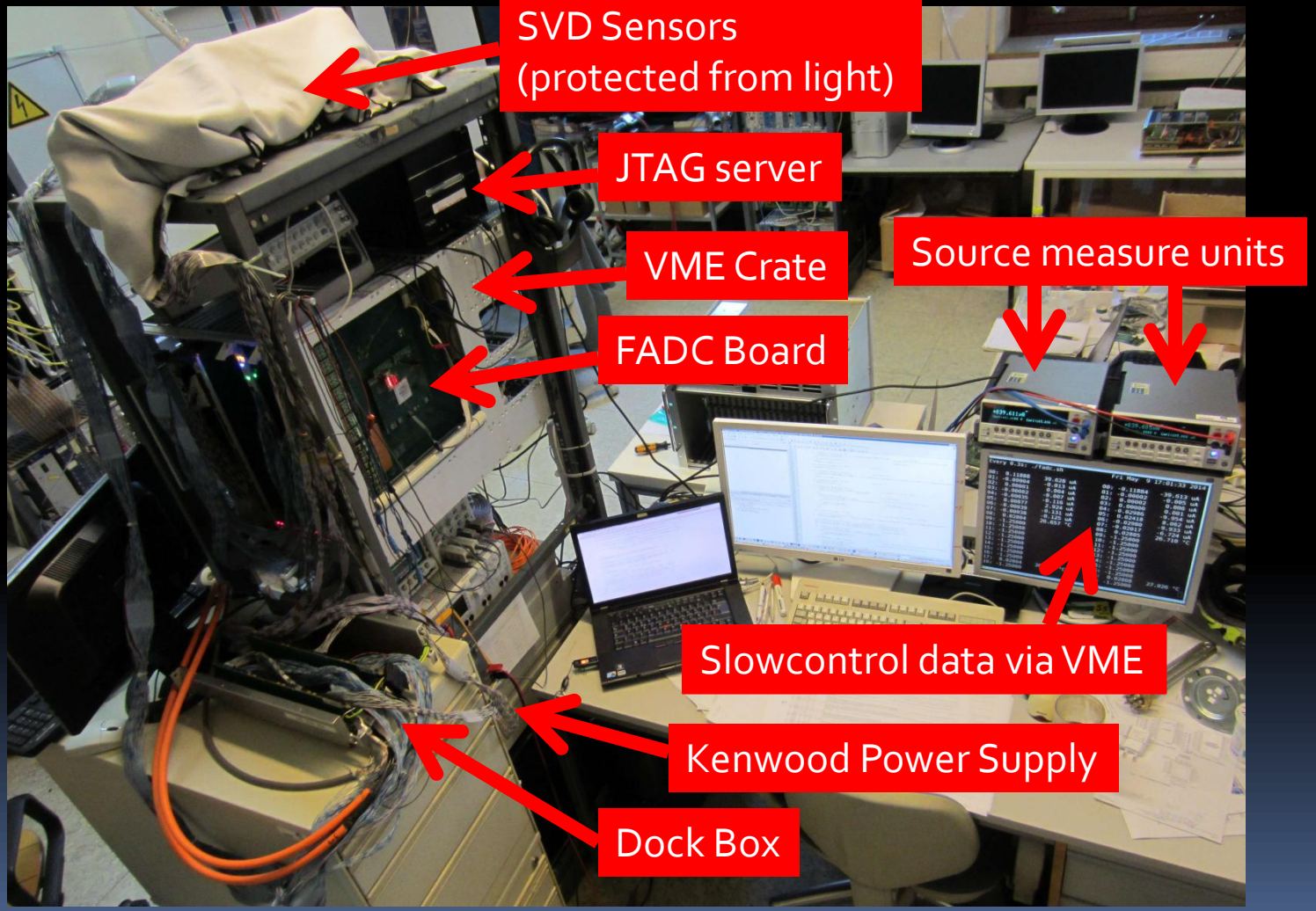
- Selection of the final FPGA: Stratix IV GX 360, Speed Grade 2
- Investigation of various FPGA configuration methods
- Revision of the passive components
- Slow-Control:
  consists of ADCs and digital I/Os, controlled by an I2C bus which is electrically insulated from the other circuits by DC/DC-data-converters, to exchange data (currents, voltages, temperatures, DC/DC-enables, DC/DC-Power-Goods) with the Dock Box.
  All input data (37 32-bit-words) can be read by the DAQ system with a single VME-Blockread.

FADC: Recent activities

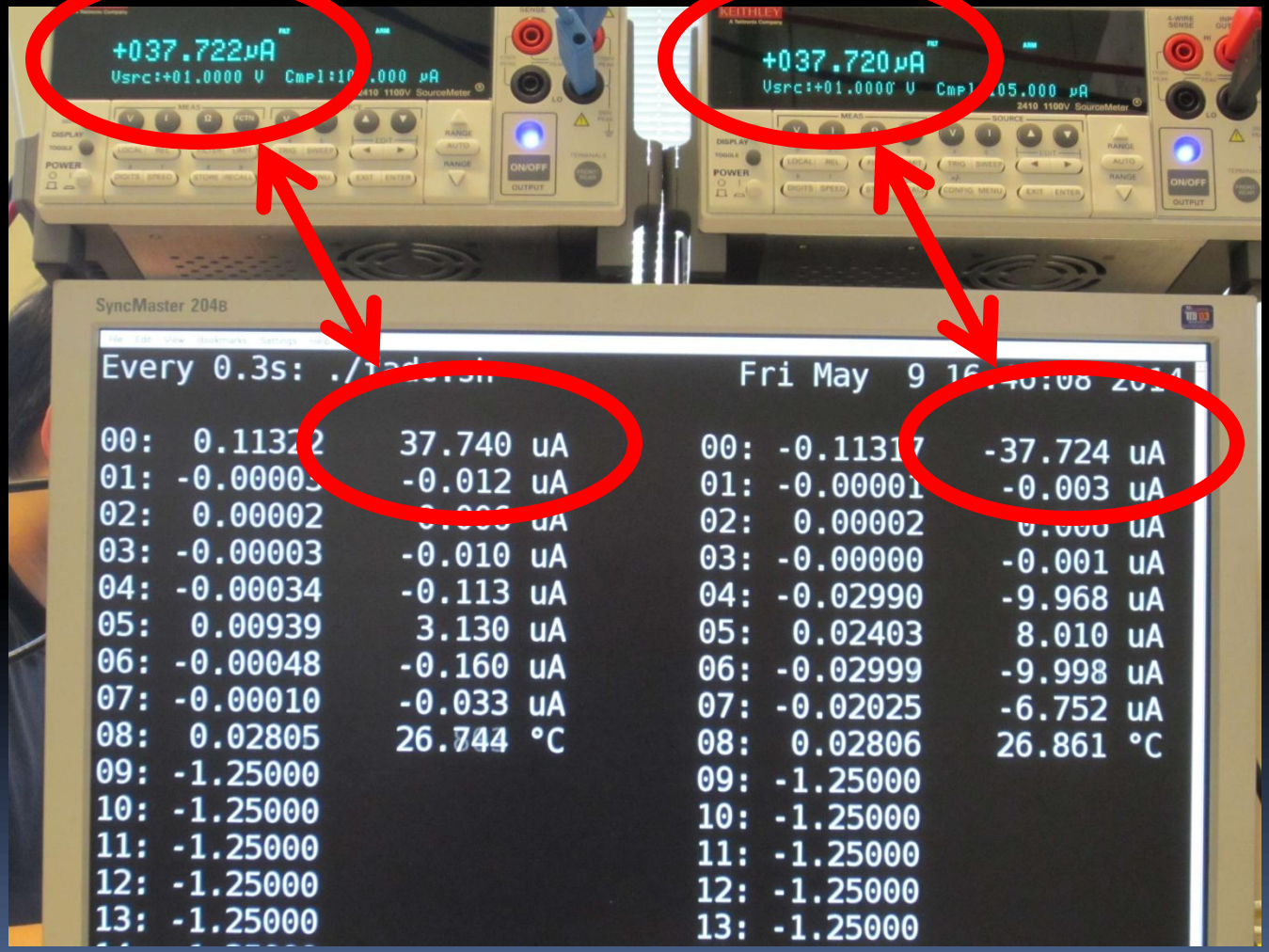


- Selection of the final FPGA: Stratix IV GX 360, Speed Grade 2
- Investigation of various FPGA configuration methods
- Revision of the passive components
- Slow-Control:
  - HV current monitoring (µA)

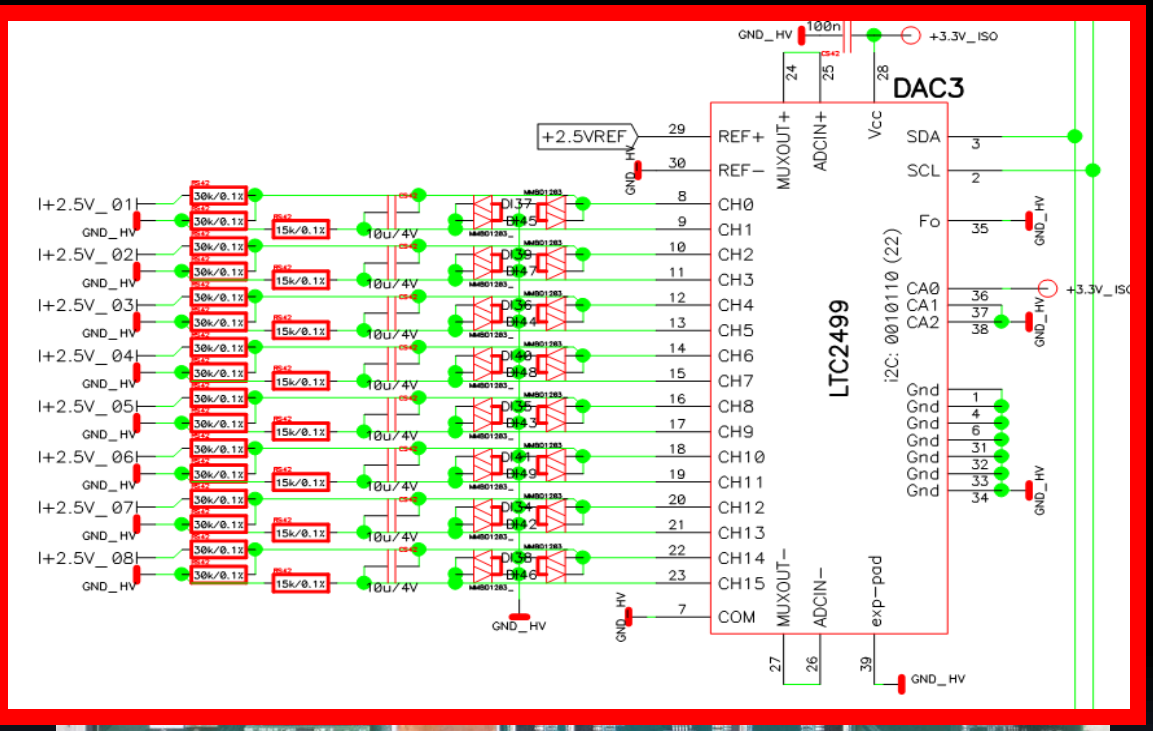
FADC – HV-current monitoring test setup



Slow Control – HV current measurement

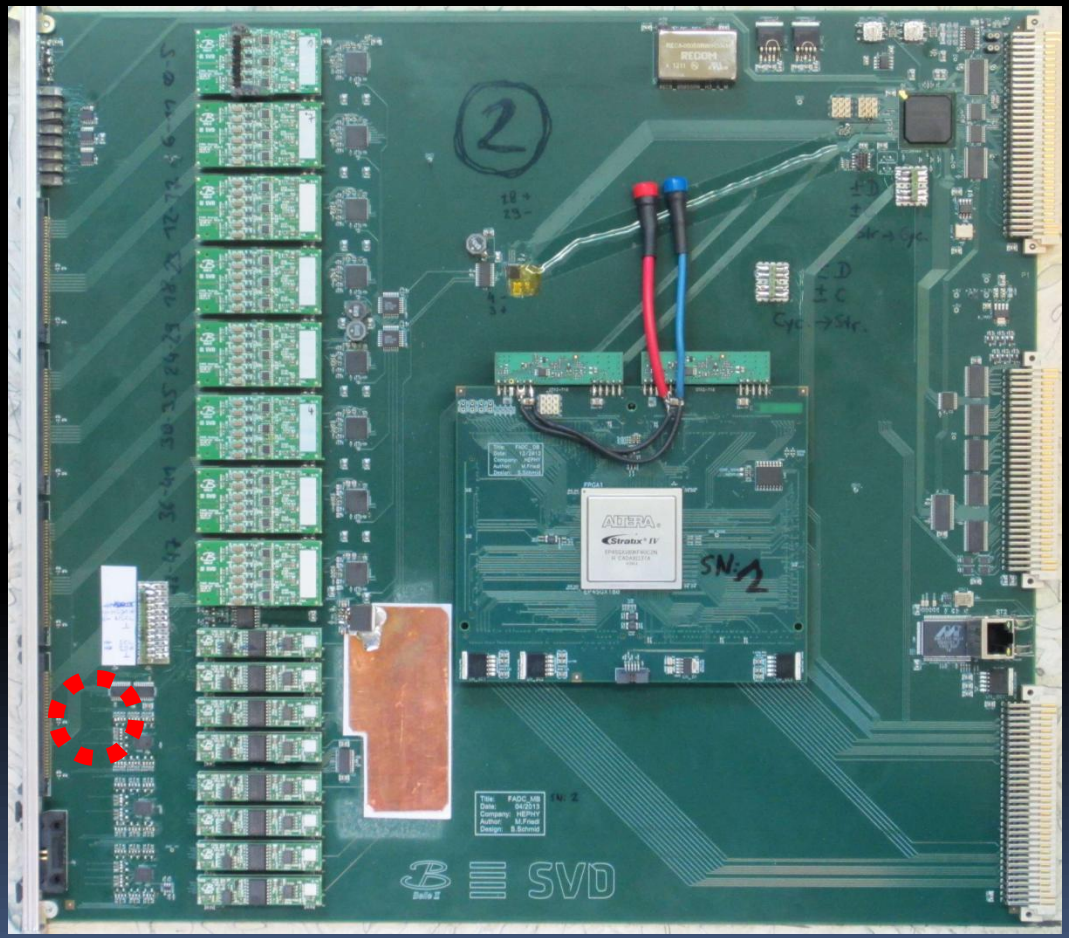


FADC: Recent activities



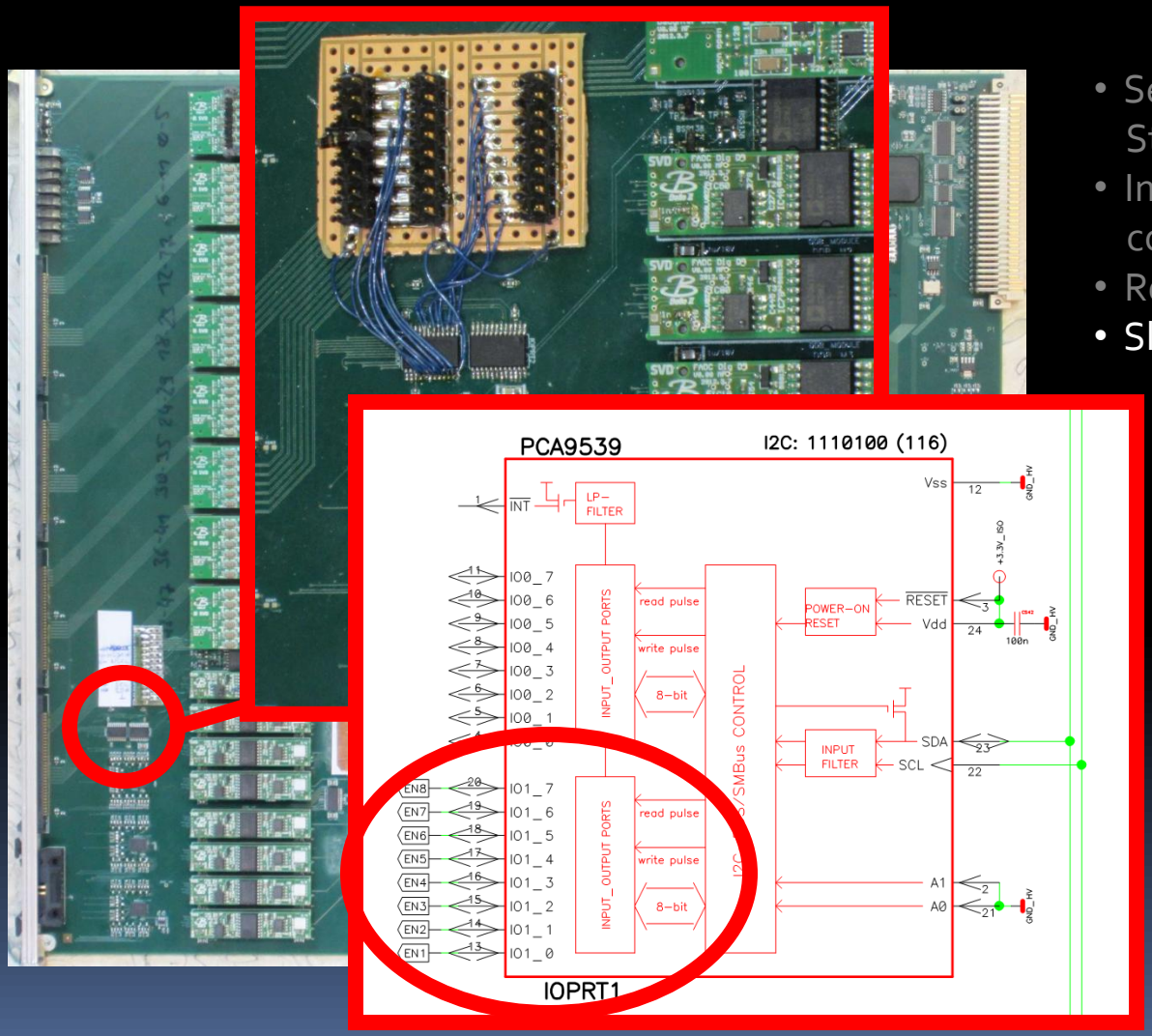
- Selection of the final FPGA: Stratix IV GX 360, Speed Grade 2
- Investigation of various FPGA configuration methods
- Revision of the passive components
- Slow-Control:
  - HV current monitoring (µA)
  - 1.25V monitoring
  - 2.5V monitoring

FADC: Recent activities



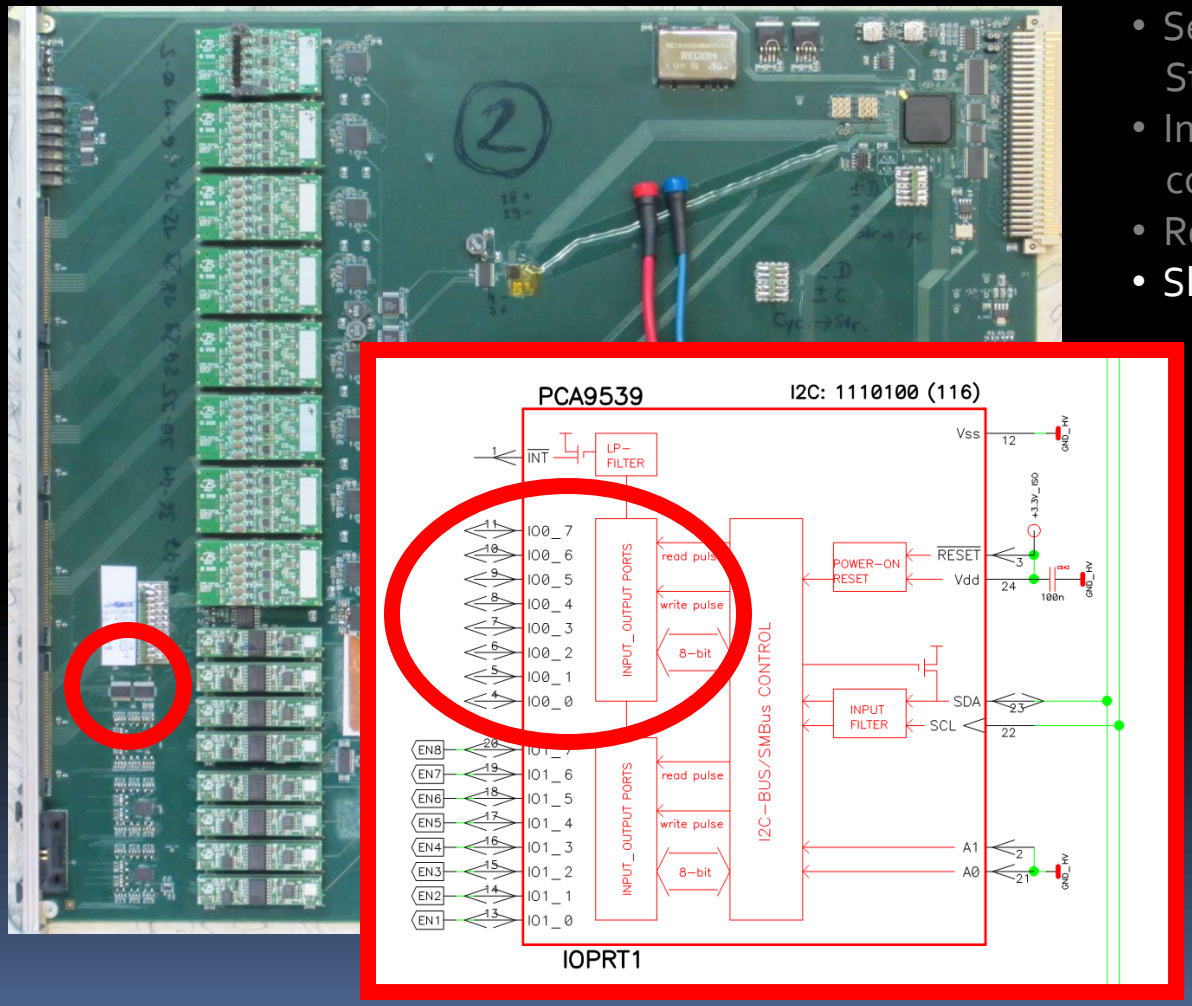
- Selection of the final FPGA: Stratix IV GX 360, Speed Grade 2
- Investigation of various FPGA configuration methods
- Revision of the passive components
- Slow-Control:
  - HV current monitoring (µA)
  - 1.25V monitoring
  - 2.5V monitoring
  - temperature monitoring of the Dock Box (the ADCs are not implemented in hardware yet; they will come in next hardware revision)

FADC: Recent activities



- Selection of the final FPGA: Stratix IV GX 360, Speed Grade 2
- Investigation of various FPGA configuration methods
- Revision of the passive components
- Slow-Control:
  - HV current monitoring (µA)
  - 1.25V monitoring
  - 2.5V monitoring
  - temperature monitoring
- DC/DC-Enable-lines to the Dock Box (the hardware will be changed here to avoid running two DC/DCs operating concurrently in parallel)

FADC: Recent activities



- Selection of the final FPGA: Stratix IV GX 360, Speed Grade 2
- Investigation of various FPGA configuration methods
- Revision of the passive components
- Slow-Control:
  - HV current monitoring (µA)
  - 1.25V monitoring
  - 2.5V monitoring
  - temperature monitoring
  - Dock Box-DC/DC-Enable-lines
  - DC/DC-Power-Good-Signals from the Dock Box