DHH Development for the EMCM Test Setup

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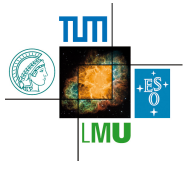
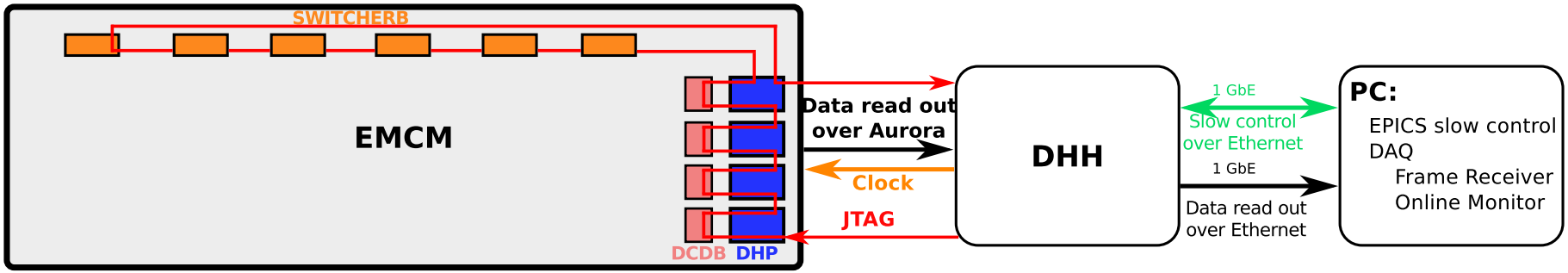
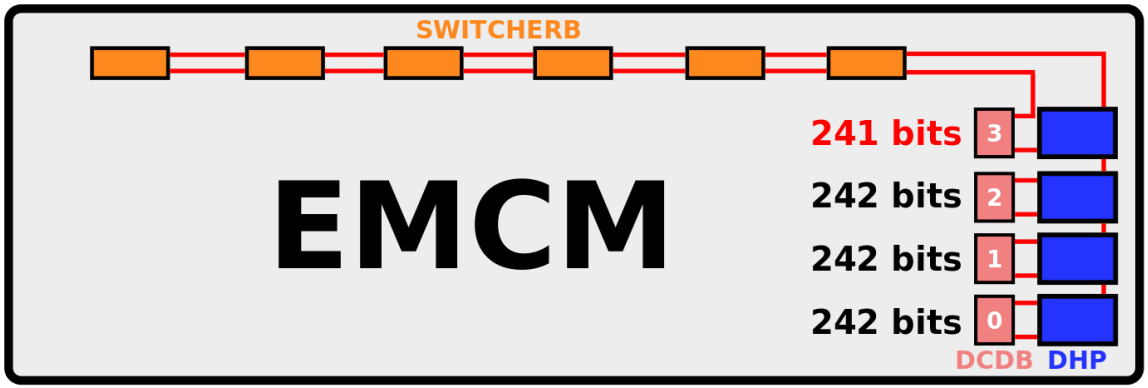


Setup Overview



Outline

DCD Configuration Problem



- last DCDB requires one bit less during configuration
- same situation on the module with only one DHP-DCD pair
- work around implemented in software to mitigate the problem

Problem Localization

- not easy to debug because reading back DCD register is not supported
- trick to localize problem:
  - program DHP and DCD simultaneously
  - read back DHP register and analyze its content
  - repeat with the same bitstream on the next pair

- Switch on DCD0: DCD0 ON. Read data: 01020304 ..
- Switch on DCD1: DCD1 ON. Read data: 01020304 ..
- Switch on DCD2: DCD2 ON. Read data: 01020304 ..
- Switch on DCD3: all DCDs OFF. Read data: 01020304 ..
- Switch on DCD3, remove one bit: DCD3 ON. Read data: **02040608** ..

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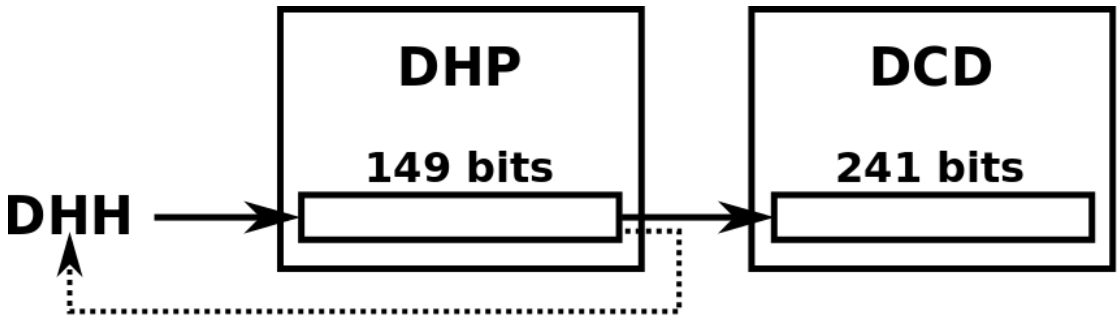

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- Switch on DCD1: DCD1 ON. Read data: 01020304 ..
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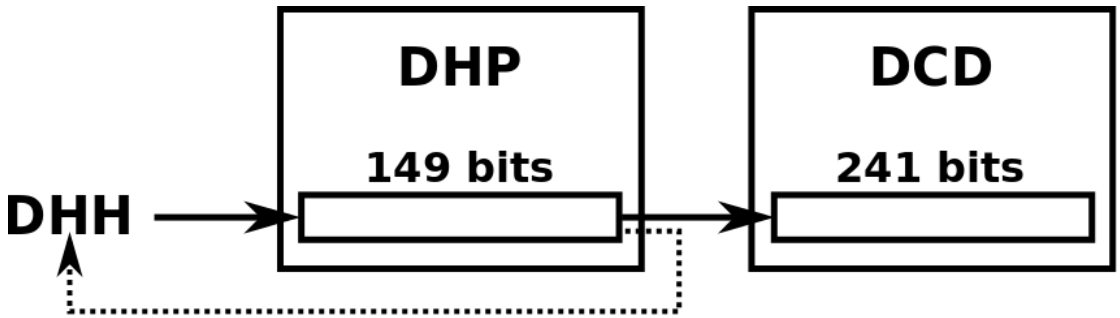

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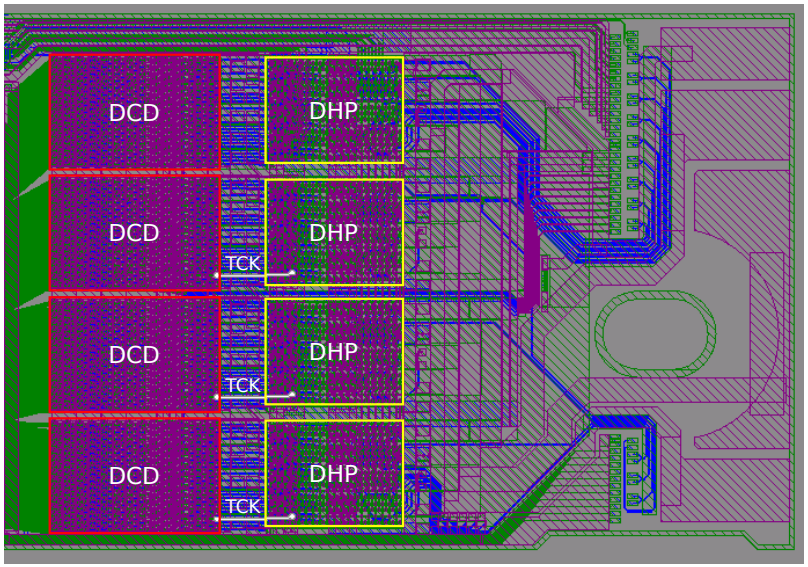
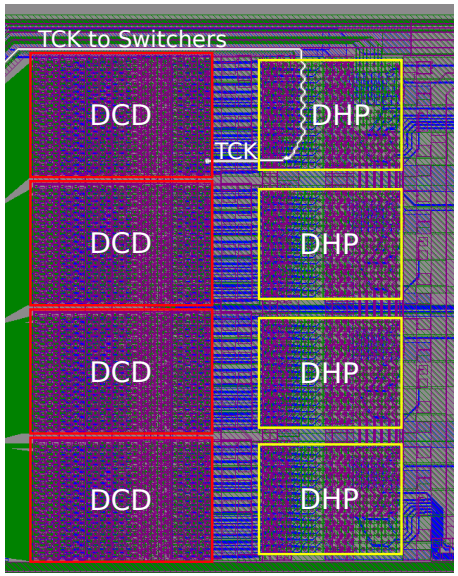
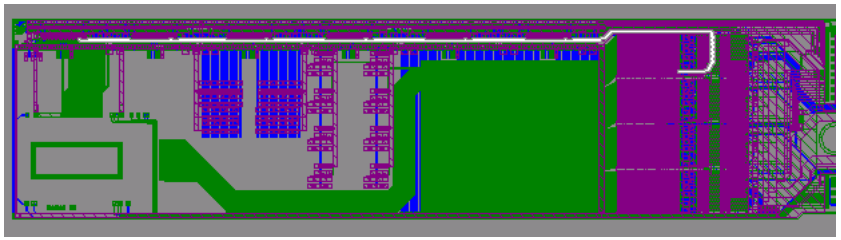
TCK Layout on the EMCM

DCD0-2:



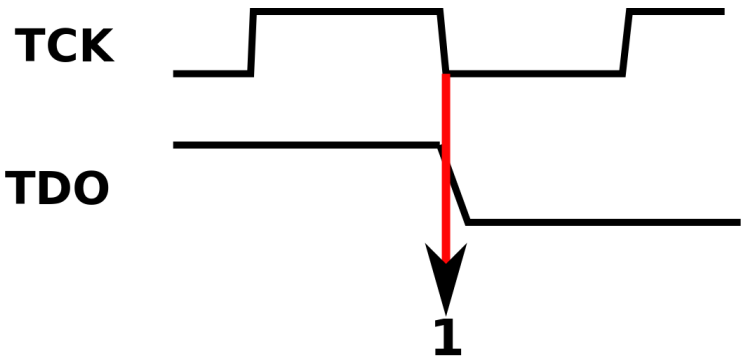
DCD3:





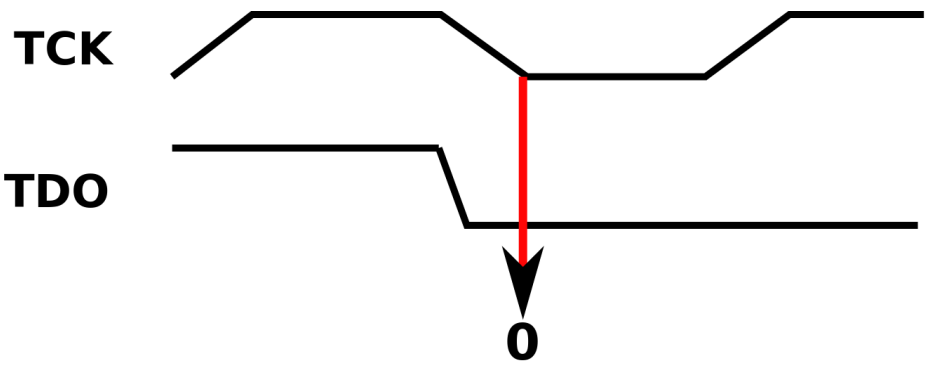
Metastability Issue

DCD0-2:



- clock and data equally fast
  - previous bit sampled
- requires additional bit for compensation

DCD3:



- long TCK line:
  - large capacitance
  - slow signal transition
- does not require dummy bit

Implications/Solutions

Implications

- uncertainty in the configuration because of metastability
- stability of the configuration strongly depends on environment

Software Workaround

- using TCK inversion on DHPT
- TMS line delayed by 1/4 of the clock cycle for safe operation
- DCD configured always in a single transaction with DHPT
- DCD target register and DHPT core register are selected
- invert JTAG clock bit is switched on in DHPT, some data is written into the target register of the DCD
  - after this transaction finishes, TCK line is inverted
  - safe programming condition for DCD: TDI changes on rising edge
- DCD target register programmed with correct values, invert JTAG clock bit switched off
- successfully tested on the EMCM

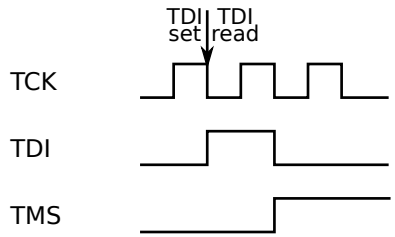


Figure : JTAG timing at DCD **without** workaround

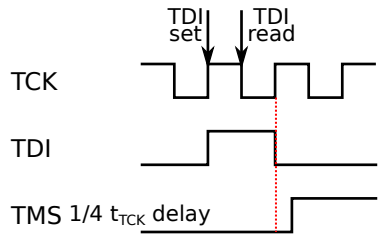
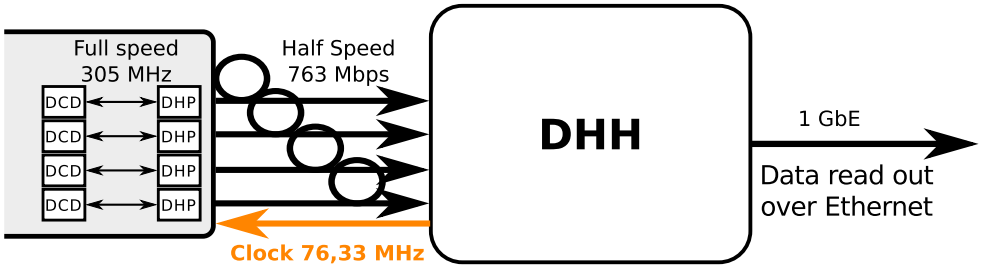


Figure : JTAG timing at DCD **with** workaround

Outline

Half Data Rate Aurora Link

- Motivation: DCD characterization at 305 MHz
  - link instability at full data rate due to signal quality
- Data rate of the link: 1/2 of 1.526 Gbps
  - DHP(T) doubles bit, configured by JTAG
  - same data processing logic on DHH
  - separate DHH firmware required due to tranceiver settings
  - stable data link established on the DHPT test board and EMCM



Conclusions

- JTAG slow control in a good shape
- Firmware for DCD characterization using half rate read out prepared
- TODO:
  - implement DDR3 memory buffer to handle 4 data streams in parallel
  - reading of the DHPT temperature sensor

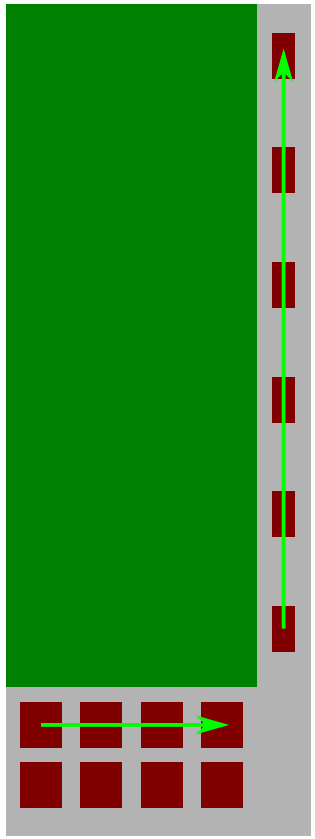
Thank you!
Questions?

Back Up

Back up slides

Back Up

Outer Backward



Outer Forward