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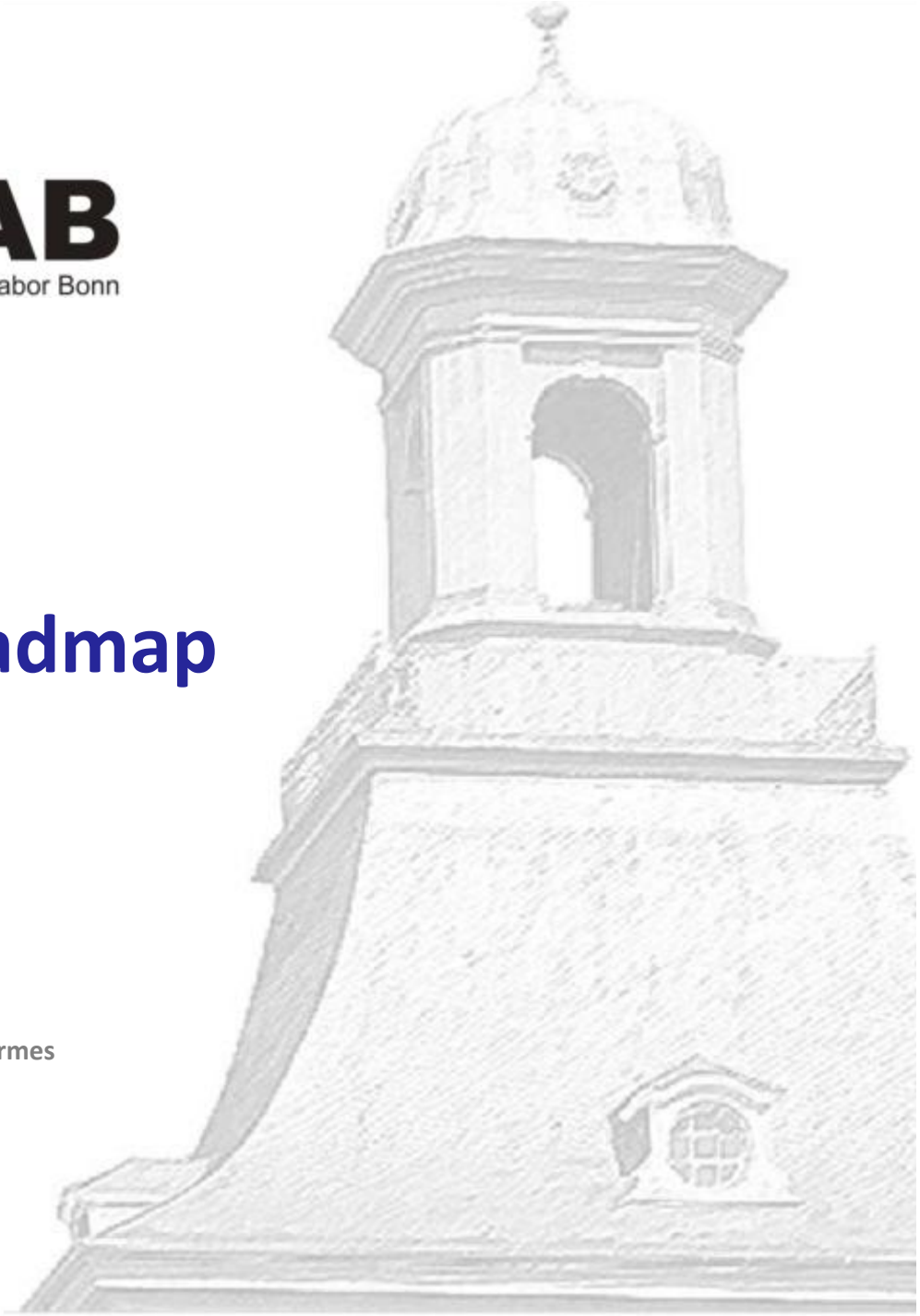

DHPT test status and roadmap

6th Belle II PXD/SVD Workshop

01-03 October 2014, Pisa, Italy

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Contents

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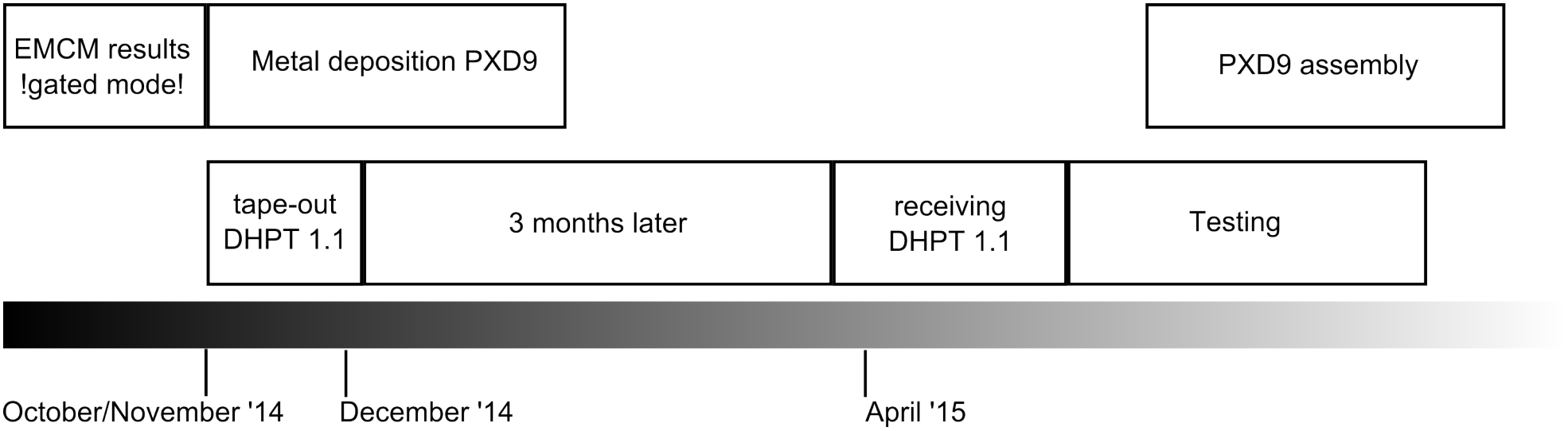
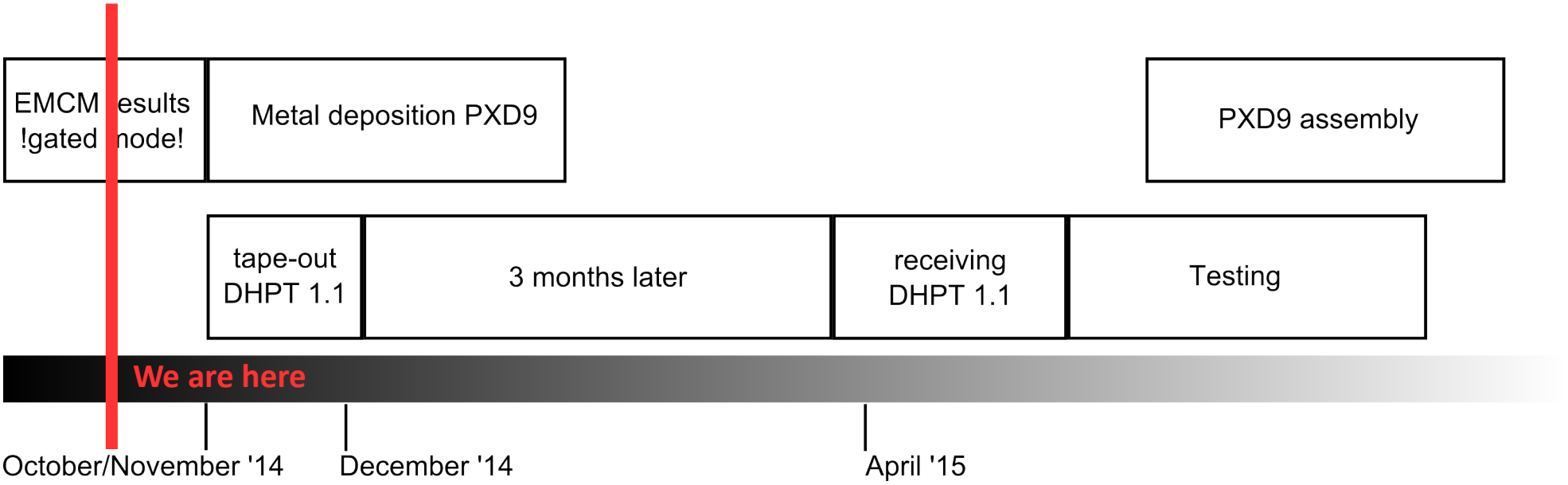
- Roadmap
- Status of Test system
- Estimation of test duration
- Outlook to the full scale test system

Roadmap of DHPT testing



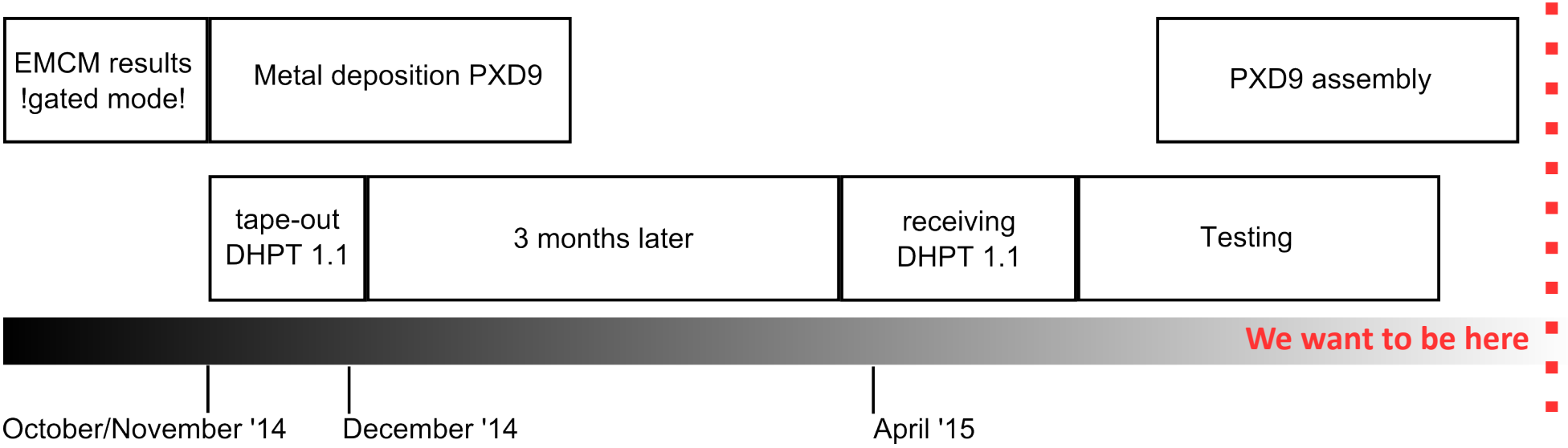
- **Assumes: Design review of all ASICs on the PXD module after Pisa Workshop ~ October/November**
- **Gated-mode has to be tested before Design review!!!**
- **Tape-out of the new revision of DHPT after tested gated mode**
- **DHPT 1.1 testing starts from Q2 '15**

Roadmap of DHPT testing



- **Development phase of the test system**
- **Early I/O tests of the DCD and switcher interface**
  - **10x DHPT 1.0 without any fail**
    - **Random switcher sequences (also with switching between sequences)**
    - **Random DCD data read-out**

Roadmap of DHPT testing



- **Development phase of the test system**
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Status of the test system

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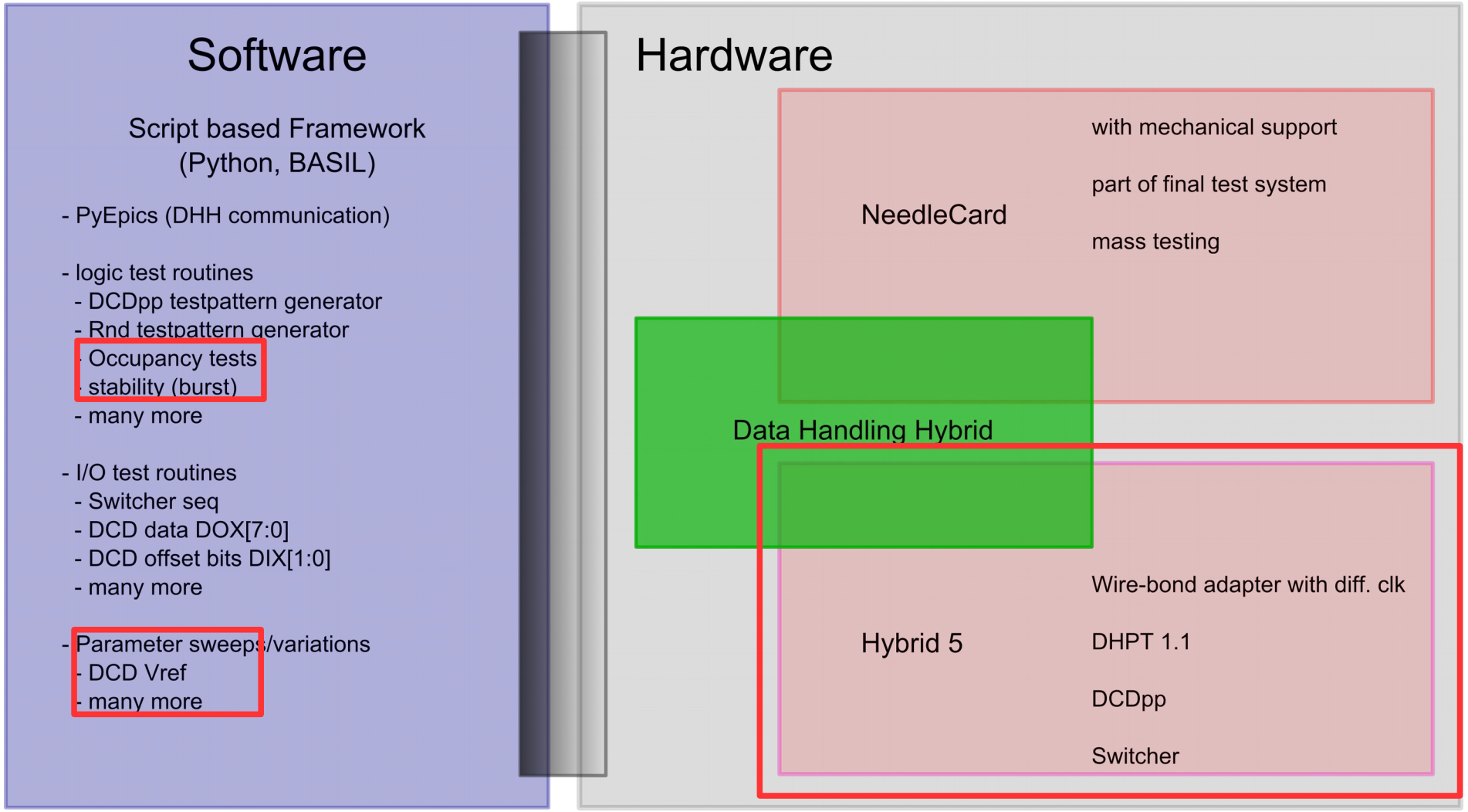
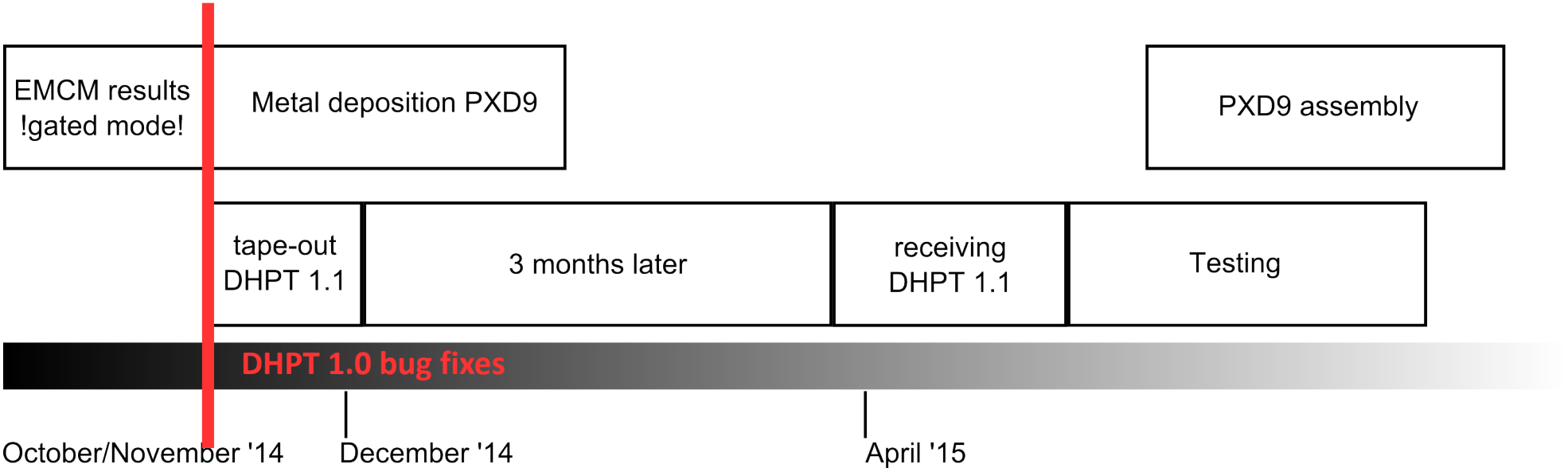


not yet finished

DHH emulator will be replaced by real DHH

Status of the test system



- **Bug fixes of DHPT 1.0 and results of the EMCM3 testing at HLL**
- **!Important! Testing of gated mode on full system → EMCM**
  - **phase tuning, delay**
  - **cannot be done on DHPT standalone tests**

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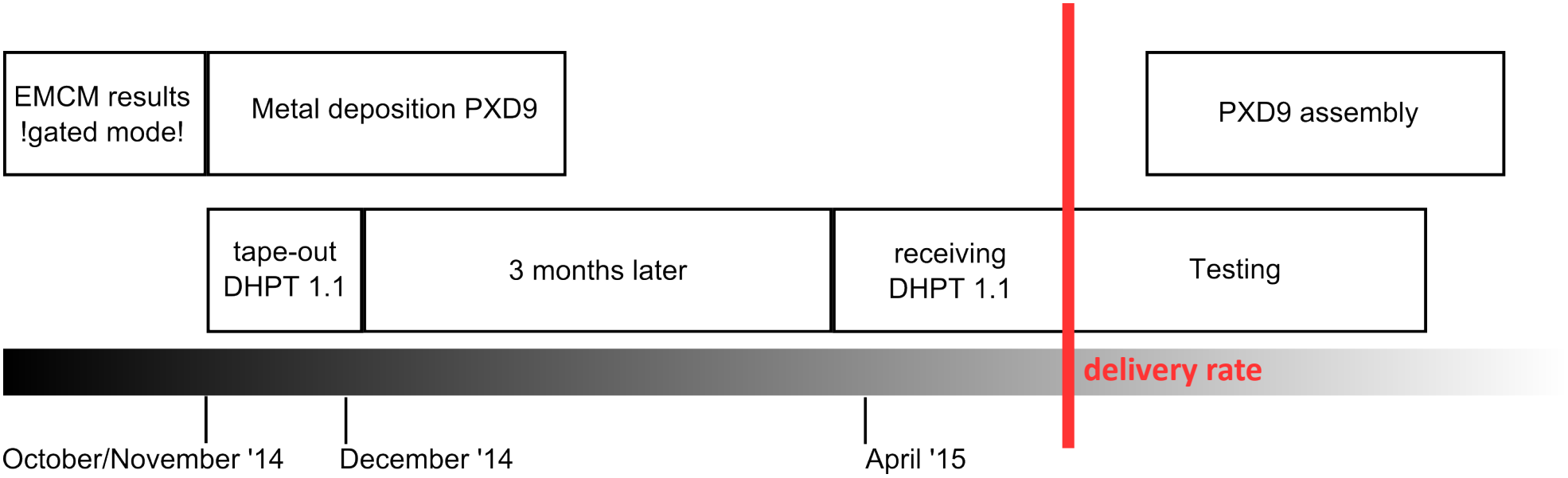
Minor bug fixes of DHPT 1.0

- CML
  - Optimized layout for lower parasitic resistance → Improvement of the output amplitude
- Serializer block
  - Improved robustness against process variations: current MPW production suffered from 'slow' NMOS which needed to be compensated by higher VDD supply
- Logic
  - Minor changes in data format (header information) and additional items to be addressed according to the outcome of the E-MCM tests

Estimation of test duration



First estimation of DHPT delivery rate

Assuming worst case scenario

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Time estimation for full scale testing (assuming "bad" conditions)

- PXD9: 3 batches à 13, 8 and 8 wafers

  → 29 wafers with 6 half modules → 29 x 6 x 4 DHPs ~ 700 DHPs

- Estimated yield 75% (for 65nm TSMC ~ 90% exp.) → 950 tested Dhps

- 1+9 Wafer (100 DHP / wafer)

- Full scale test duration ~ 1h / chip

  A) T_{tot} ~ 5 months or 42 DHPs/week (7 days/week, 6 DHPs/day) 

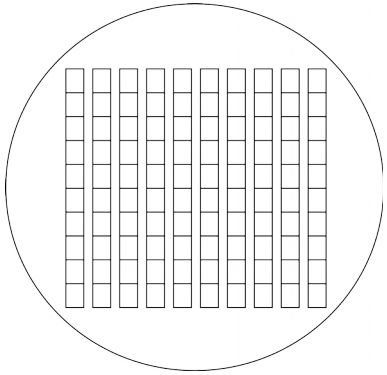
  B) T_{tot} ~ 7 months or 30 DHPs/week (5 days/week, 6 DHPs/day) 

Tuning parameters: Test duration/DHP, Yield, Worktime

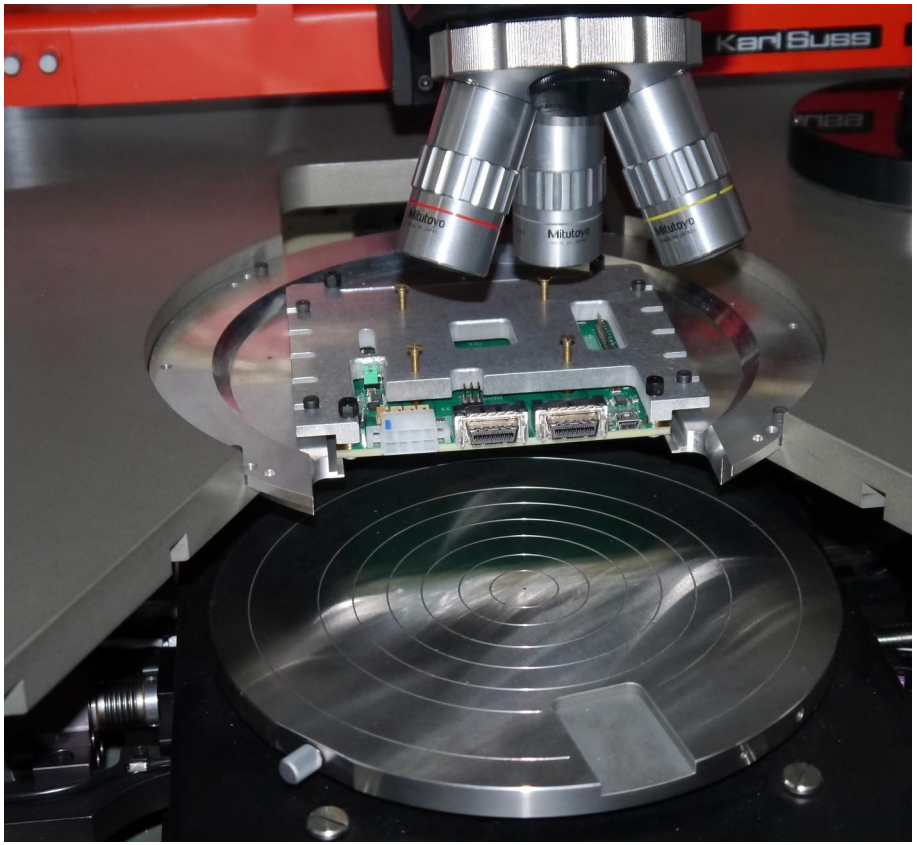
Starting at Q2 '15 –> finishing at ~ Q4 '15 (end of '15)

Outlook to the full scale test system

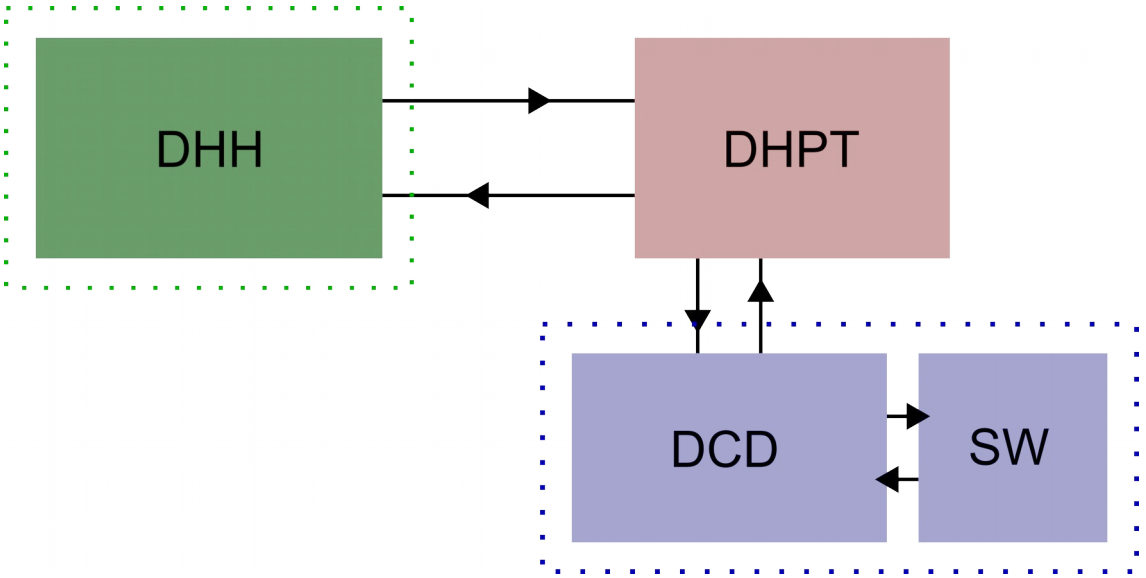
- Automatic test procedure with needle card on a 10x10 chip reticle

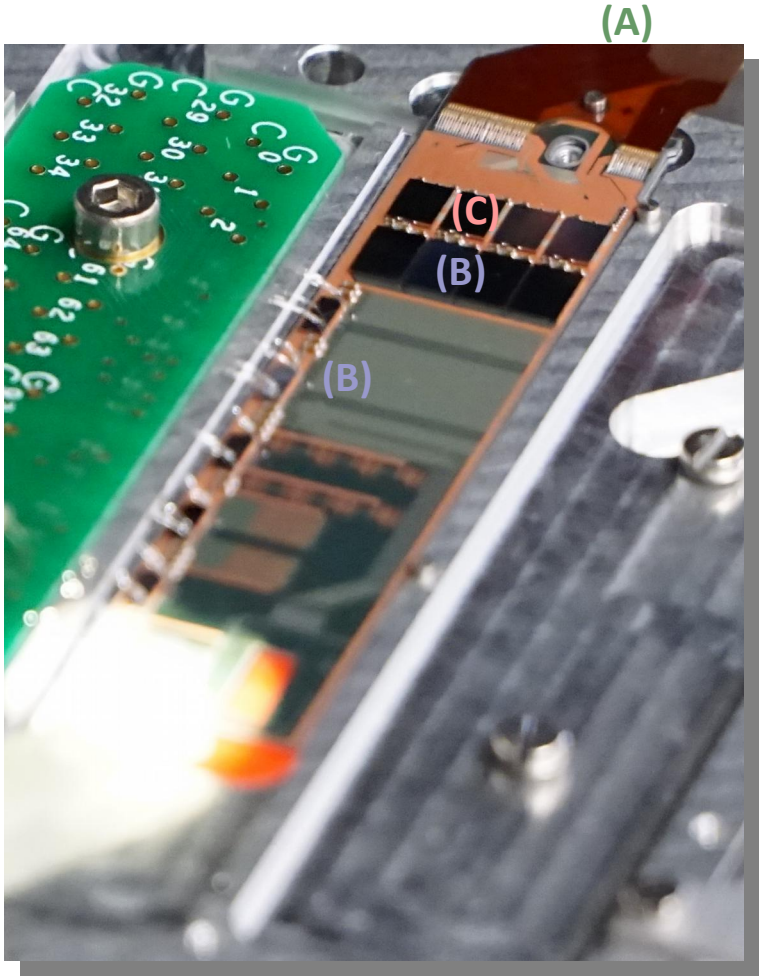


- Automatic movement from chip to chip
- No optical pattern recognition → manual touch down with the needle



Outlook to the full scale test system





- **Full scale test environment**

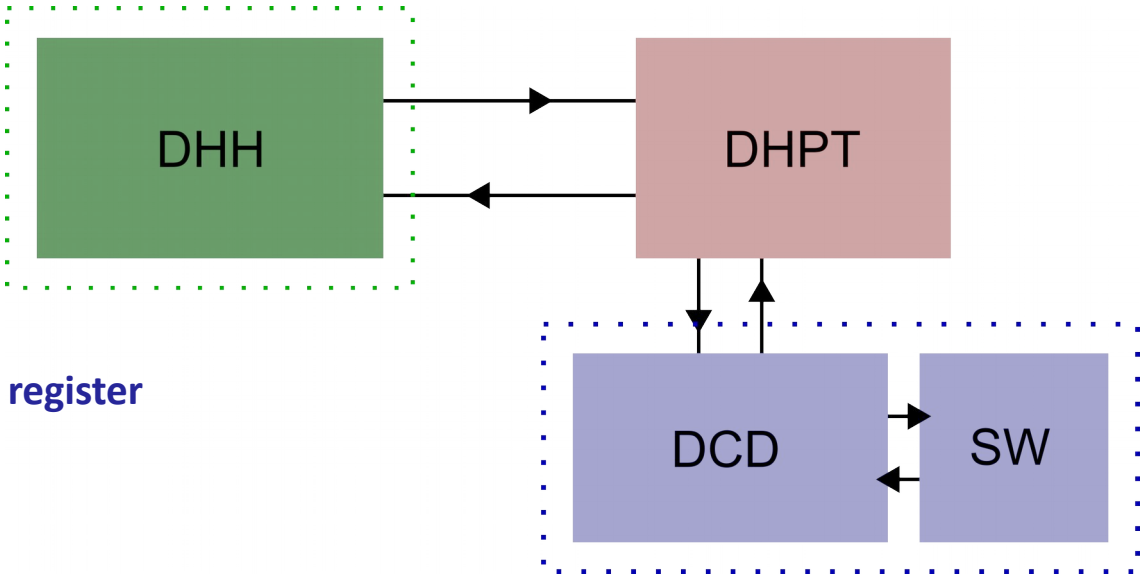
  3 blocks

  JTAG/Link **(A)**

  I/O **(B)**

  Logic **(C)**

Outlook to the full scale test system



JTAG/Link (A)

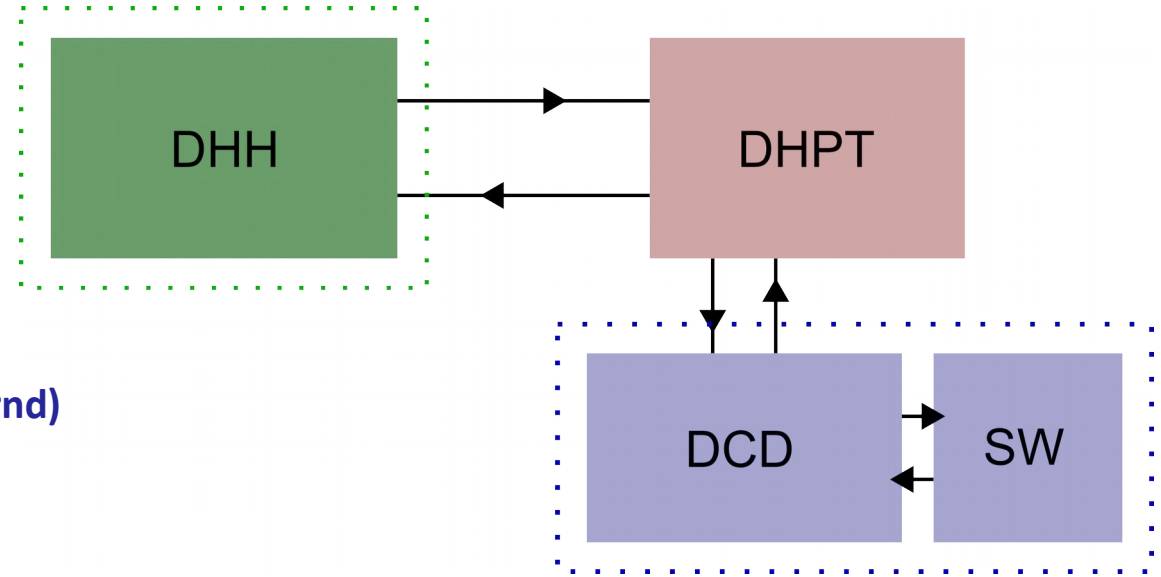
via JTAG:

- Configuration of Global & Core register
- JTAG chain to DCD
- Temperature DACs

Via current consumption:

- Check CML driver DACs (Gbit Serial Link)

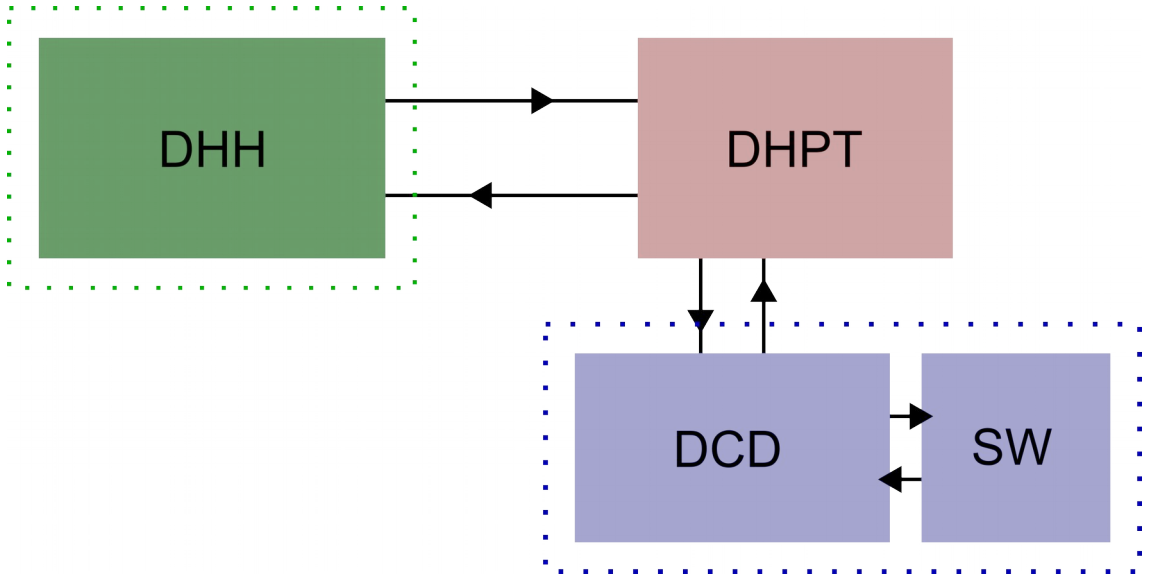
Outlook to the full scale test system



I/O (B)

- DCD data (DCDpp Testpattern and rnd)
- Switcher sequence generator
- DCD Offset bits

Outlook to the full scale test system



Logic (C)

- Zero-suppression
- Occupancy test / stability
- Threshold / hit finder
- SRAM tests
  - standardized pattern, i.e. 0xaa
  - bit error counter (for single bit flip compensation)

Summary

- Full scale testing starts in Q2 '15 (assuming design review in October/November)
- Total estimated testing time ~ 6 months (dependent on the conditions, yield + test routine duration)
  - reasonable is a delivery rate up to 30DHP/week
- Final full scale testing consists of three major blocks

  i.e. I/O tests, JTAG/Gbit Link and Logic tests
- I/O tests already successfully performed on 10 chips → Correct working test algorithm
- Needle card stability tested (→ Nevertheless one additional card as backup is foreseen)

We are in time, but there's a lot more to go for!!!

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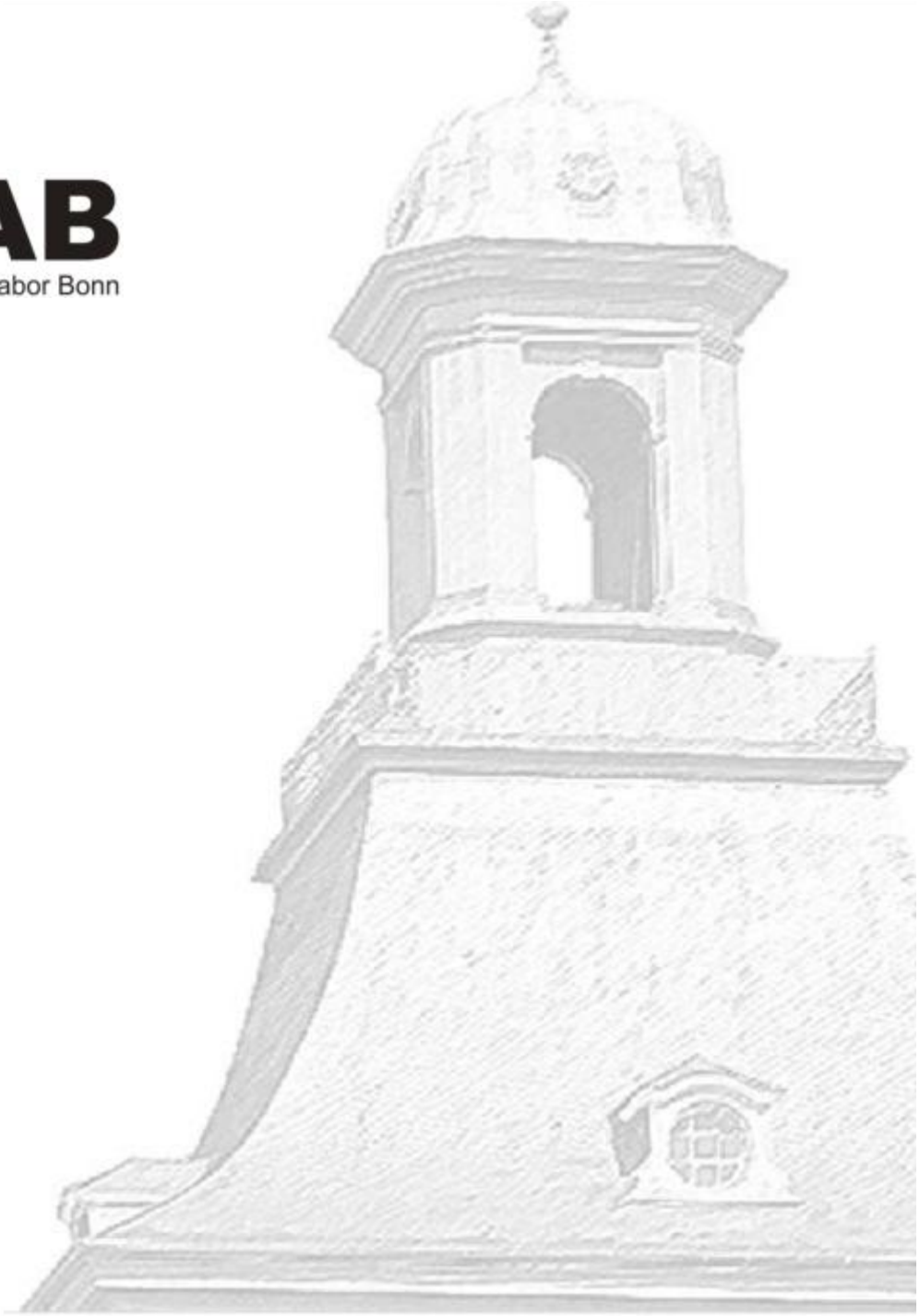

Thank you

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