Interlock

L.Lanceri /INFN Trieste
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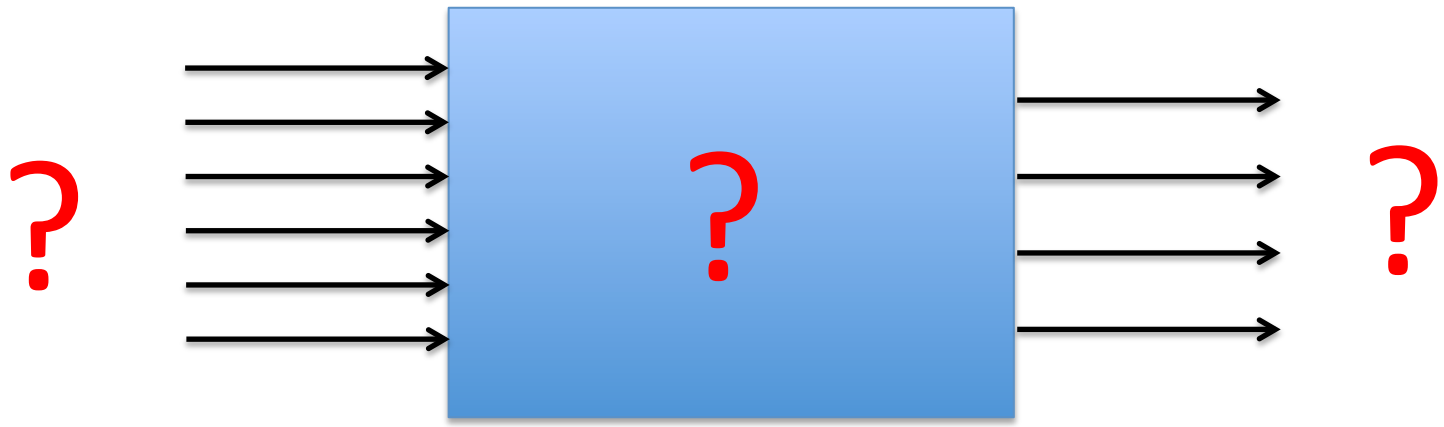
- Who interlocks whom, when ?
- Belle II global, (PXD + SVD) = VXD local

[“Software interlocks” ➔ Slow Control, EPICS]

- Hardware interlock: implementation ?

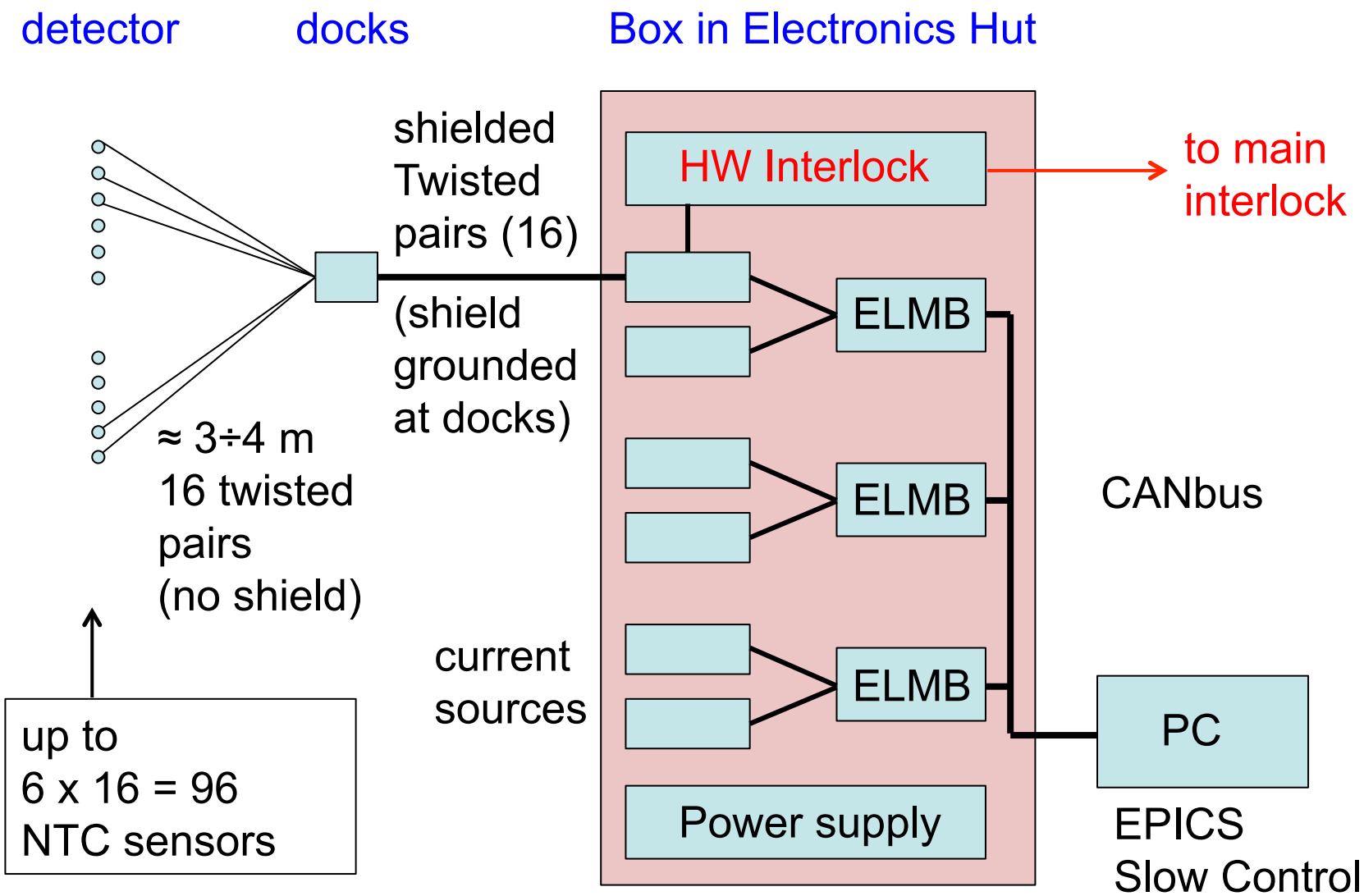


1. WHO INTERLOCKS WHOM, WHEN?

Who ?

- Tentative list of (hardware) interlock sources for VXD
  - VXD/Belle II beam abort
  - SuperKEKB beam abort (injection?)
  - VXD Temperature: NTC thermistors
  - VXD Humidity: sniffers + Vaisala sensors
  - VXD CO_2 cooling plant
  - Earthquake sensors ?
  - Fire detectors in the experimental hall ?
  - … more? Alarms/signals from nearby subdetectors, SuperKEKB, …?
- Software interlocks: EPICS
  - Full conditions information available, programming flexibility
  - Not considered here, it is a separate issue
- A complete list of interlock sources is needed

Example: NTCs ELMB readout & interlock



Whom ?

- Tentative list of (hardware) interlock recipients in VXD
  - PXD power supplies: global or by subsections ?
  - SVD power supplies: global or by subsections ?
  - … more?

- Other recipients of VXD-generated interlocks
  - Global Belle II interlock system ?
  - Neighbor subdetectors ?
  - … others?

- A complete list of interlock recipients is needed

When ?

- In principle, simple logical OR of different sources
  - VXD/Belle II *beam abort*
  - SuperKEKB *beam abort (+ injection?)*
  - VXD Temperature: NTC thermistors, if *temperature above threshold*
  - VXD Humidity: sniffers + Vaisala sensors, if *Dew Point > -30°C*
  - VXD CO_2 cooling plant, *shut down or failure, CO_2 leaks etc.*
  - … etc
- To be implemented in "permit" mode
  - defective connections or missing conditions generate an interlock
- More refined interlock conditions and outputs ?
  - Ramp down only parts of the PXD or SVD ?
  - Flexibility/programmability, implementation issues, see below

Based on 16th B2GM reports

Monitor summary table

Compiled by Nakayama

Group	Slow Control	Env. Monitor	Temperature	Relative humidity	Waterleak	others		Radiation / Beam Loss monitor	radiation monitor	neutron monitor
BP	-	Hiroyuki Nakayama	PT100	-	considered	coolants		Hiroyuki Nakayama	PIN? Scinti? (around QCS)	-
PXD	Michael Ritzert	Carlos Marinas	FOS + NTS thermister	FOS + other (UPS-500?)	-	CO2 leak?		Carlos Marinas	sCVD diamonds	-
SVD	Christian Irmler	Lorenzo Vitale						Lorenzo Vitale		-
CDC	Sadaharu Uehara	Sadaharu Uehara	considered	considered	-	gas		Shoji Uno	-	PD?
BPID	Shohei Nishida	Kenji Inami	considered	considered	-	gas, coolant		Kenji Inami	-	-
EPID	Hidekazu Kakuno	Shohei Nishida	considered	considered	considered	-		Shohei Nishida	-	ELMA diode?
ECL	K.Miyabayashi	K.Miyabayashi	keep Belle-1	keep Belle-1	-	-		V.Zhilich	-	-
Barrel KLM	VPI postdoc	?	-	-	-	gas		Kazutaka Sumisawa and Leo Piilonen	-	-
Endcap KLM	Dmitri Liventsev	Dmitri Liventsev	-	-	-			Tagir Aushev	-	-

S. Uehara (KEK) for data loggers

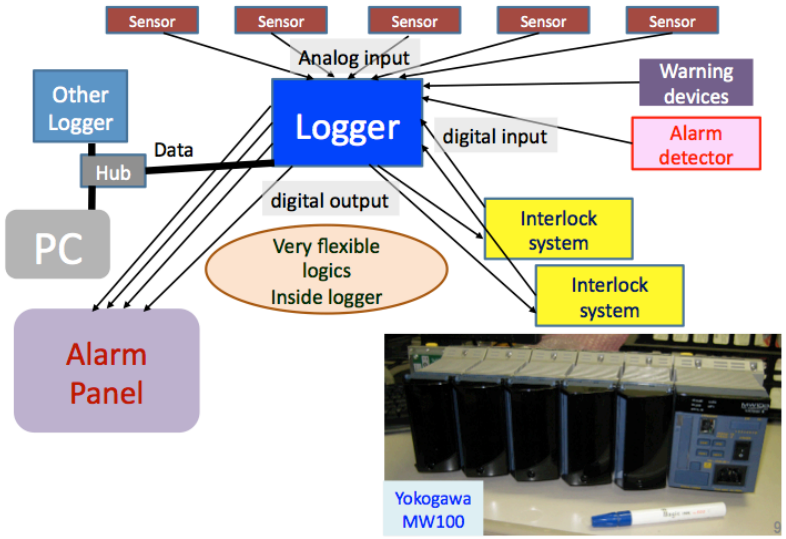
onboard sensors are omitted

Power supply related are omitted

BEAST detectors	
Carlos Marinas	SDD for SR
David Cinavro	PIN diode
Sven Vansen	micro TPC
Sam de Jong	He3-tubes
FaHui Lin	BGO crystals
Peter Lewis	BEAST DAQ

To be updated after this session

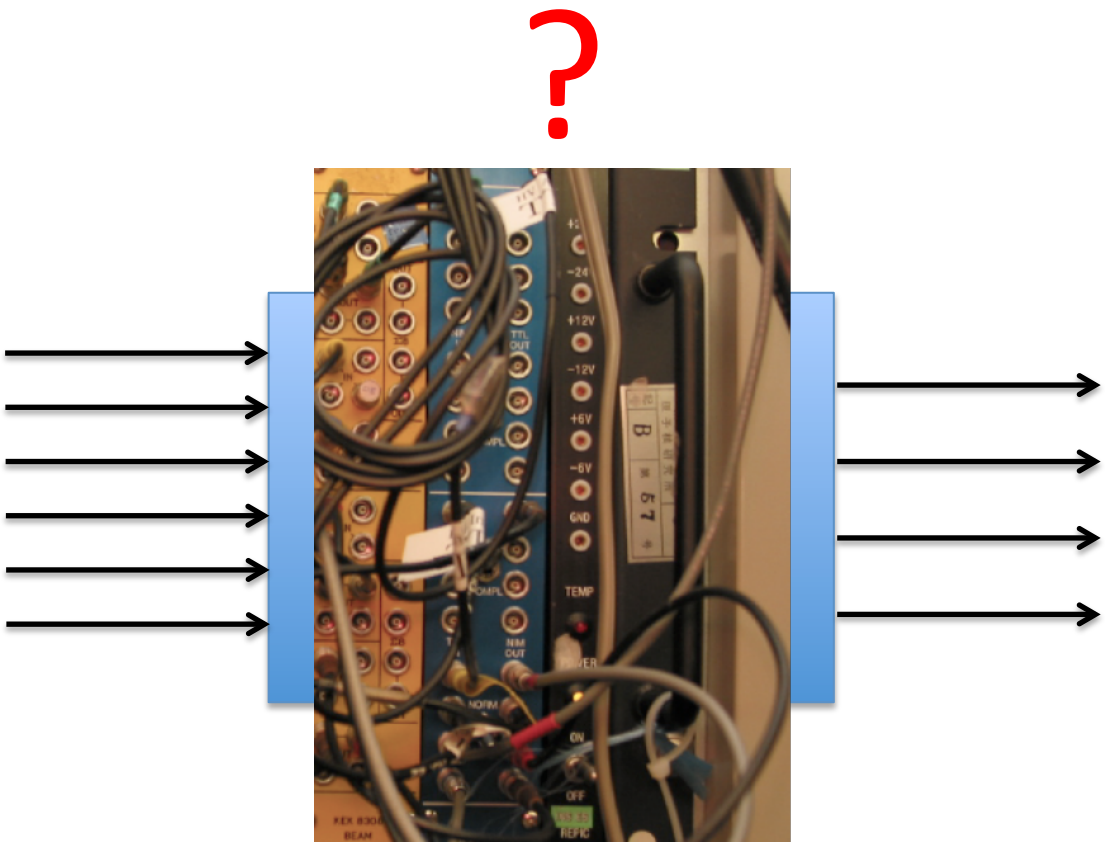
Logger system (hardware)



Nakayama-san is coordinating the overall Belle II Monitoring and Interlocks

see 16th B2GM report (mainly monitoring discussed up to now)

2. BELLE II GLOBAL INTERLOCKS AND VXD…



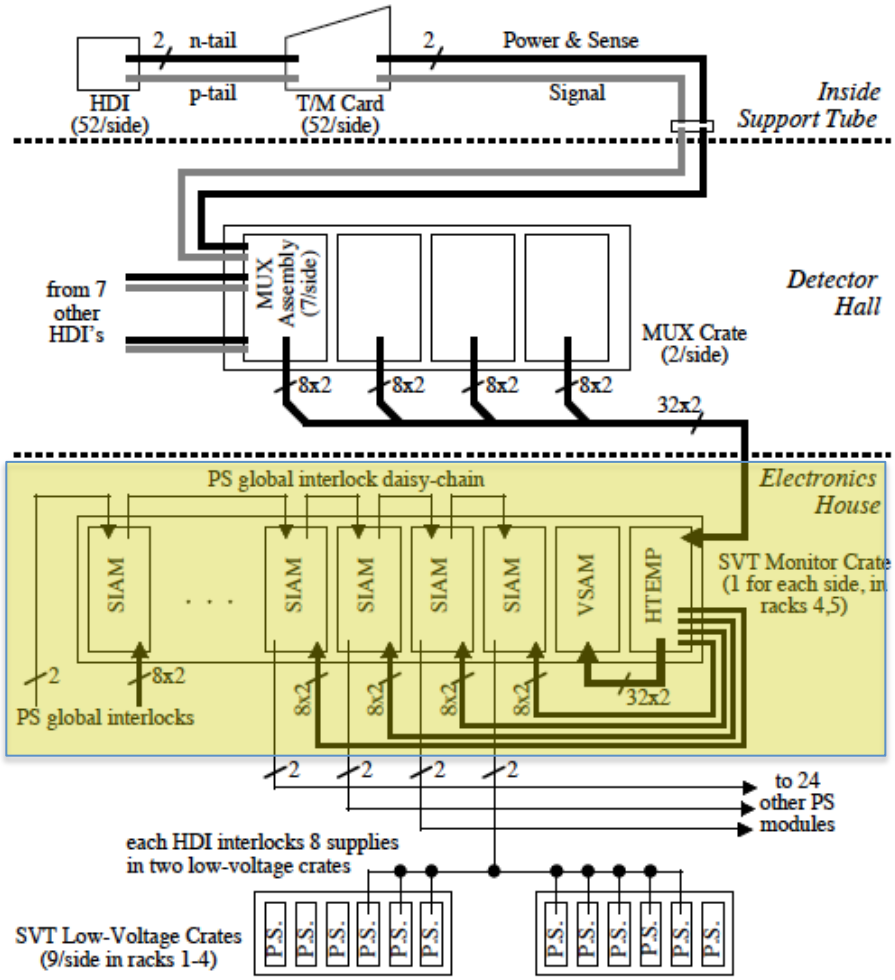
3. VXD HARDWARE INTERLOCK: IMPLEMENTATION ?

VXD Interlock Implementation ?

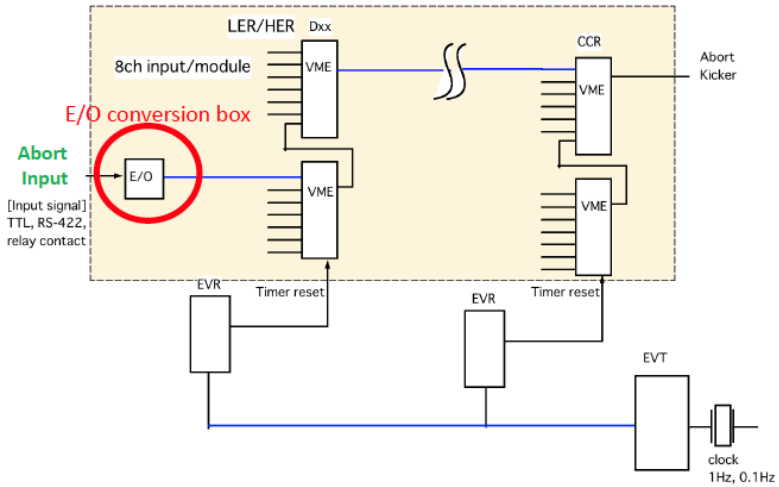
- Requirements, in order of priority:
  - Reliability, availability of spares, uniformity across Belle II/SuperKEKB
  - Independence from network & software
  - Some flexibility/programmability
    - partial interlocks ?
    - evolving interlock conditions and requirements ?
- Possible implementations, in order of complexity:
  - Hardwired OR of inputs (standardized across Belle II ?)
    - Examples: SIAM modules in BaBar, Beam Abort units in SuperKEKB
  - More complex decision logics (i.e. FPGA-based), custom made or commercial (standardized across Belle II ??)
  - Industry-standard, commercial Programmable Logic Controllers (PLC)
    - For instance Siemens PLCs, adopted by some experiments

“Low end” implementation examples

BaBar/PEP-II “SIAM” modules



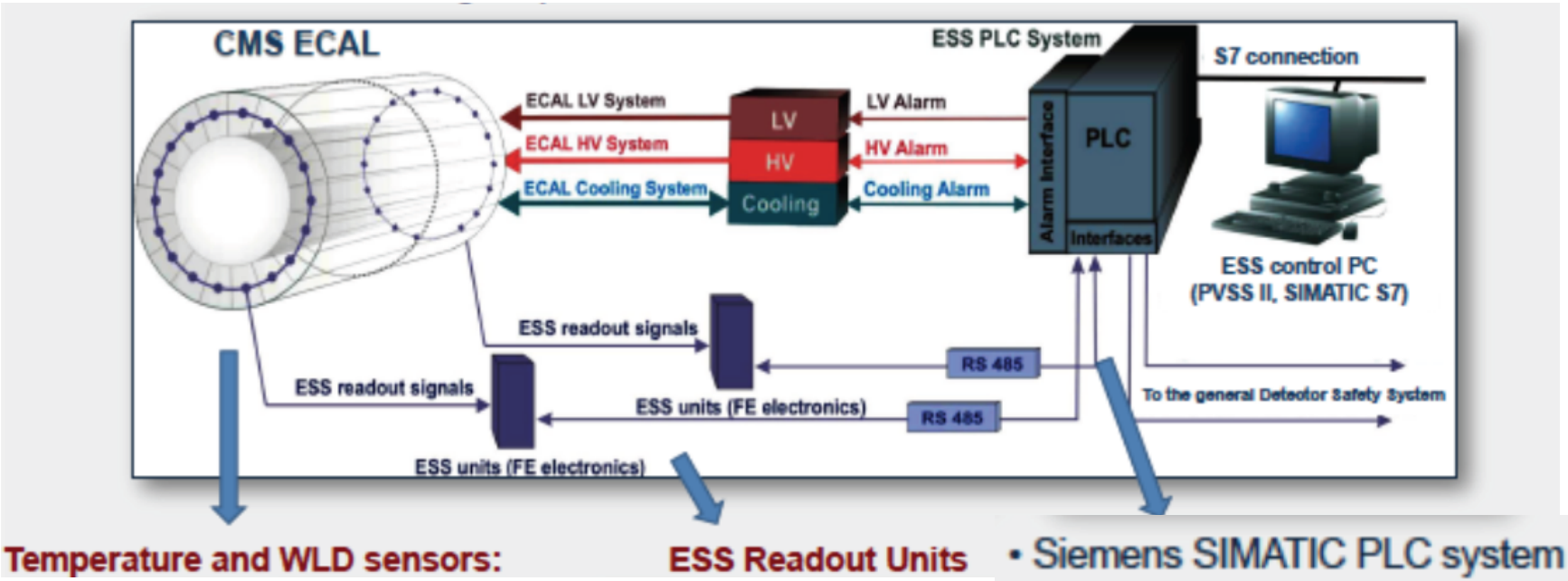
SuperKEKB abort modules



In both cases, essentially hardwired ORs of inputs

“high end” implementation example

Siemens PLC (Programmable Logic Controller)
in a subdetector at LHC



- Siemens SIMATIC PLC system (S7-400H and S7-300 family)
- Redundant system
  Effective MTBF ~ 10 years
- Fault-tolerant / Fail-secure
- Digital filtering (2nd IIR NF filter)

PLCs (or similar approaches) an overkill?

It depends on the global Belle II decisions

Conclusions, To Do

- Who? a complete list of interlock sources is needed
  - VXD Temperature, humidity, leaks, …; Belle II, SuperKEKB
- Whom? a complete list of interlock recipients is needed
  - PXD, SVD power supplies, (granularity), …; Belle II, SuperKEKB
- When? interlocking conditions need to be defined
  - (thresholds, combined conditions, etc.)
- Implementation
  - Reliability; some flexibility (masks etc.); uniformity across Belle II !