Karlsruher Institut für Technologie

Belle II

Online-Cluster-Analysis on FPGAs for recovery of slow pions

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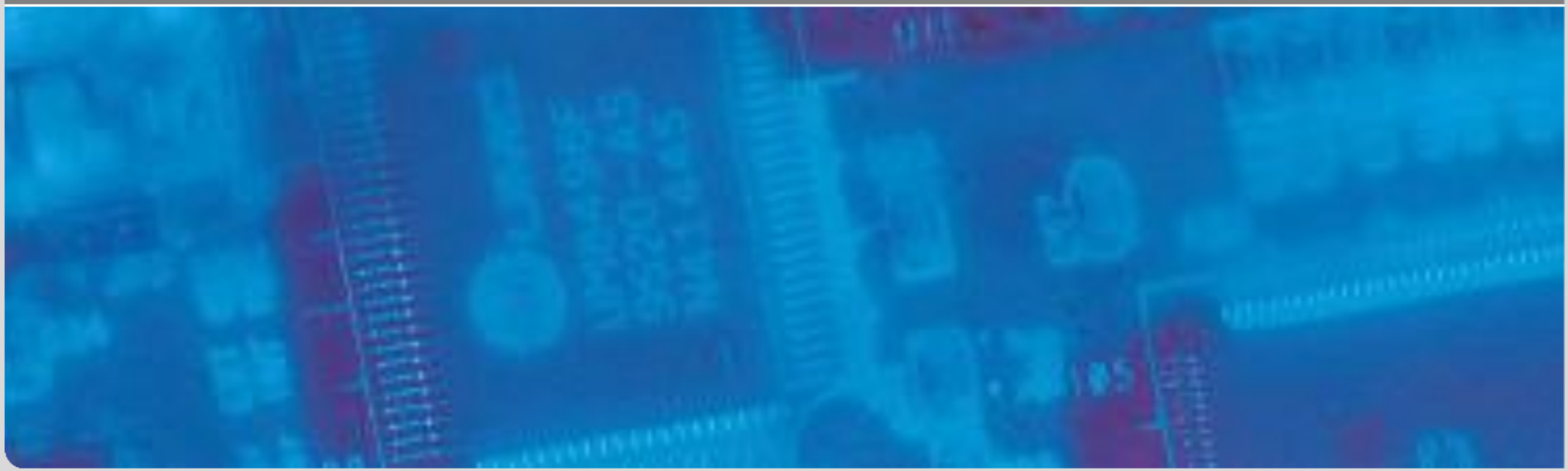
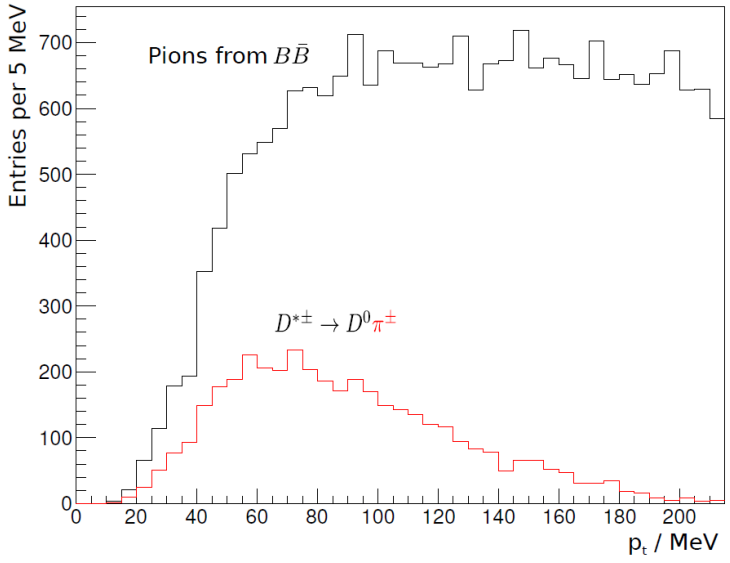
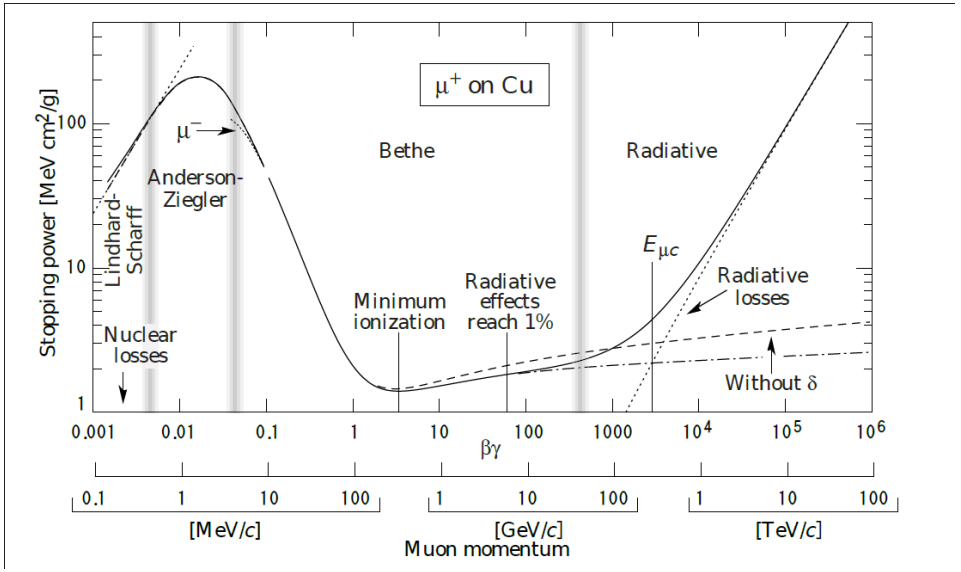


D* Decay in VXD

- Particles with low impuls experience high stopping power
- D* decays produce pions with low transversal momentum
  - Below 60 MeV majority of the pions attributed to to this decay





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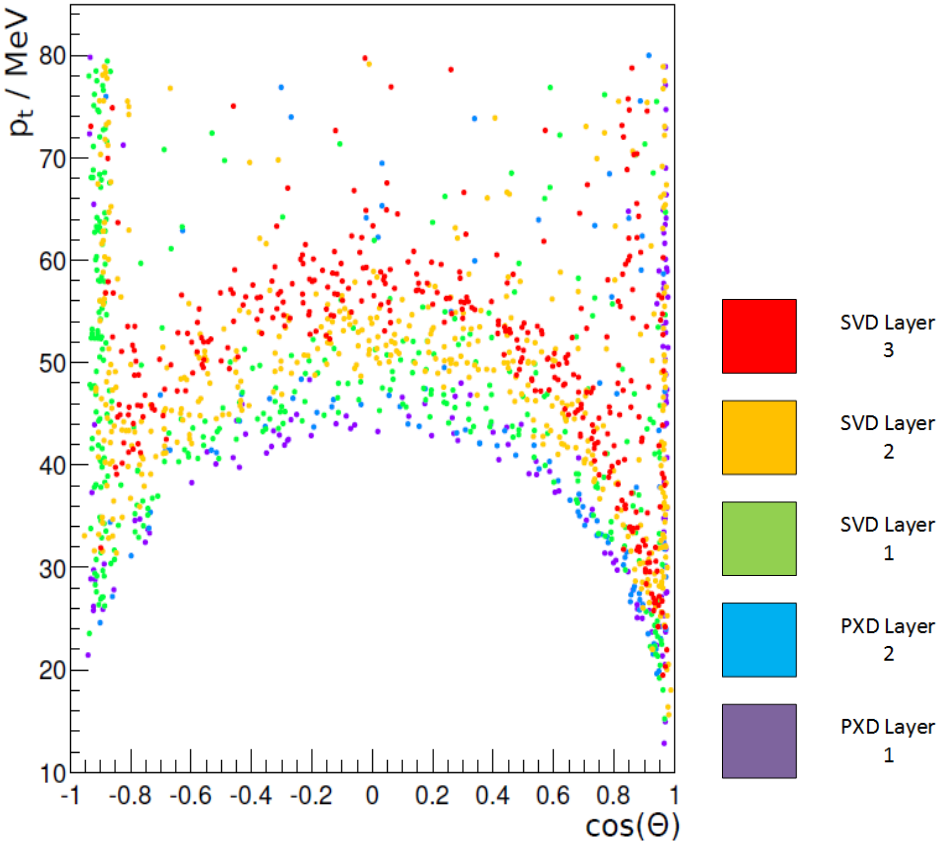
Momentum Distribution of Slow Pions

- P_t < 60 MeV may already be insufficient to reach all SVD Layers
- PXD Hits of slow pions will get lost since no RoI is built
- Recovery mechanism necessary



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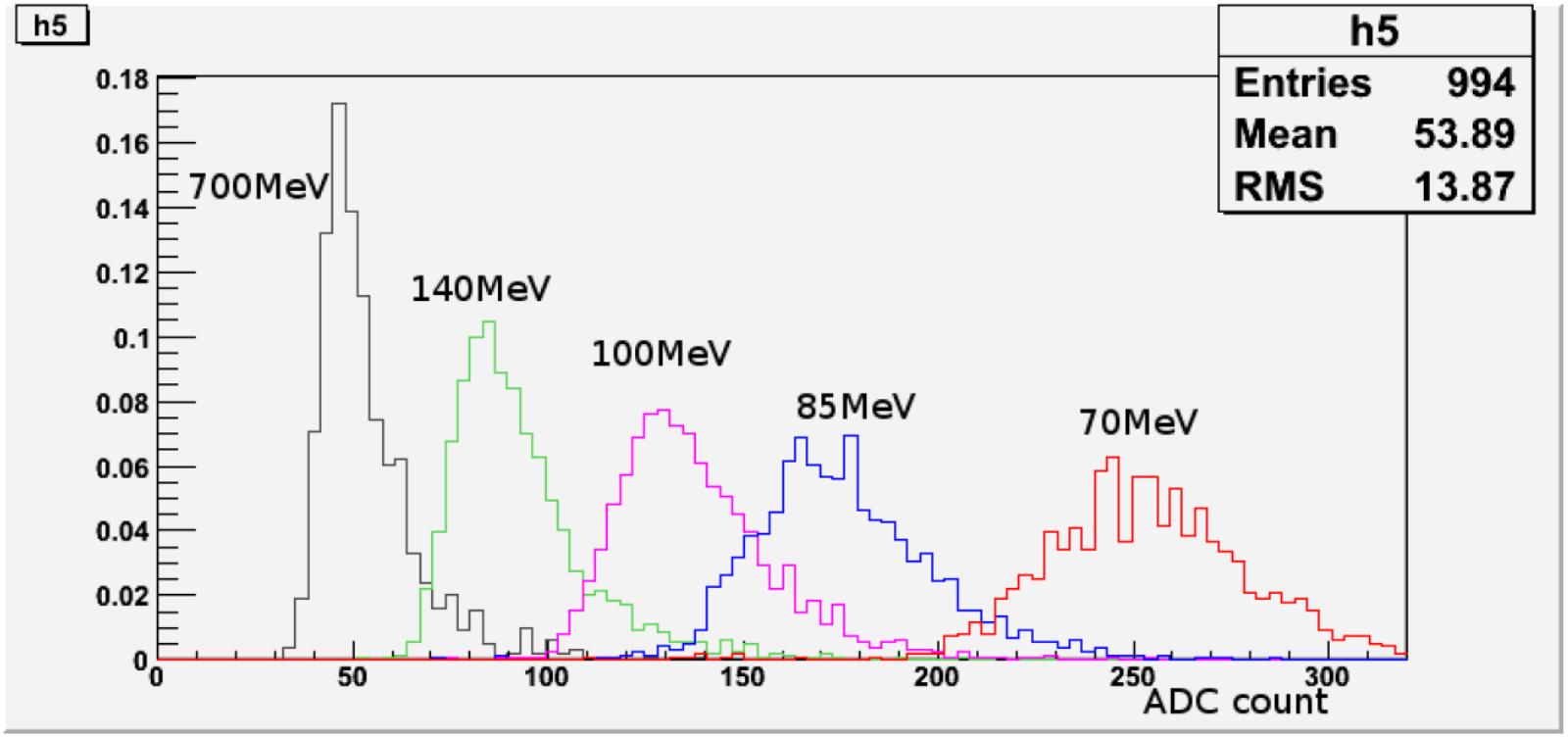
Charge of slow Pions with PXD

- Use charge deposit in PXD for different momenta tracks to separate pi from mip



Charge deposit for different momentum

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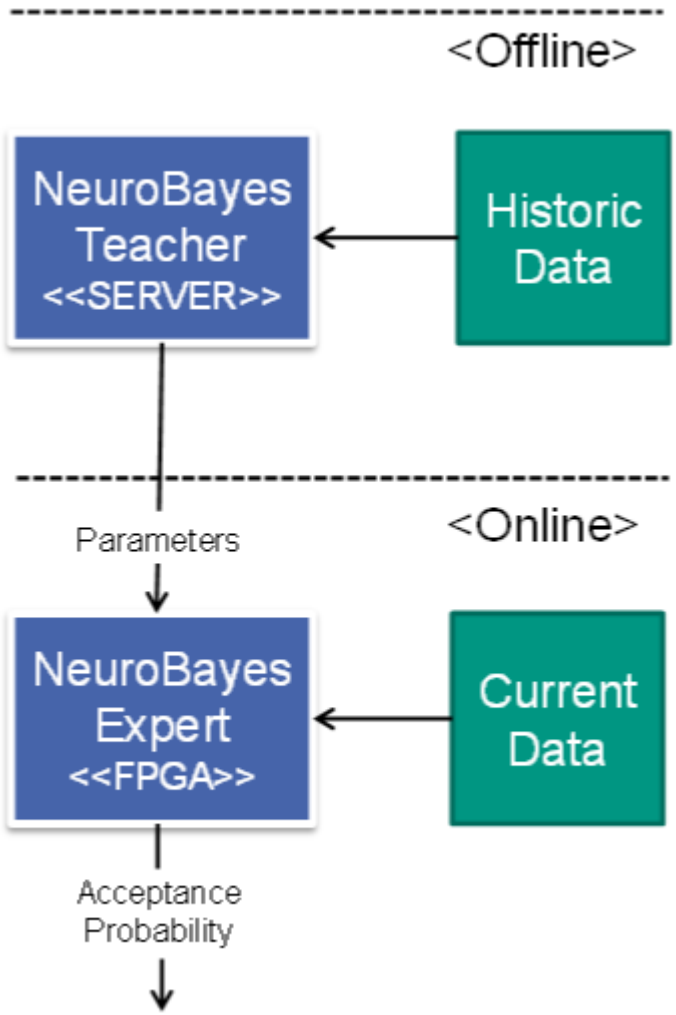
Algorithm for Recovery of slow pions

- Usage of the NeuroBayes Algorithm to predict Slow Pions by using cluster features

- Training
  - Usage of Simulated Clusters
  - Conducted Offline

- Prediction
  - Usage of Detector Data



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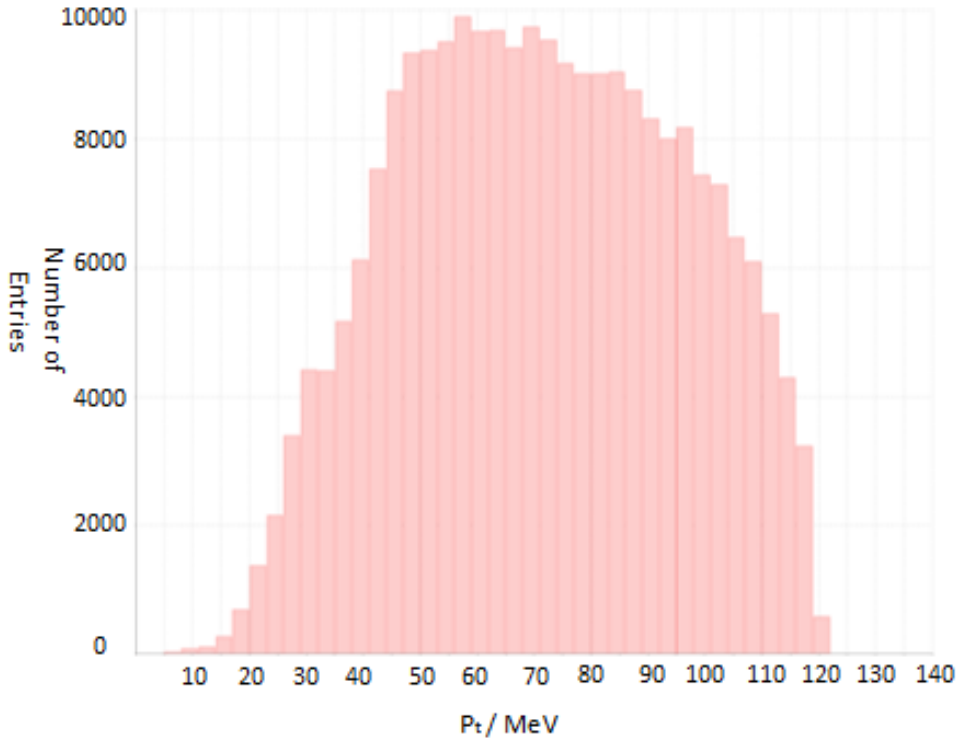
Cluster Data used for Recovery

- Charge deposition of Clusters can be supplemented by additional Information
  - Additional information about the charge in a cluster
  - Spreading of clusters in the PXD
  - Features have different impacts on the result

Cluster Feature	Importance
Total Charge	1st
Standard Deviation	8th
Maximum Pixel Charge	5th
Minimum Pixel Charge	3rd
Length in Z	4th
Length in Phi	6th
Total Length	2nd
Number of Pixels	9th
PXD Layer	7th

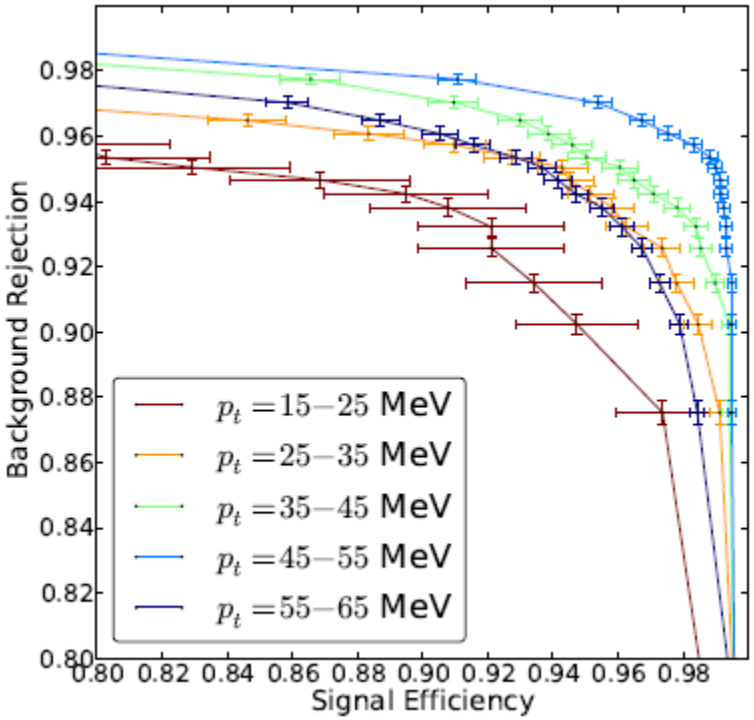
Sample used for NeuroBayes Training

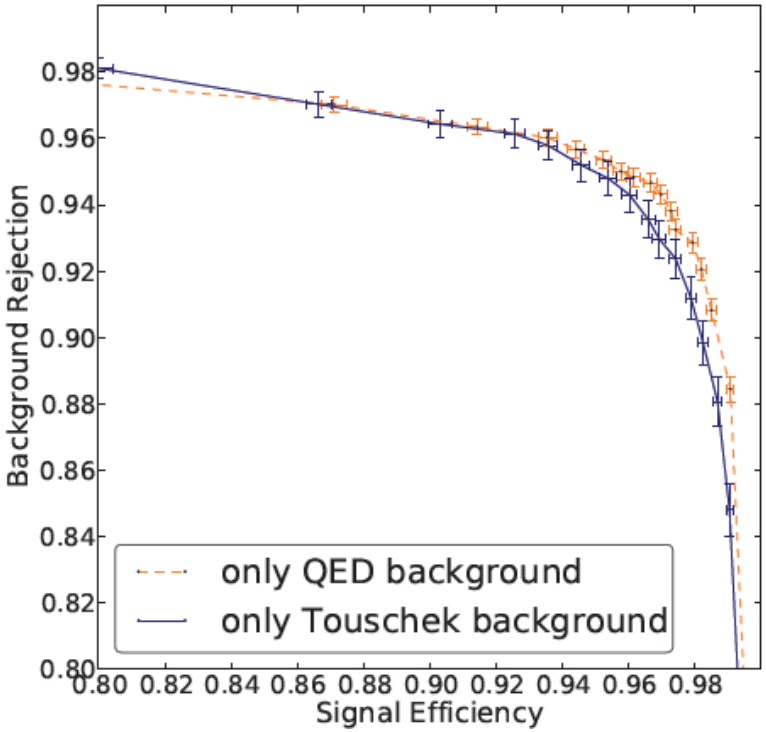
- The Pion Sample covers the transversal impuls of pions not reaching the outer Layers
- Background includes QED, Touschek and Coulomb



NeuroBayes Performance

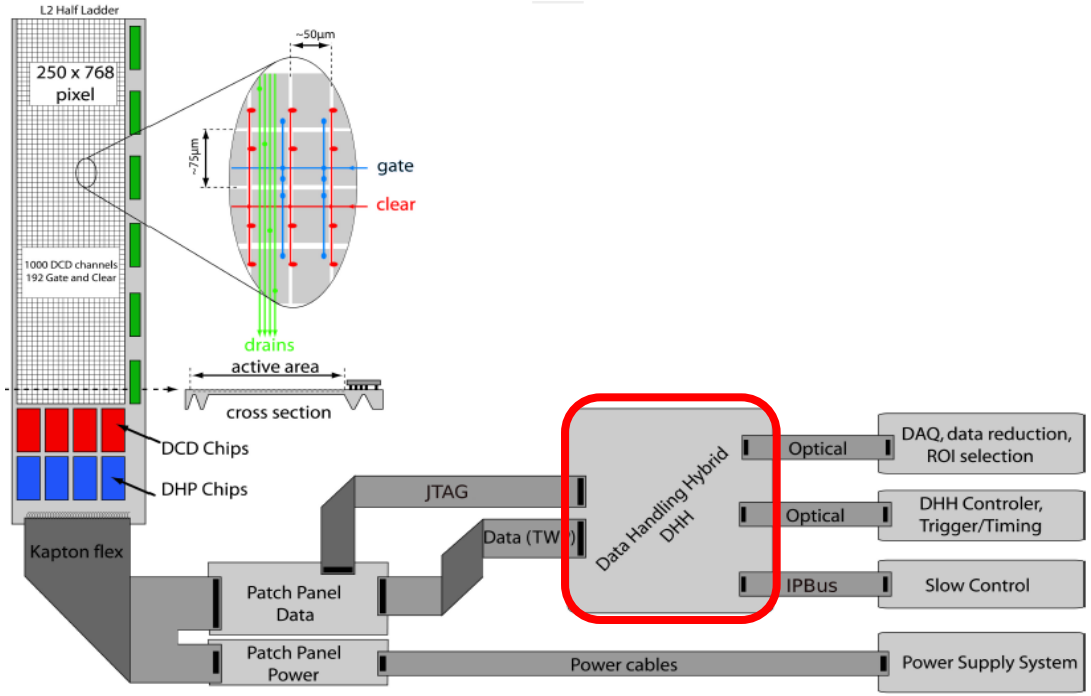
- NeuroBayes achieves good Signal Efficiency and Background Rejection Ratios for pions with $P_t < 65$ MeV





Using the NeuroBayes at the PXD

- Algortihm needs to handle the data rates
  - Usage of FPGAs with guaranteed Throughput
- Needs to be placed close to the readout of PXD
  - FPGAs of DHH has free resources



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Challenges for the Implementation on FPGA

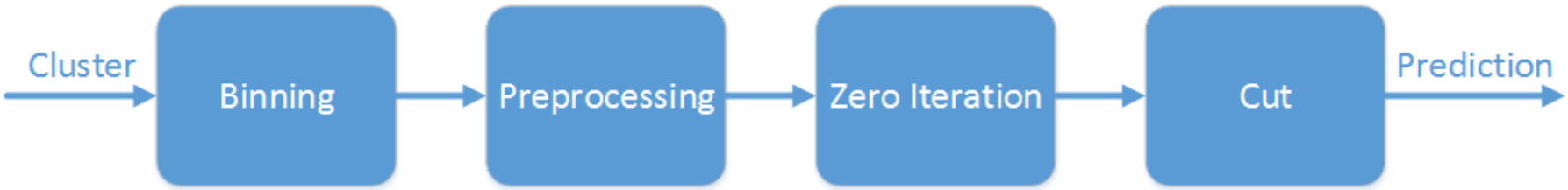
- Performance
  - Interface is clocked with 200 MHz
  - 1 Cluster / Clock Cycle has to be able to be achieved
- Resources
  - 30 % of the CLBs available
  - 50 % of the DSPs available
- Quality
  - Output of FPGA Implementation cannot differ to much from Software

Cluster Processing Pipeline

- Incoming Clusters are passing through a processing pipeline
  - Protocol Handling for the Interface to the DHH‘s Clustering
  - Computation of Cluster Features for the NeuroBayes
  - NeuroBayes Expert makes the decision and passes it to the output interface

Overview of NeuroBayes on FPGA

- The NeuroBayes Expert consists of 4 major components
  - Binning of the Cluster Features
  - Preprocessing by using CDF
  - Zero-Iteration done by vector multiplication
  - Cut on the Ouput



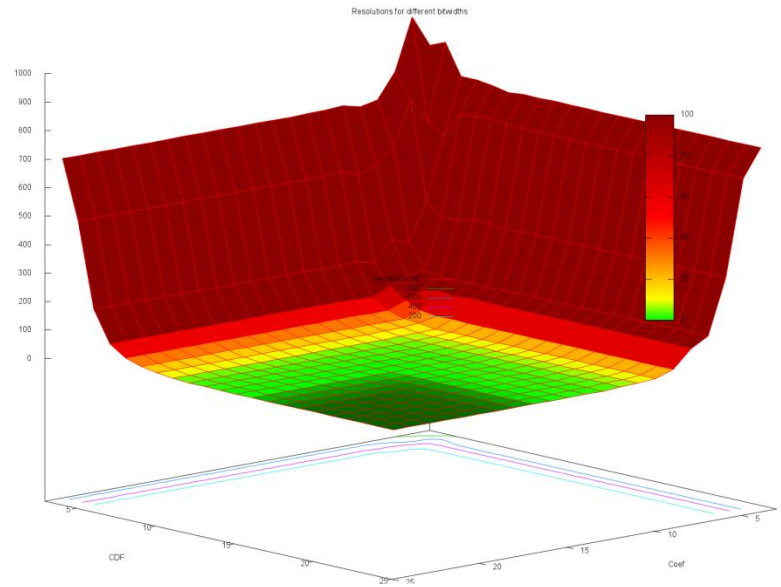
Conversion to Fixpoint

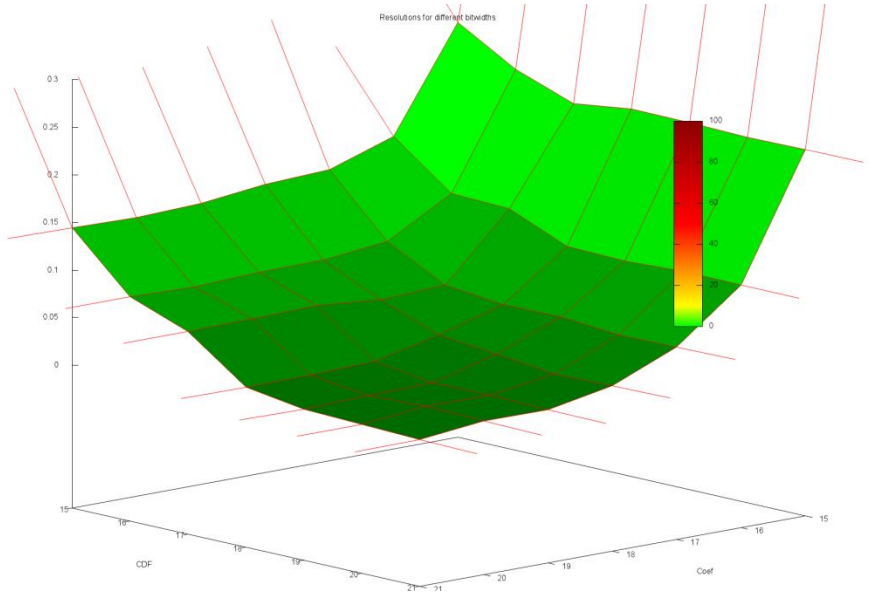
- Original NeuroBayes Algorithm uses Floating Point
  - Usage on FPGA requires more ressources and impacts latencies
  - Transformation to fixpoint is more efficient, but impacts the quality

- Quality of a Fixpoint implementation‘s Output depends on the used bitwidth
  - Higher Bitwidth equals higher consumption of Ressources, while increasing Quality
  - DSPs have 25*18 Bit Inputs

Evaluation of Fixpoint Implementation

- Usage of 25*25 Bitwidth results in no difference of output to floating point implemenation
- Difference is small for 25*18
  - Most resource efficient configuration for multiplication
  - Difference is at 1.5 * 10^-5





Evaluation of Performance

- Computation of the Algorithm takes several clock cycles
  - Performance requirements cannot be met
- Usage of Pipelining throughout the implemenation
- Fixpoint Vector Multiplication is the critical path
  - High Frequency through usage of cascading DSPs

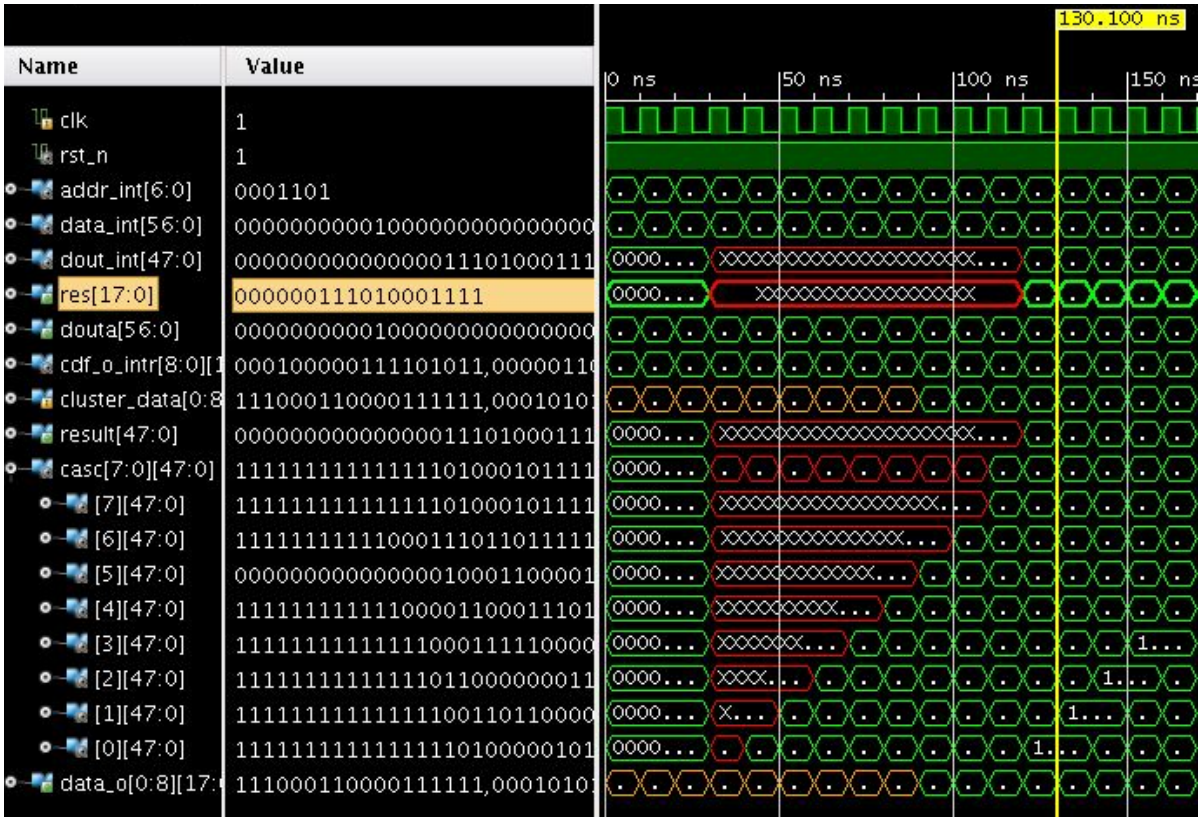
Component	Latency	Frequency
Cluster Feature	1 cycle	446 MHz
Preprocessing & Binning	1 cycle	446 MHz
Vector multiplication	9 cycles	350 MHz
Cut	1 cycle	446 MHz
Total	**12 cycles**	**350 MHz**

Ressource Consumption

- Critical Path for CLBs in the implemenation is the Binning and Preprocessing
  - Mostly Usage of Look Up Tables
- Usage of DSPs for vector multiplication makes life easier
  - 50 % of DSPs are still available
  - Each multiplication needs one DSP

Ressource	Demand	Constraint
DSP	3,125 %	< 50 %
CLB	~ 2 %	< 30 %

Simulation



Cluster Feature	Value
Total Charge	425
Standard Deviation	49
Maximum Pixel Charge	135
Minimum Pixel Charge	23
Length in Z	2
Length in Phi	2
Total Length	1
Number of Pixels	4
PXD Layer	2

Result of Software is:
00000011101000111100100001 -> slow Pion Cluster
(S)DDD,DDDDDDDDDDDDD

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Summary

- Recover slow Pions using FPGAs near PXD
- FPGA-Implementation is sufficient
  - Quality : Difference < 1.5 * 10 ^ -5
  - Throughput : 350 Mio Cluster per secons
  - Resources : ~ 2 % CLBs , ~3 % DSPs
- Integration into DHH

Demo

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