Simulations for SiMPl devices with active quenching

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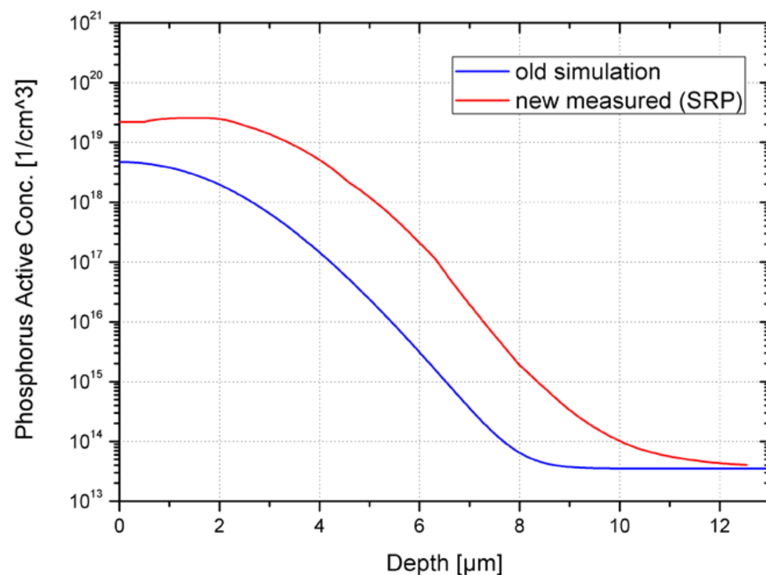
Static Simulations – R_Q



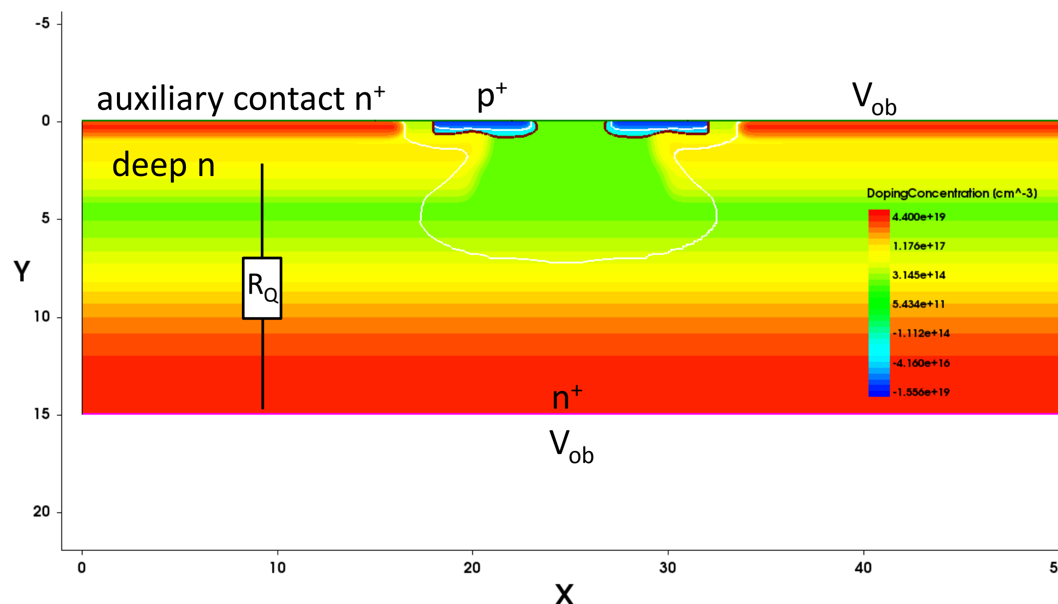
new backside profile for simulations

→ higher doping concentration

→ smaller resistance expected

static simulation

- ramping of central auxiliary contact $V_{bd} \rightarrow V_{ob}$
- IV-curve for resistance and linearity



Static Simulations – R_Q

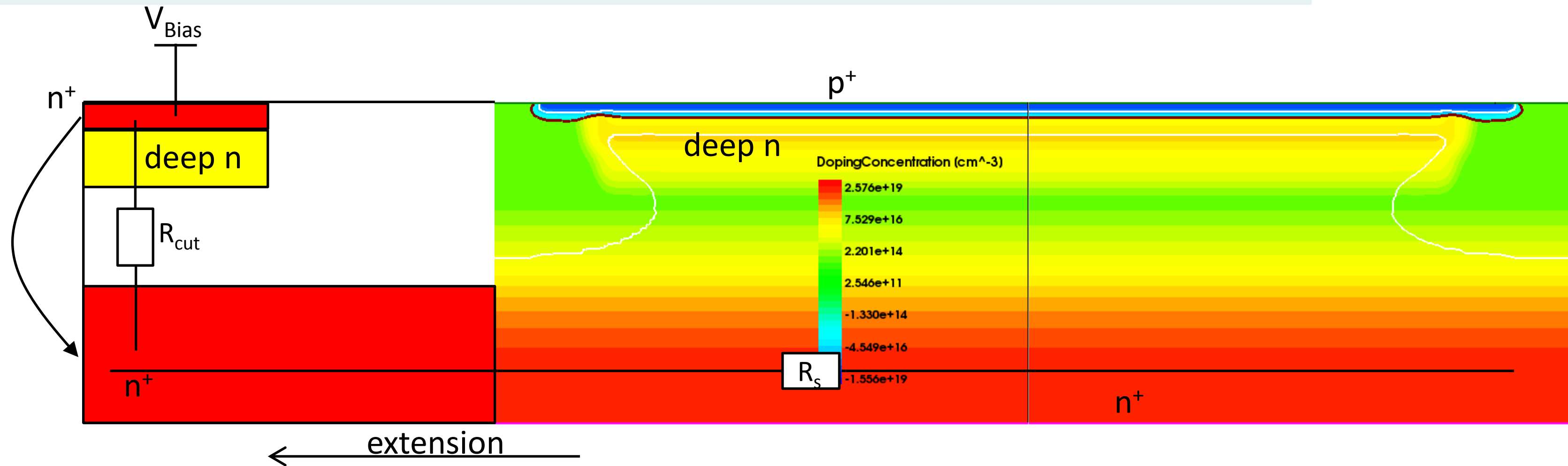
Annealing Scenario	Thick um	Pitch um	Gap um	Bulklvl 1/cm^3	Rquench Ohm	R^2
11	11	50	10	3.51E+13	13.23155	0.99988
4	11	50	10	3.16E+13	14.93085	0.99991
4	11	50	10	3.51E+13	14.92576	0.99992
4	11	50	10	3.86E+13	14.92068	0.99992
11	13	50	10	3.51E+13	81.13606	0.99482
4	13	50	10	3.16E+13	81.55187	0.99611
4	13	50	10	3.51E+13	81.3905	0.99614
4	13	50	10	3.86E+13	81.22973	0.99618
11	15	50	10	3.51E+13	369.0609	0.98324
4	15	50	10	3.16E+13	362.3192	0.9832
4	15	50	10	3.51E+13	359.8857	0.98347
4	15	50	10	3.86E+13	357.4805	0.98374
11	17	50	10	3.51E+13	1171.727	0.97371
4	17	50	10	3.16E+13	1180.422	0.97209
4	17	50	10	3.51E+13	1161.97	0.97293
4	17	50	10	3.86E+13	1144.004	0.97375
11	20	50	10	3.51E+13	4032.439	0.96879
4	20	50	10	3.16E+13	4251.978	0.96588
4	20	50	10	3.51E+13	4098.02	0.96791
4	20	50	10	3.86E+13	3953.026	0.9698
11	7	50	10	3.51E+13	0.83326	1
4	7	50	10	3.16E+13	0.82835	1
4	7	50	10	3.51E+13	0.82835	1
4	7	50	10	3.86E+13	0.82834	1
11	9	50	10	3.51E+13	3.35012	0.99999
4	9	50	10	3.16E+13	3.25649	1
4	9	50	10	3.51E+13	3.25637	1
4	9	50	10	3.86E+13	3.25625	1
4	15	50	16	3.16E+13	504.4965	0.98203
4	15	50	16	3.51E+13	500.9314	0.98232
4	15	50	16	3.86E+13	497.4089	0.98261

Summary:

Wafer 4 Thickness [µm]	R_q [Ohm]	Deviation from Bulk (10%)	Gap(16)	R^2
9	3.25	0		1
11	14.925	0.005		0.99992
13	81.39	0.16		0.99614
15	359.88	2.4	500	0.98347
17	1161.97	17		0.97293
20	4098	150		0.96791

- negligible influence of bulk variation
- thicknesses up to 15µm provide R < 1kΩ
- resistance scales to gap in accordance with equation
- very linear behavior

Sheet resistance



<u>cutting edge biasing:</u>

- extension of chip to sides → deep n and additional n^+ implant at the edge
- biasing of backside via this topside n^+ contact

→ vertical and lateral resistors important (possible voltage drop over chip length)

- R_{cut} similar to previous R_Q and can be chosen freely by area of n^+
- lateral resistor R_s = sheet resistance

→ rough calculation: ≈ 6Ω   simulation: ≈ 8Ω

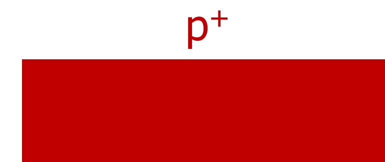
→ should not pose a problem for biasing

Dynamic Simulations

Basic idea:

- creation of charge according to the diode capacitance within the high field region
- now also with realistic creation time span ≈ 100ps
- calculation of C_Q with the displacement current

p^+



eq. charge

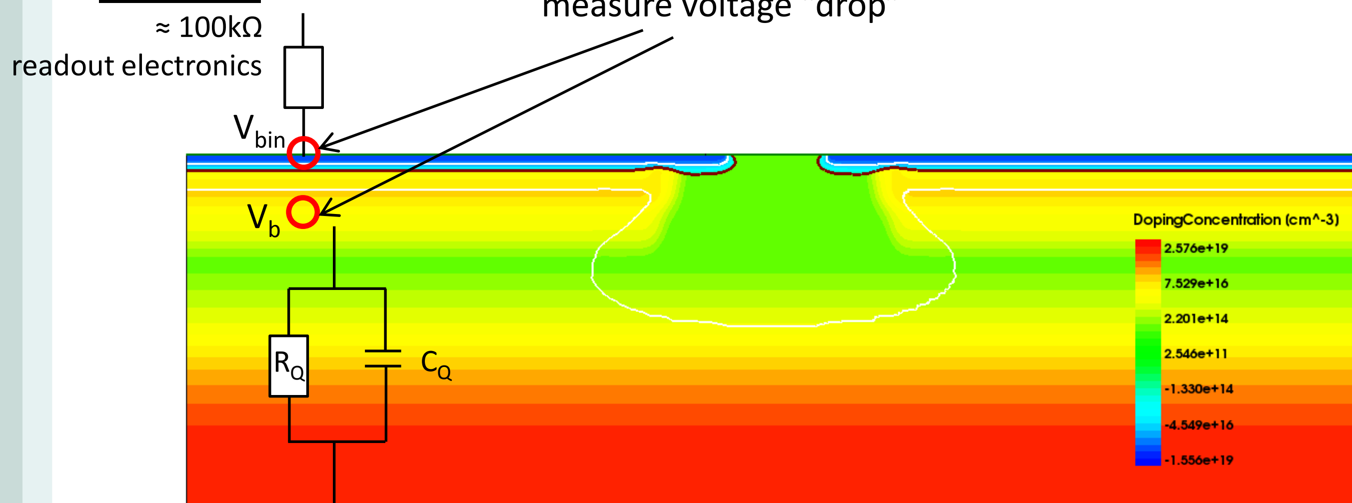
deep n

R_Q

displacement current

Problem: Ansatz only valid for high resistivity material

Concept:



Dynamic Simulations

<u>Results:</u>

Annealing Scenario	Thick um	Pitch um	Gap um	V_b V	V_bin V	C_Q F	C_D F
4	11	50	10	0.1067	4.06E+00	1.68E-13	1.14E-13
4	13	50	10	0.3841	3.90E+00	5.69E-14	1.16E-13
4	15	50	10	0.8138	4.14274	3.23E-14	1.20E-13
4	17	50	10	1.071	3.69943	2.36E-14	1.27E-13
4	20	50	10	1.4319	3.51078	1.68E-14	1.39E-13
4	9	50	10	0.0117	3.52655	7.89E-13	1.18E-13

But:

- current behavior dominated by high ohmic top side
- bulk resistor very low ohmic

→ impedance of “C_Q“ much larger (>>1kΩ) compared to “R_Q”
→ “R_Q” dominates the bulk
→ “C_Q“ almost redundant

→ possible new model approach without C_Q and only featuring a series resistor for the bulk

Summary

Backside resistance:

- new backside profile → reduced resistance values with marginal deviations
- should also pose no problem for cutting edge biasing (small sheet resistance (≈7Ω))

→ suggested thickness for devices:
15µm → R_{bulk} = 360Ω

Dynamic simulations:

- for 15µm thickness: $C_Q \approx$ 32fF
- behavior in the bulk dominated by R_{bulk}
- C_Q almost redundant

→ possible new model approach without C_Q and only featuring a series resistor for the bulk R_{bulk}