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SI LAB
Silizium Labor Bonn

DHPT
status and plans

Tomasz Hemperek

hemperek@uni-bonn.de

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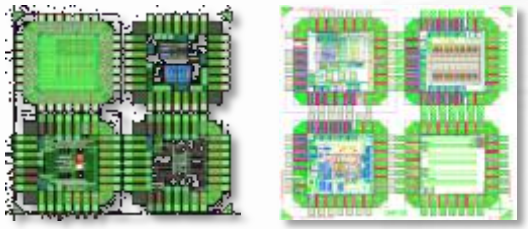
DHPT subbmision

Test chips for **custom IP verification**

- Two mini@sic submissions in 2011 and 2012
- 1.6GHz PLL
- Gigabit link driver
- LVDS transmitter & receiver
- Pixel matrices with analog front-ends (CSA + comp.)
- In pixel ADCs

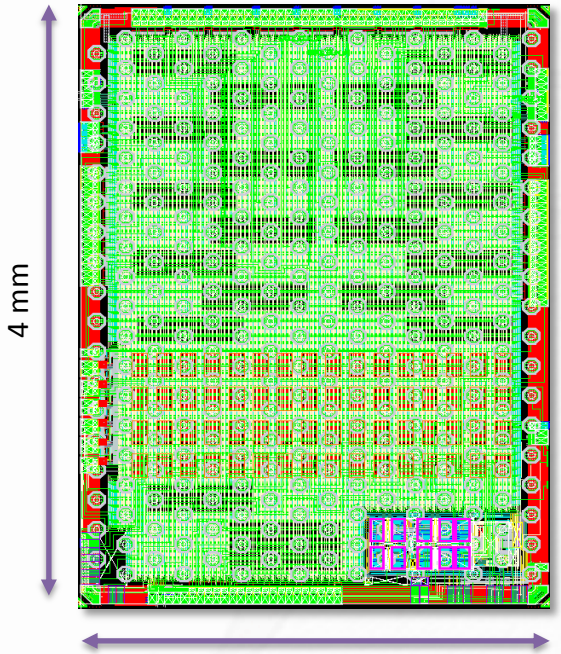


DHPT 0.1 and DHPT 0.2 test chips

DHPT 1.0, **first production version**

- MPW submission in Aug. 2013
- 12 mm^2 area, C4 bumps, 200µm pitch

- >300k Gates, >3MB SRAM
- PLL, 1.6Gb/s serial link, CML preamhasis
- Reference
- >100 LVDS and HSTL IO
- DACs, ADC
- ...



Data handling processor DHPT 1.0

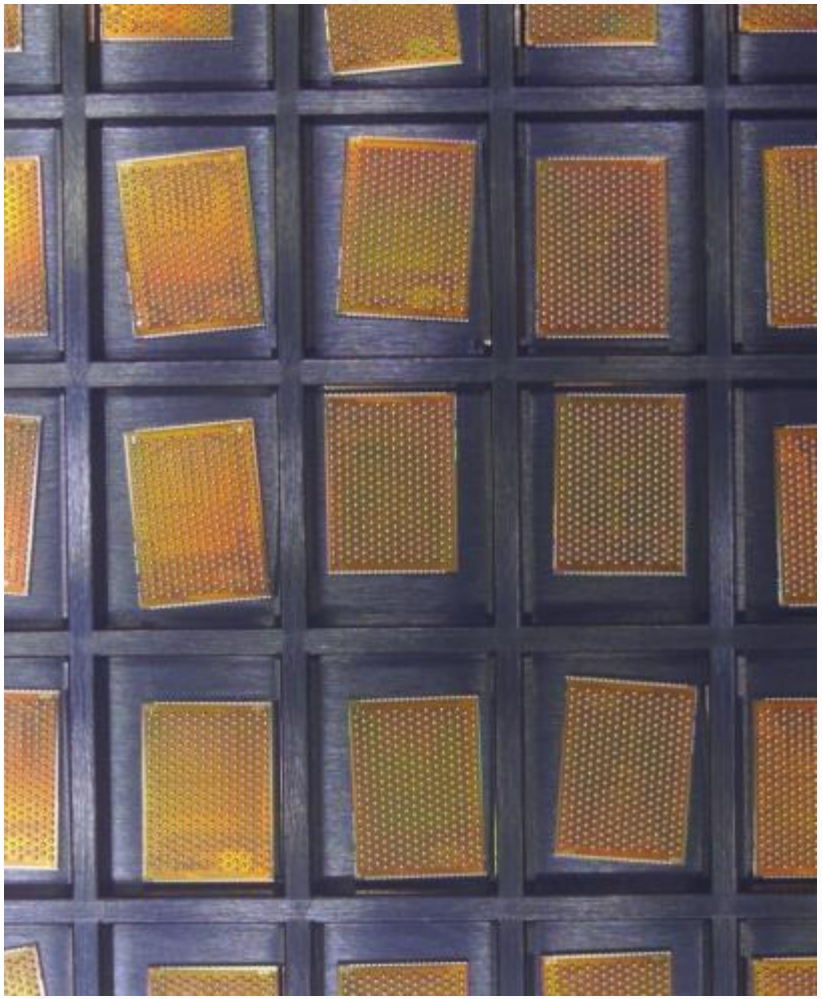
DHPT 1.0

DHPT 1.0, **first production version**

– 12 mm^2 area, C4 bumps (SAC 305)

– Mainly digital with analog IP blocks (PLL, serializer, Gbit link, LVDS…)

- MPW submission in Aug. 2013
- Delivery end of Nov. 2013
- 100 chips received (eq. one wafer)
- Turn-around: 3 months including bumping



Status of Verification

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	IP Block / Task	Status	Comment
Data Processing	Gbit Link Driver	✓	
	PLL / Serializer	(✓)	Works with adjusted VCC / CLK freq.
	Temperature Sensor	✓	
	LVDS IO	✓	
	Interface DHP-DCD	(TBD)	Need new WB adapter (LVDS DCDCLK)
	Interface DHP-Switcher	TBD	
	Bias DAC, Currrent reference	✓	
Data Processing	Command Interface (Manchester encoded)	✓	
	Memory Access (via JTAG)	✓	
	Data Processing: Channel Masking	TBD	
	Double Precision Common Mode Processing	TBD	
	Overflow Handling	**TBD**	

- Functional verification: DHPT 1.0 mounted on PCB with WB adapter ongoing
  - Analog blocks ✓
  - Digital signal processing → ✓, ongoing
  - Interface DCD, Switcher → TBD
  - Serializer needs non standard operation conditions

- Next verification steps
  - Full functional coverage with current PCB test setup
  - Probe station tests → known good die
  - System tests!!! (E-MCM…)

- Planned re-design DHPT 1.1
  - Serializer bug fix
  - Anything else that eventually shows up (Data processing, E-MCM operation …)

Extra

Some maybe useful documents:

Phases of an ASIC Project:
https://dl.dropboxusercontent.com/u/2937630/ASIC/Phases%20of%20an%20ASIC%20Project.pdf

Design Review Checklist:
https://dl.dropboxusercontent.com/u/2937630/ASIC/Design_Review_Checklist.pdf

Our small checklist:

- PADS/ESD
- Powering (Power/Ground separation)
- Bias lines (default currents/voltages/ranges)
- Configuration
- Full chip simulation if needed (extracted)
- Testability (what is testable if failure?)
- IO Drivers/receivers (Interface)
- TID
- How the chip will be tested