DCD B Review:

1. Documentation needed:
2. Description of new registers
3. Schematics (updated of DCD manual)
4. List of known good settings
5. BSDL file for boundary scan test
6. Description of digital test pattern

Proposed Tests:

We need to define the test conditions (optimal parameters, clock frequency (needed is 305 MHz, 320 is a kind of safety margin)

1. Digital test: write in all registers and read back
2. Power test: all currents as expected (@ 305 MHz)
3. JTAG boundary scan ok?
4. Pedestal control (VNSubIn, VNSubOut, 2bit DAC)
5. Functionality of calibration circuit (internal & external)
   1. Tuning of optimal settings……
6. Pedestal spread (rms, peak-to-peak), without sensor
7. Gain and linearity (with internal or external current source?)
8. Dynamic range
9. RMS noise without sensor: @ 305 MHz (and 320 MHz), dependence on parameters (supply voltages, Amplow, Refin, number of active chips (EMCM), temperature)
10. Number of defect channels:
    * 1. Large pedestal offset (criteria)
      2. Excessive noise (> 2 x rms?)
      3. Missing codes / excessive non-linearities
11. Link DCD-DHP: stability @ 305 MHz and 320 MHz (How to measure?)
12. Analogue common mode subtraction (with internal current source)
13. DACs for pedestal correction

Tests should be performed on hybrid 4/5 (only part of the channels testable?) and on EMCM.

Test with matrix: average noise (increase with respect to measurements without matrix, take care of noisy pixels in the matrix).