PXD ASICs Review, JTAG Issues

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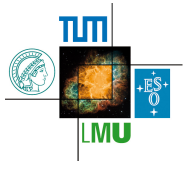

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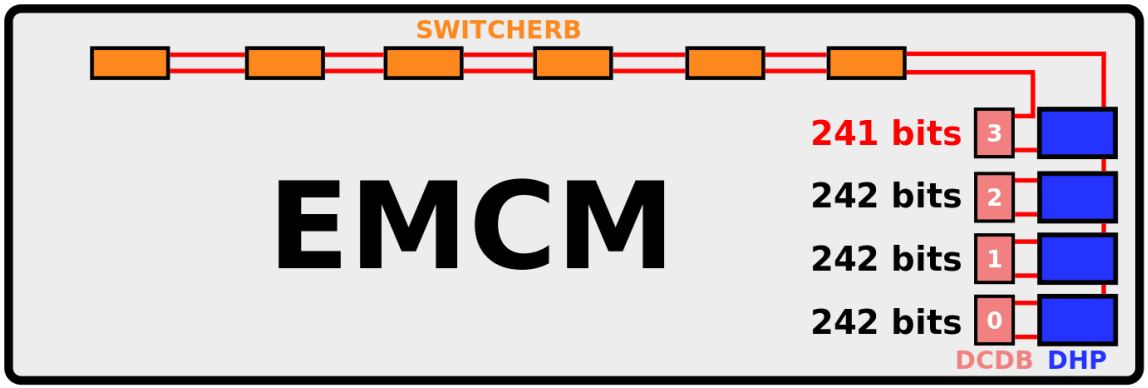
DCD Configuration Problem



- last DCDB requires one bit less during configuration
- same situation on the module with only one DHP-DCD pair
- work around implemented in software to mitigate the problem

Problem Localization

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- not easy to debug because reading back DCD register is not supported
- trick to localize problem:
  - program DHP and DCD simultaneously
  - read back DHP register and analyze its content
  - repeat with the same bitstream on the next pair

- Switch on DCD0: DCD0 ON. Read data: 01020304 ..
- Switch on DCD1: DCD1 ON. Read data: 01020304 ..
- Switch on DCD2: DCD2 ON. Read data: 01020304 ..
- Switch on DCD3: all DCDs OFF. Read data: 01020304 ..
- Switch on DCD3, remove one bit: DCD3 ON. Read data: **02040608** ..

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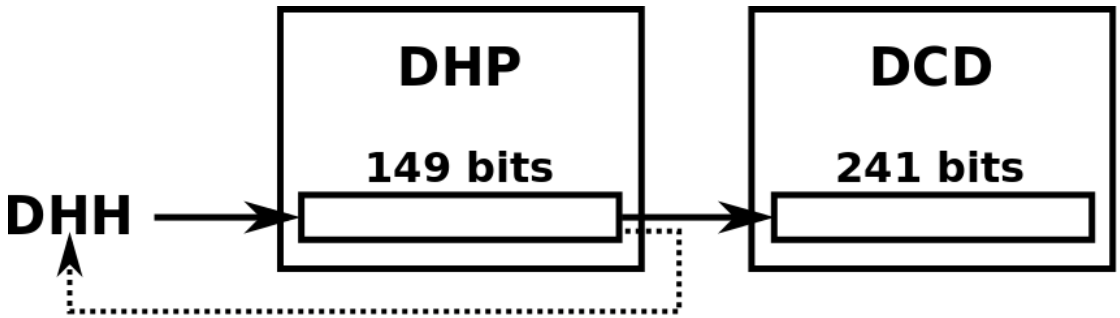

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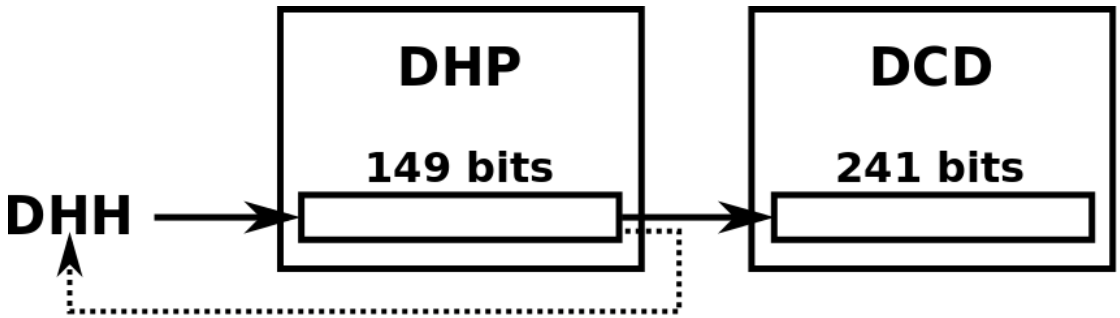

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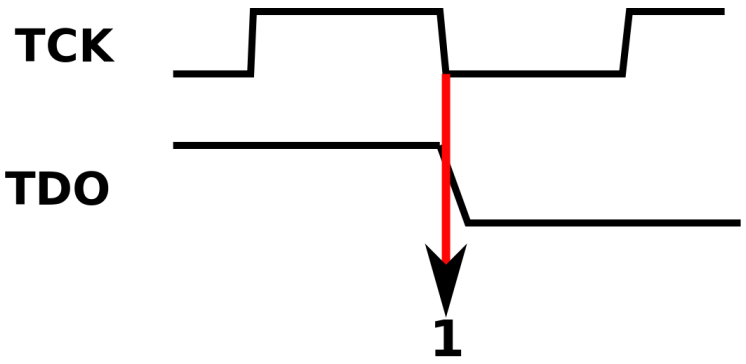
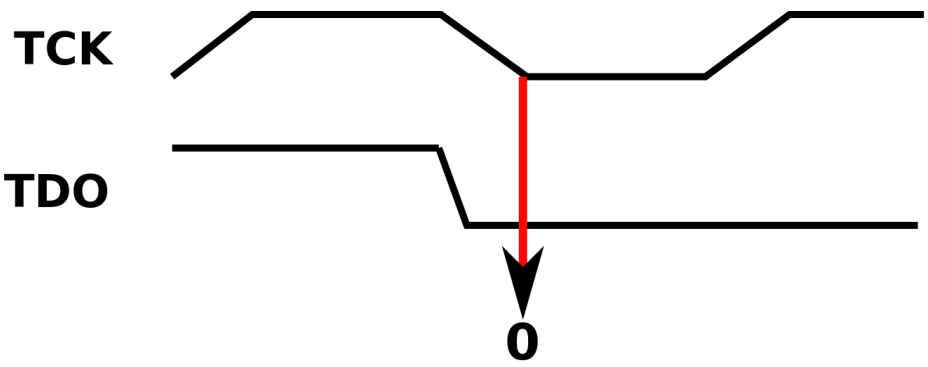
DCD0-2:



- clock and data equally fast
  - previous bit sampled
- requires additional bit for compensation

DCD3:



- long TCK line:
  - large capacitance
  - slow signal transition
- does not require dummy bit

Implications/Solutions

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Implications

- uncertainty in the configuration because of metastability
- we can loose 1/4 of the matrix

Solutions

1. Use DHPT TDO delay to adjust signal timing:
   - has to be tested in hardware
2. Software workaround: remove one bit if configuring DCD which is connected to Switchers
   - very ugly solution: two affected DCD positions depending on the half ladder layout.
   - uncertainty remains
3. Fix DCD JTAG design

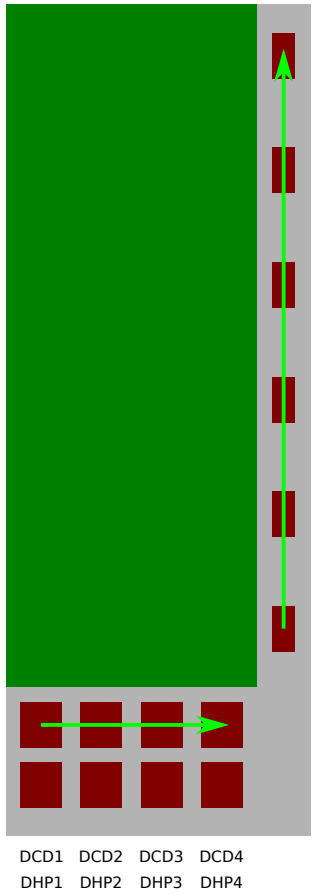
IDCODE Issues

IDCODE Problems in DCD (not critical)

- After resetting JTAG FSM (5xTMS High) bypass register with ’0’ is loaded instead of IDCODE. IDCODE is still present.
- Unique IDCODE for DCD Pipeline?

Back up slides

Outer Backward



Outer Forward