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SI LAB Silizium Labor Bonn

DEPFET Active Pixel Detector

Ideas on Module Slow Control

C. Marinas
University of Bonn

F. Lütticke, L. Germic, C. Koffmane, R. Richter,
I. Peric, M. Ritzert

cmarinas@uni-bonn.de

The DEPFET Ladder

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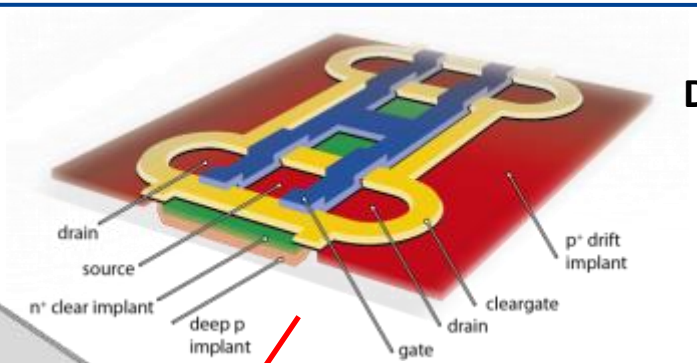
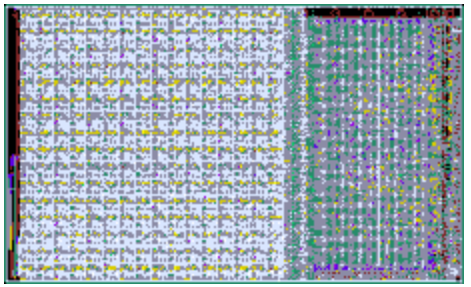
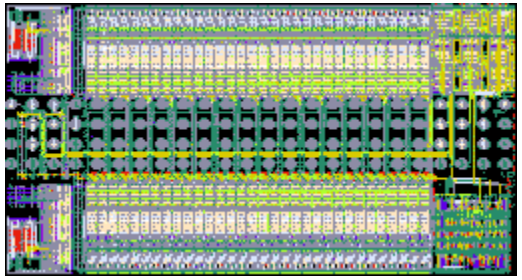


DCDB (Drain Current Digitizer)
Analog frontend



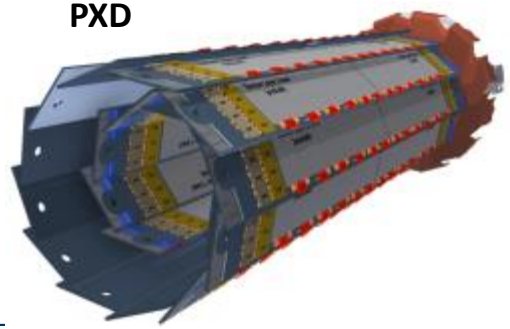
UMC 180 nm
Size 5.0×3.2 mm^2
TIA and ADC
Pedestal compensation
Rad. Hard proved (20 Mrad)

SwitcherB
Row control

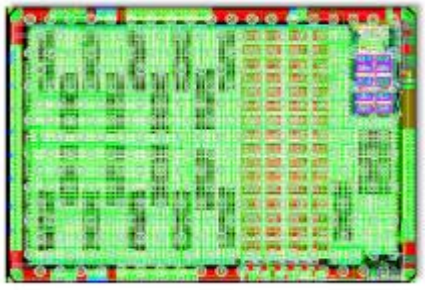


AMS/IBM HVCMOS 180 nm
Size 3.6×1.5 mm^2
Gate and Clear signal
Fast HV ramp for Clear
Rad. Hard proved (36 Mrad)

PXD

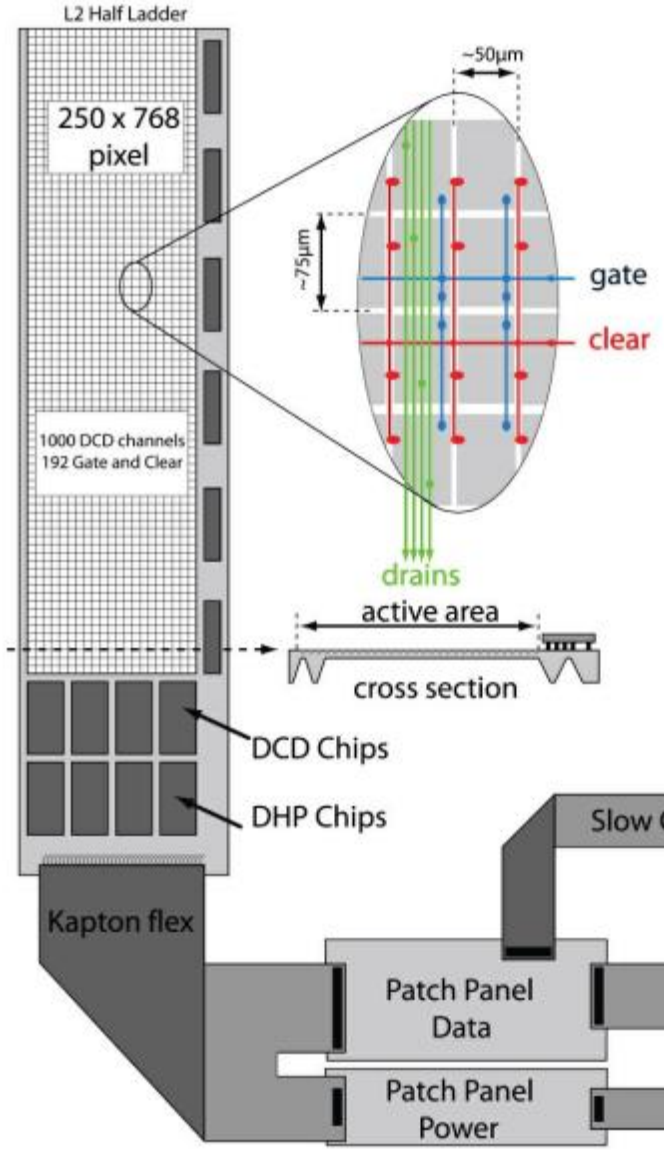


DHP (Data Handling Processor)
First data compression

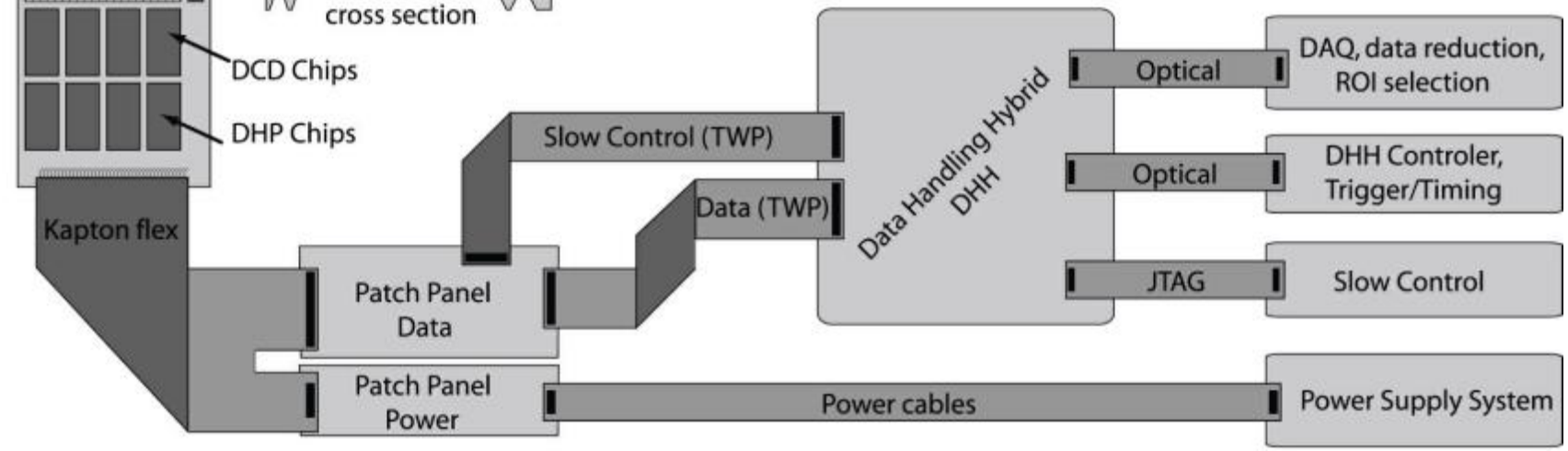


TSMC 65 nm
Size 4.0×3.2 mm^2
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation
Rad. Hard proved (100 Mrad)

Off-module Data Flow



- **DHH** (Data Handling Hybrid)
  - Electrical - optical interface
  - Slow control master (JTAG)
  - Clustering
- **ONSEN**
  - Data buffer
  - Reduction via ROI selection (DATCON, HLT)



PXD6 Module

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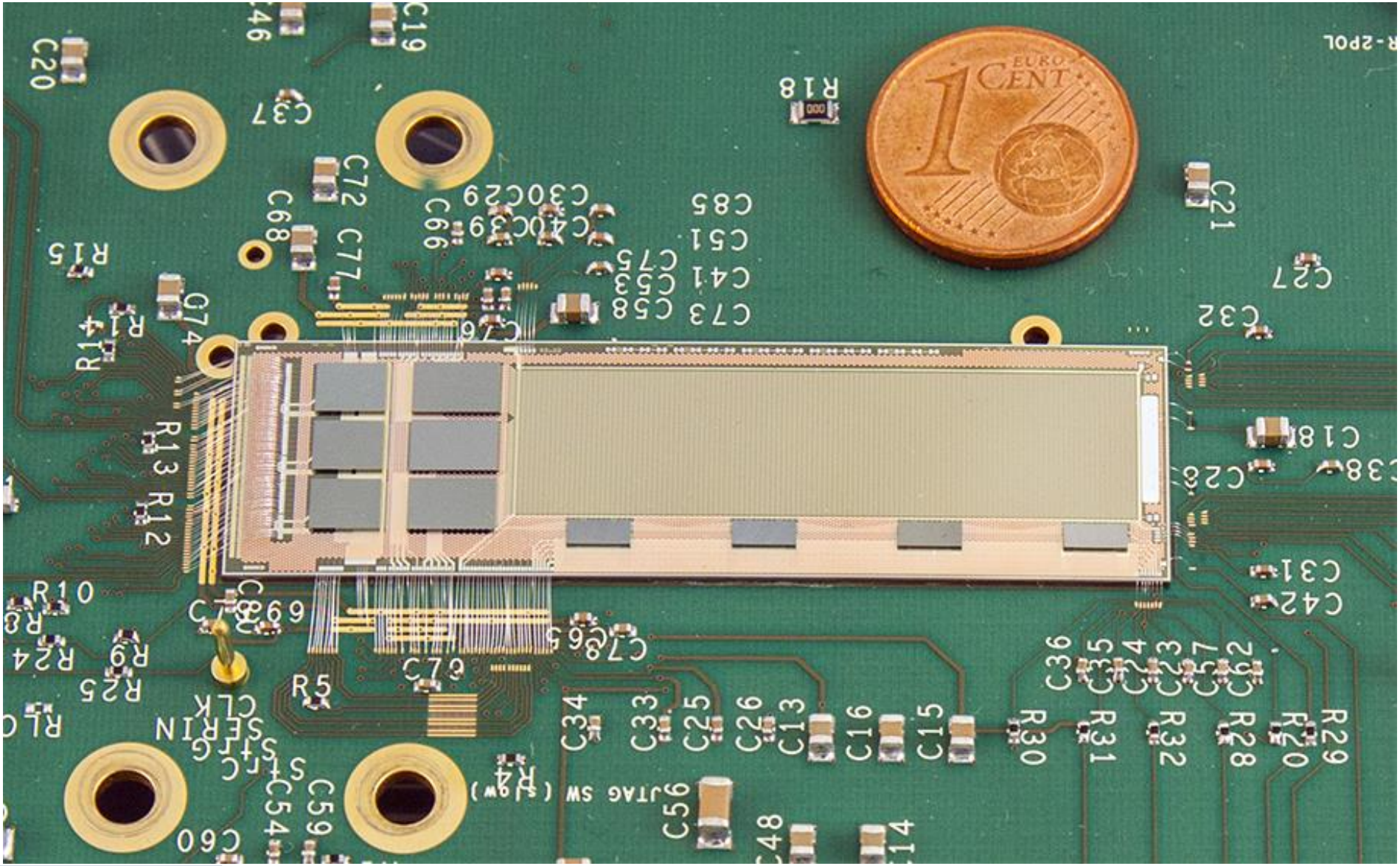
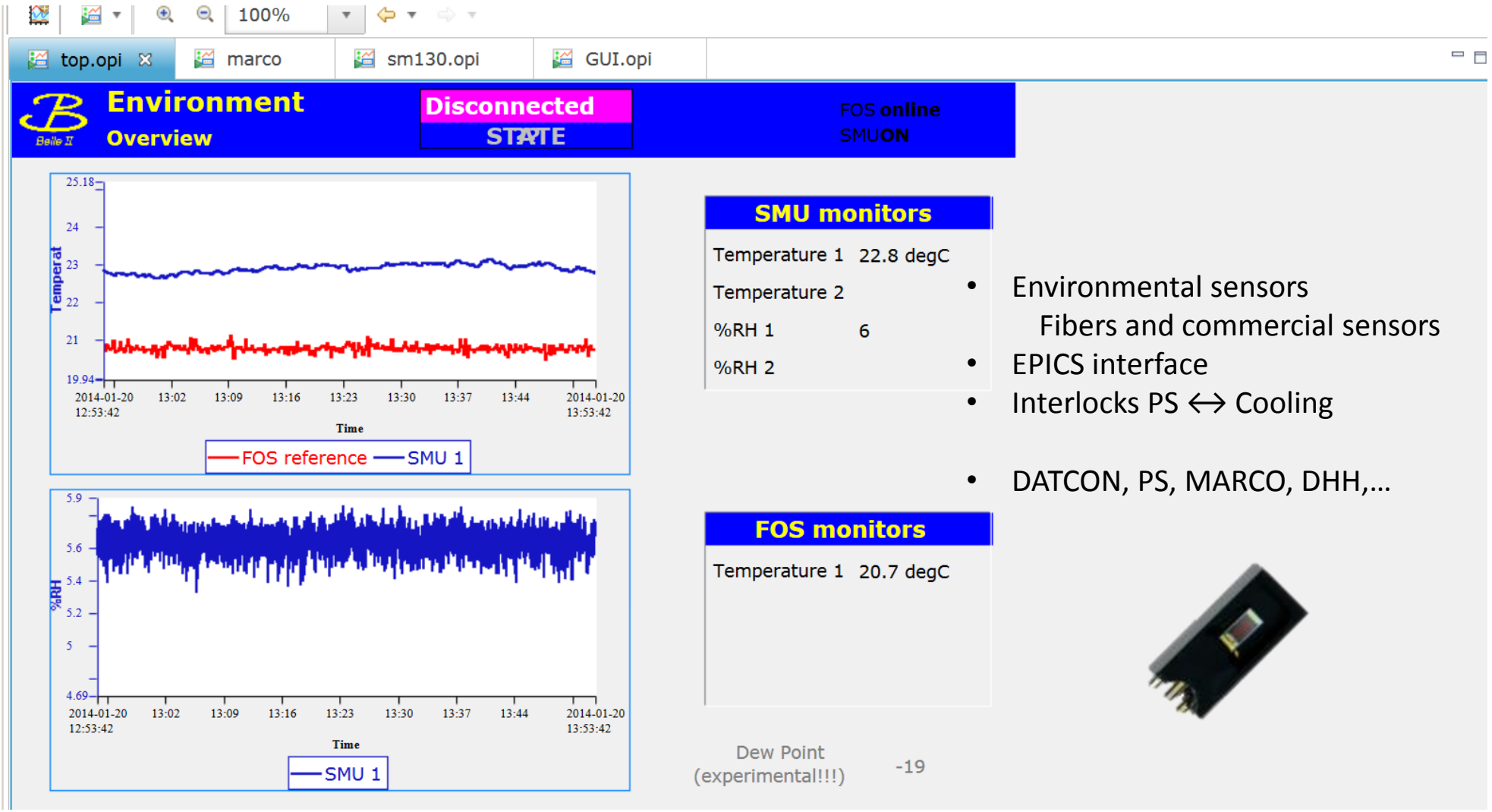


Test Beam Slow Control Exercise



- Environmental sensors
  Fibers and commercial sensors
- EPICS interface
- Interlocks PS ↔ Cooling
- DATCON, PS, MARCO, DHH,…

CO_2 Cooling Plant

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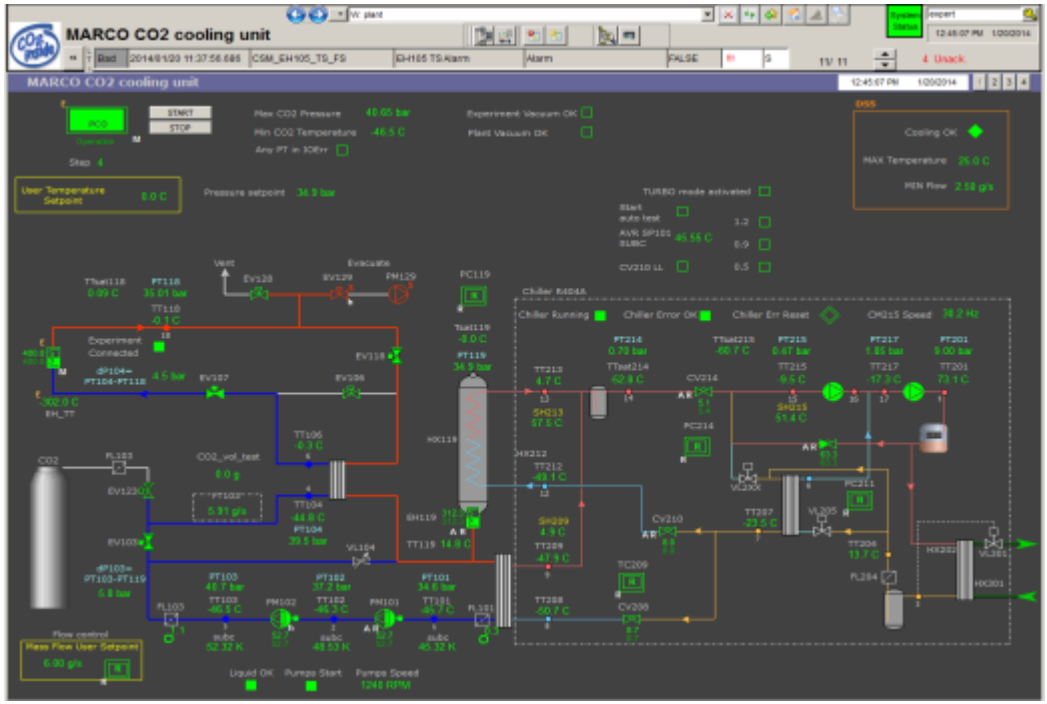

- Connected (only) to the SVD
- Additional close loops with heaters for tuning

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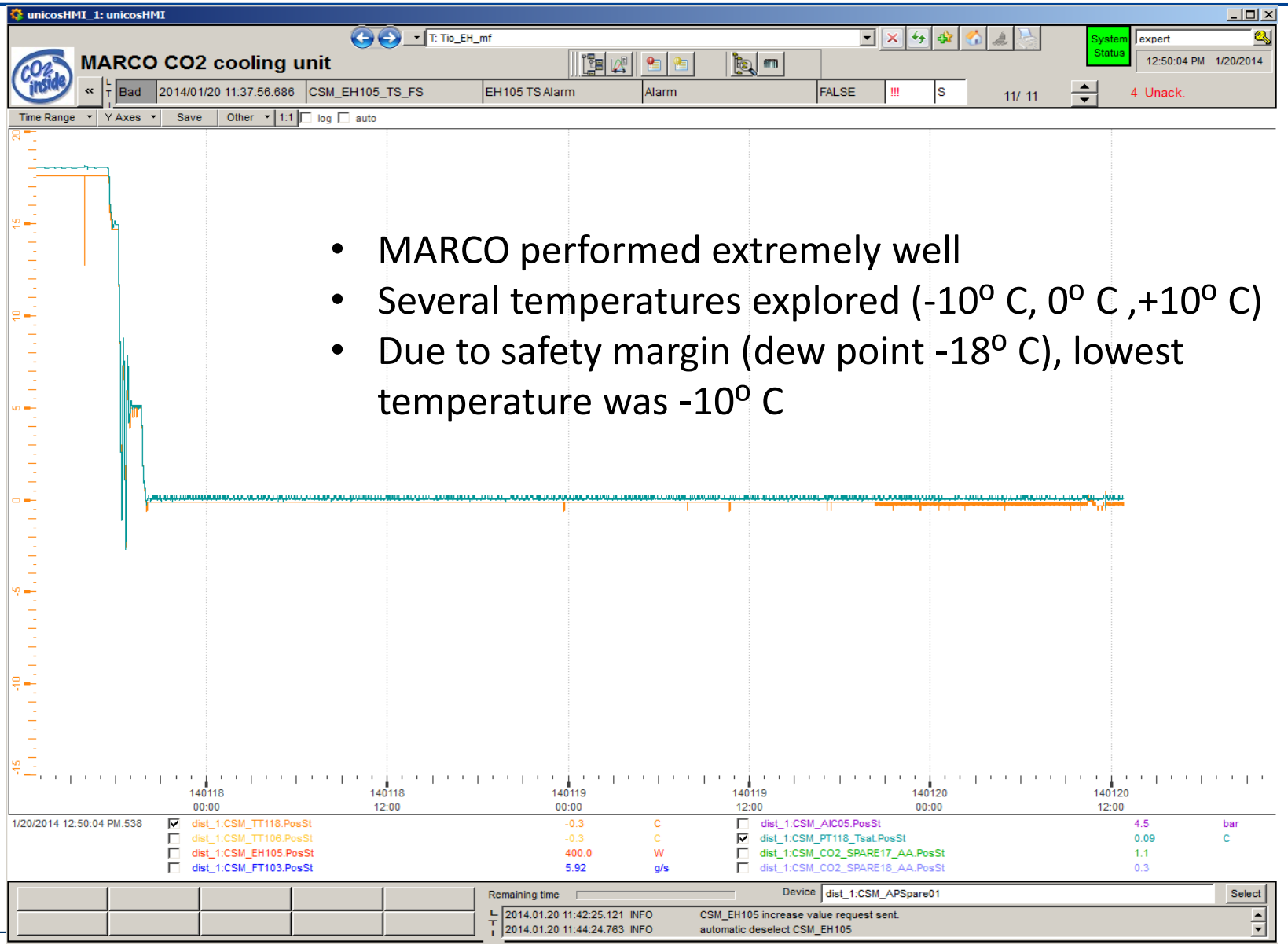
Temperature Stability



- MARCO performed extremely well
- Several temperatures explored (-10^{o} C, 0^{o} C ,+10^{o} C)
- Due to safety margin (dew point -18^{o} C), lowest temperature was -10^{o} C

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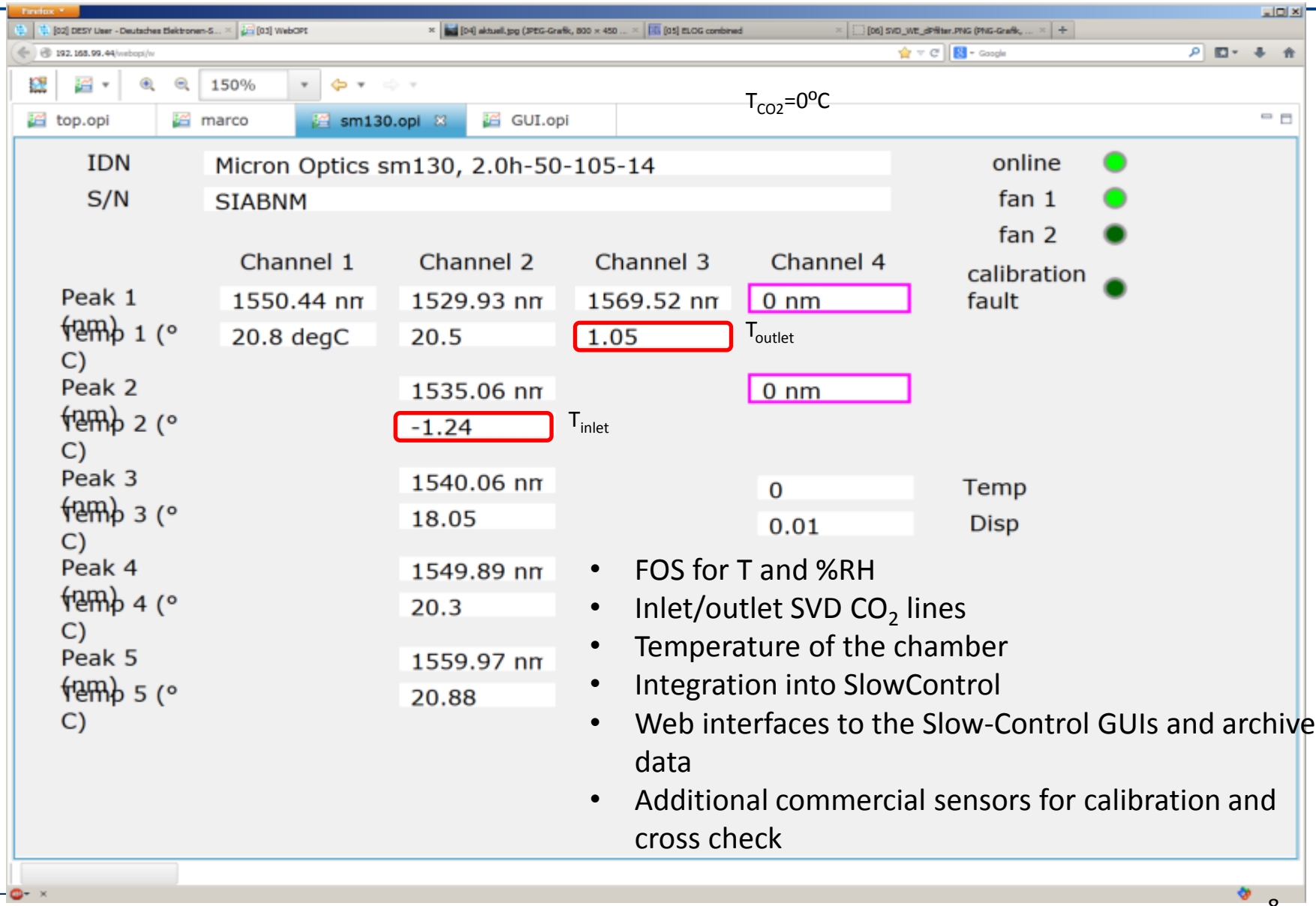
Environmental Monitors



- FOS for T and %RH
- Inlet/outlet SVD CO_2 lines
- Temperature of the chamber
- Integration into SlowControl
- Web interfaces to the Slow-Control GUIs and archived data
- Additional commercial sensors for calibration and cross check

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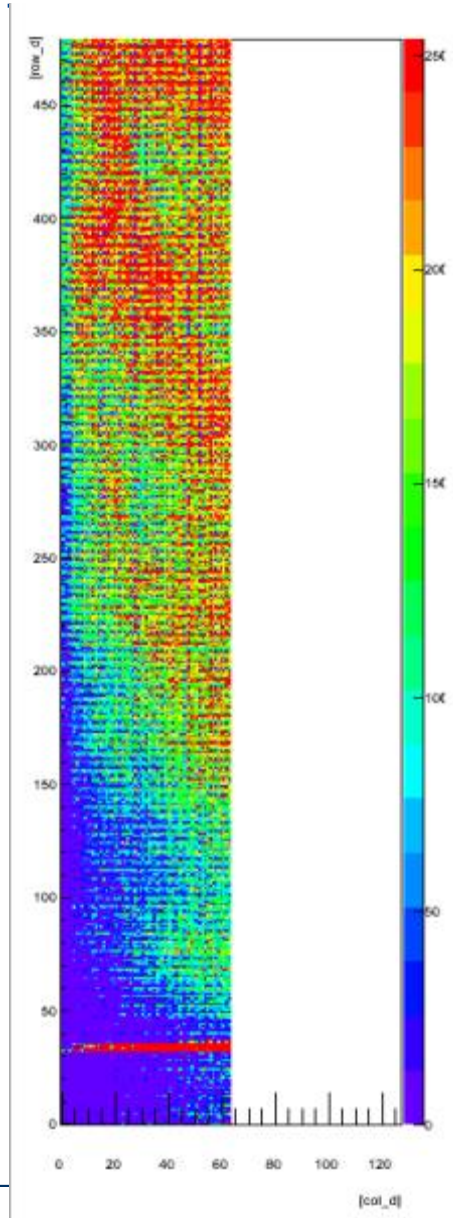
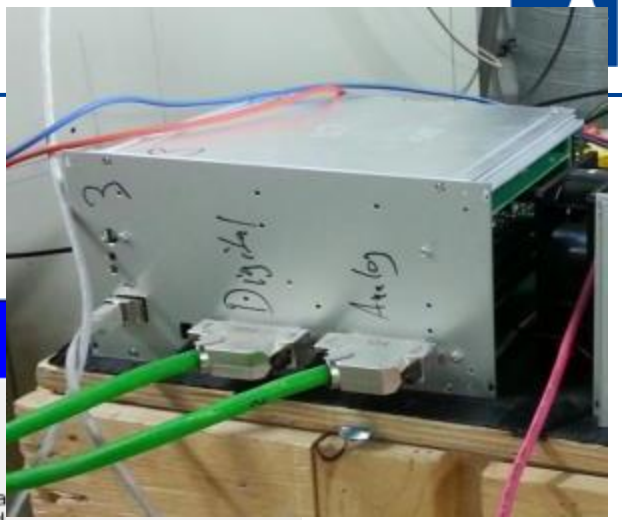
PXD Power Supply



Powersupply — P03 Overview — ERROR

ENABLED | CONNECTED | INITIAL | OVP | THERMAL | UPS

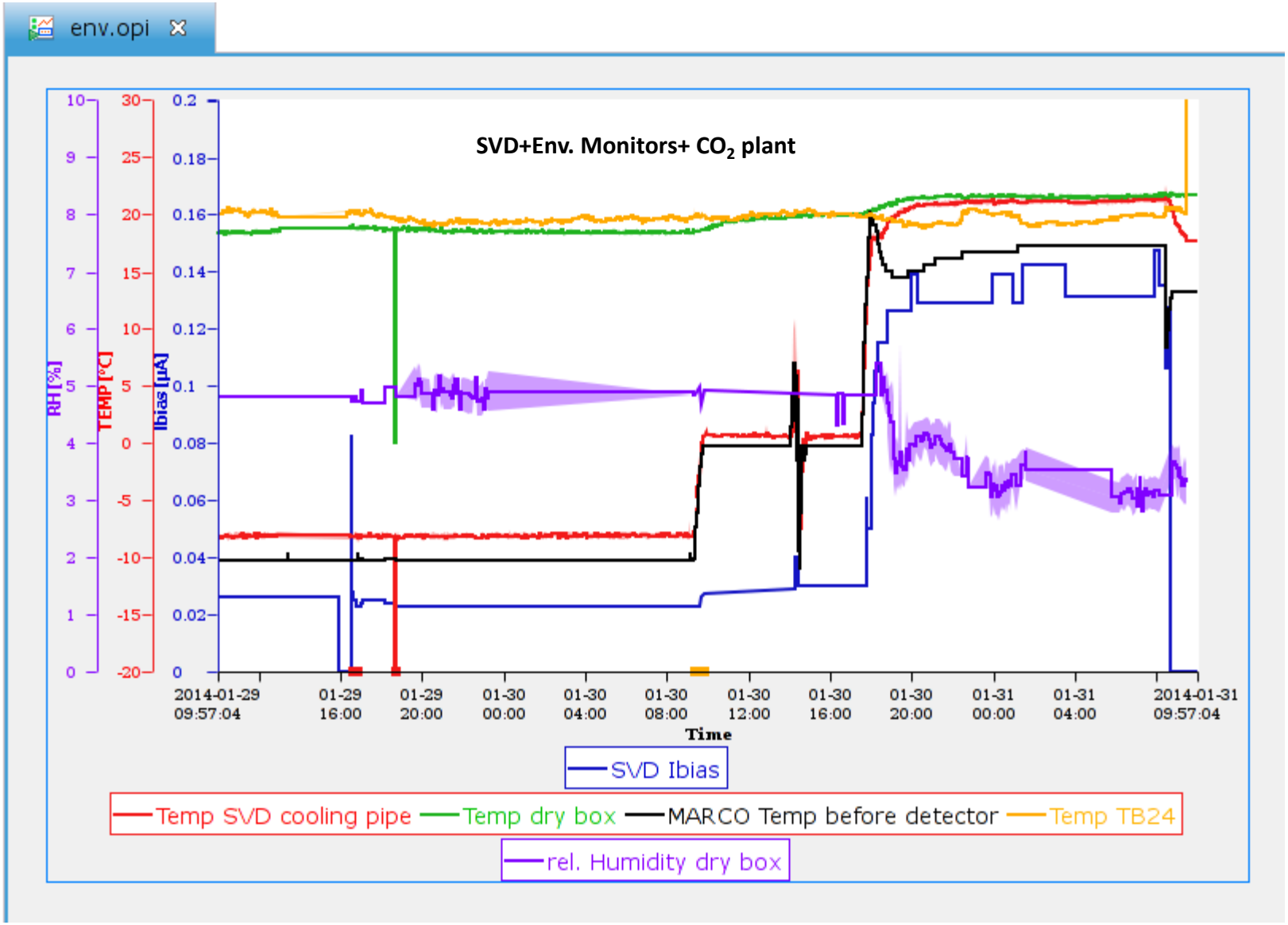
	Set Current	Set Voltage	Regulator Status	Voltage at Regulator	Volta Load	
NOT_USED_1	0 mA	0 mV	1	0 mV	0 mV	0 mA
NOT_USED_2	0 mA	0 mV	1	0 mV	0 mV	0 mA
NOT_USED_3	0 mA	0 mV	1	0 mV	0 mV	0 mA
NOT_USED_4	0 mA	0 mV	1	0 mV	0 mV	0 mA
NOT_USED_7	0 mA	0 mV	0	3 mV	16 mV	1 mA
NOT_USED_8	0 mA	0 mV	0	9 mV	1 mV	6 mA
buffer	20 mA	2200 mV	1	2215 mV	2206 mV	8 mA
bulk	10 mA	17000 mV	1	17027 mV	16998 mV	0 mA
ccg	10 mA	5000 mV	1	5234 mV	5009 mV	0 mA
clear-off	20 mA	10000 mV	1	10225 mV	9990 mV	-10 mA
clear-on	50 mA	19000 mV	1	19304 mV	19029 mV	12 mA
dcd-amplow	400 mA	350 mV	1	414 mV	348 mV	-322 mA
dcd-avdd	900 mA	1900 mV	1	2768 mV	1907 mV	874 mA
dcd-dvdd	600 mA	1800 mV	1	2516 mV	1803 mV	509 mA
dcd-refin	100 mA	1050 mV	1	1447 mV	1052 mV	72 mA
dhp-core	200 mA	1200 mV	1	1622 mV	1196 mV	92 mA
dhp-io	150 mA	1800 mV	1	2199 mV	1795 mV	57 mA
drift	20 mA	4000 mV	1	4003 mV	4029 mV	0 mA
gate-off	20 mA	10000 mV	0	9003 mV	9003 mV	13 mA
gate-on	20 mA	2550 mV	1	2782 mV	2552 mV	-8 mA
hv	10 mA	-12000 mV	1	-12046 mV	-54 mV	0 mA
polycover	20 mA	4900 mV	1	4902 mV	4919 mV	-2 mA
source	70 mA	7000 mV	1	7361 mV	7000 mV	40 mA
sw-dvdd	100 mA	1800 mV	1	2042 mV	1804 mV	12 mA



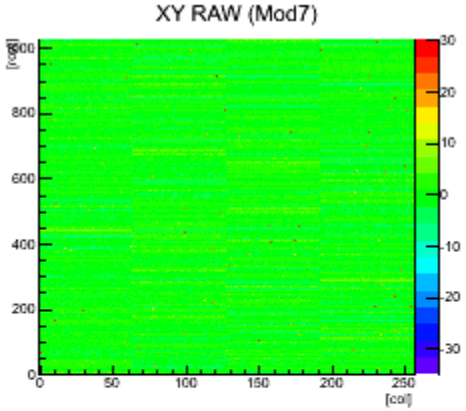
- EPICS interface
- Interlock to CO_2 cooling plant

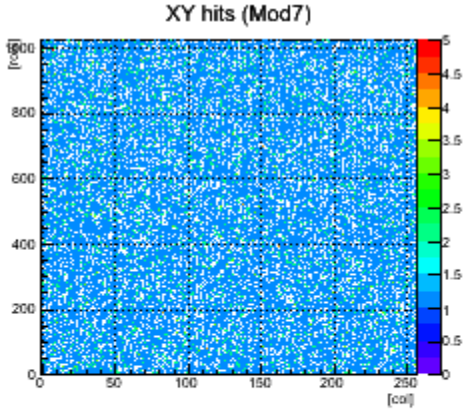
cmarinas@uni-bonn.de

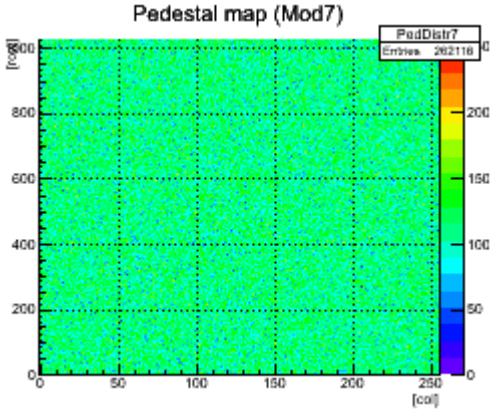
Test Beam Slow Control Exercise

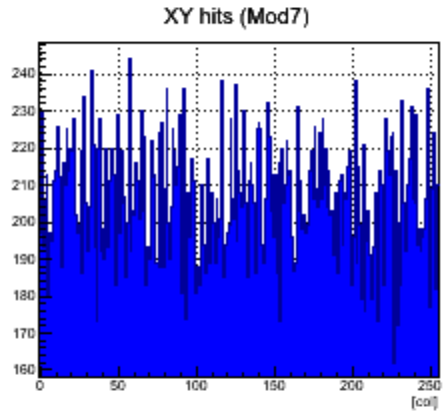


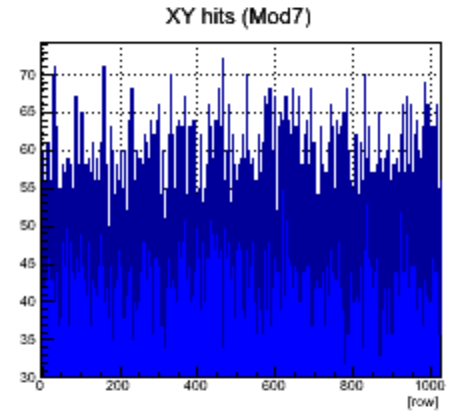
Data Quality Monitoring - BonnDAQ

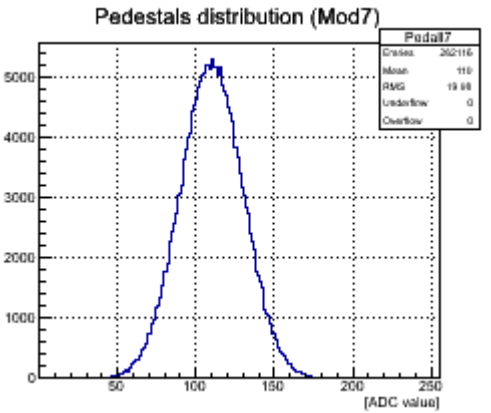


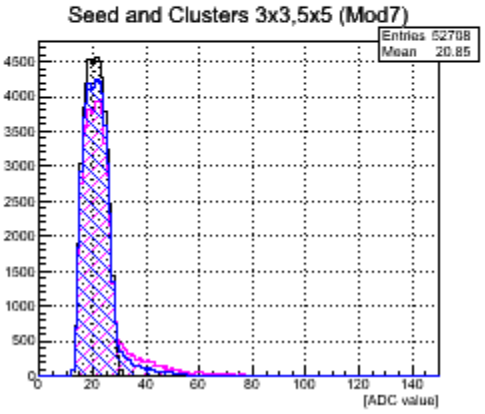


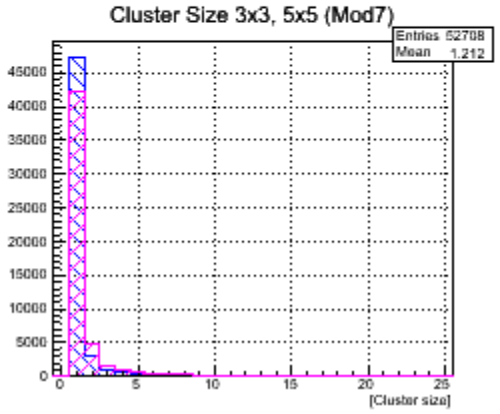


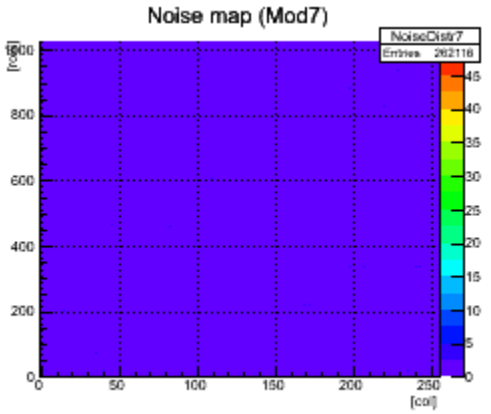




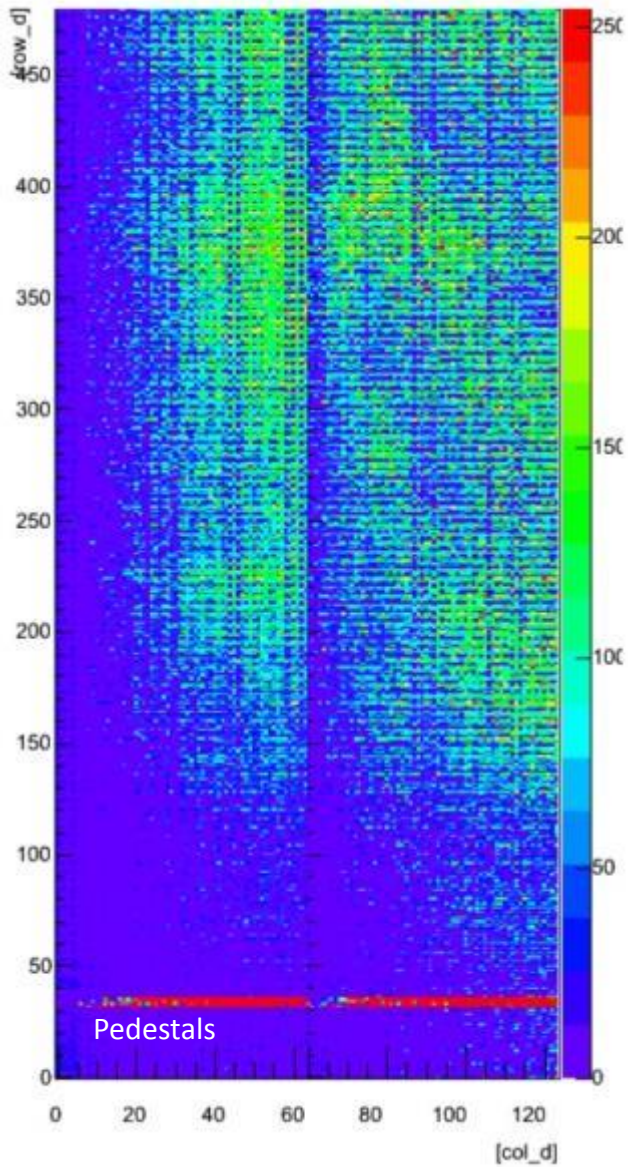


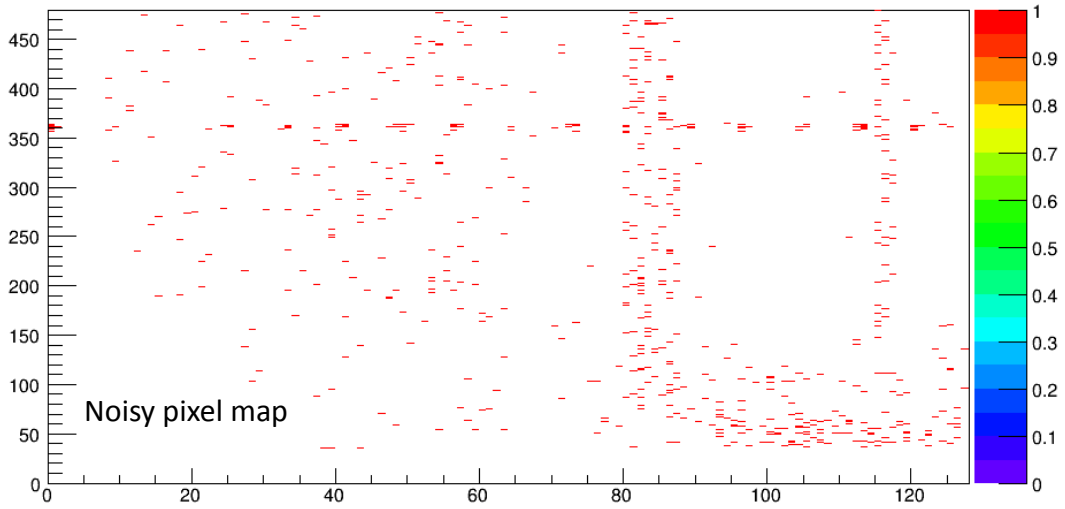




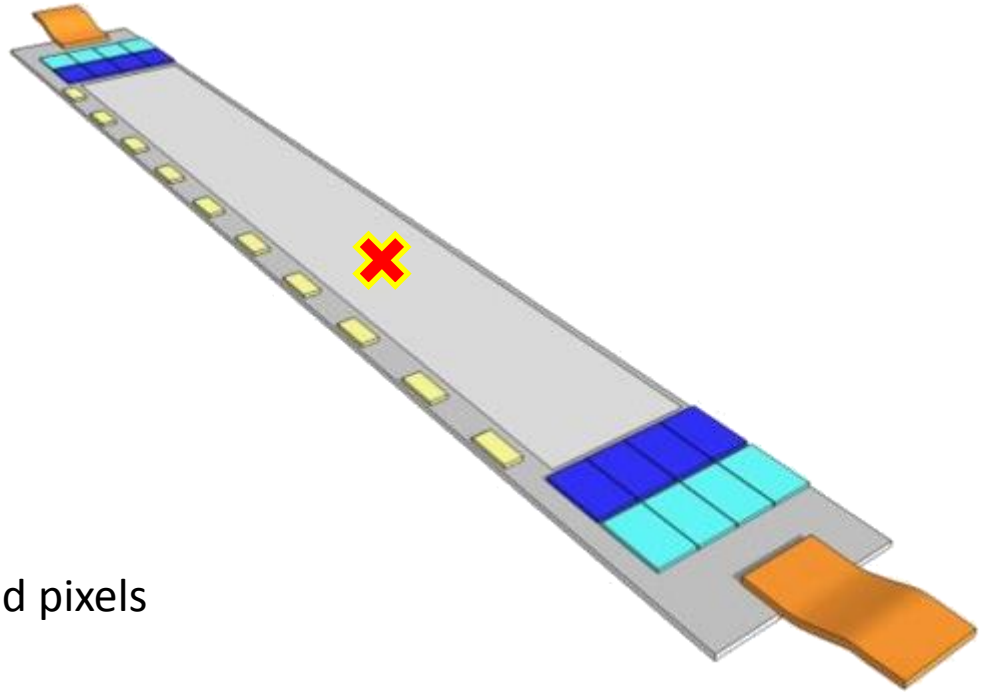


Data Quality Monitoring - BonnDAQ





DEPFET



DEPFET Sensor

Online Monitor / Data Quality Monitoring

- Hit maps for each module.
- Pedestal distribution and noise maps. Masked pixels

Irradiation: Voltage shift threshold compensation (3 areas).

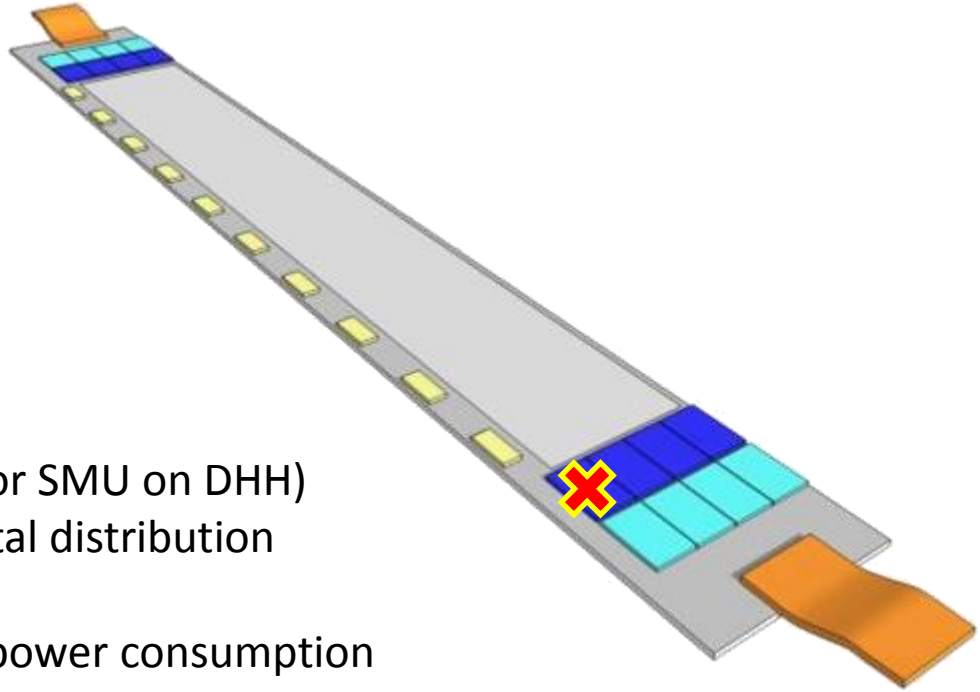
- Through the pedestals? Through the Source current?

Time series of quantities: Temperature, humidity, voltages and currents.

GUI for shifter with basic information (full access for experts).

Which pedestal distribution goes with which run?

DCD



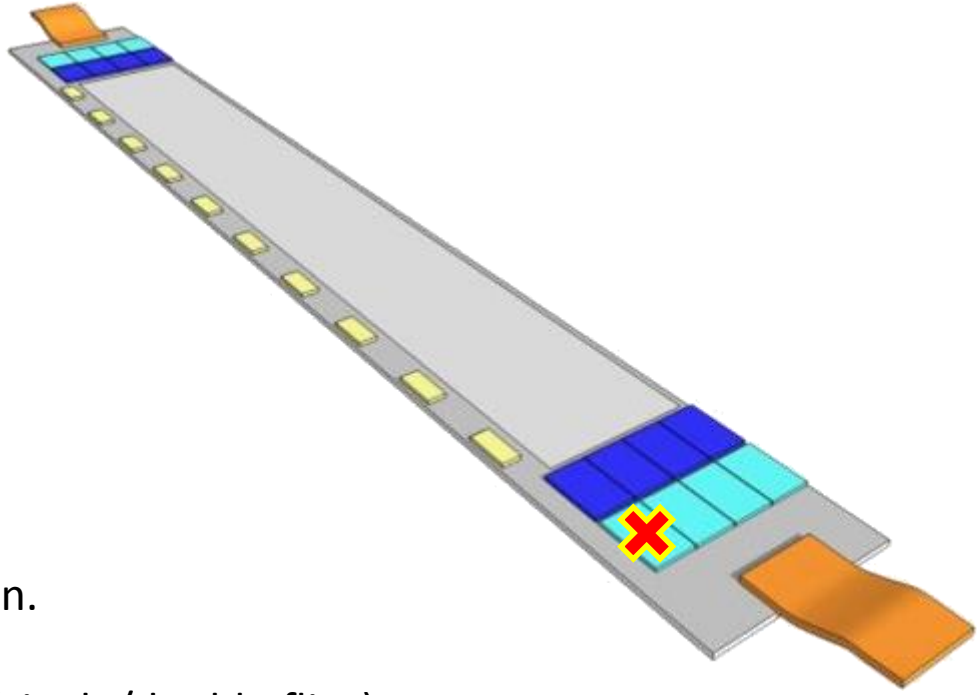
DCD

DCD Calibration curves (Internal current sources or SMU on DHH)
INL, DNL, Gain, noise, dynamic range, pedestal distribution

Time series of quantities: Voltages and currents, power consumption

Initialization files and (offset) DAC values
To be stored together with the run information

DHP



DHP

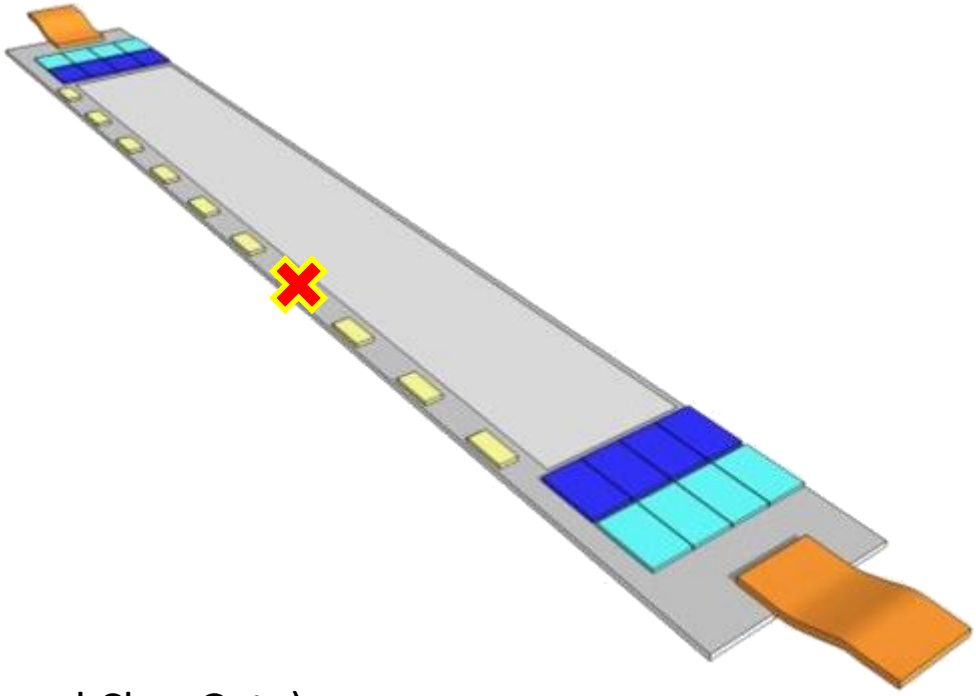
Store DACs and pedestal distribution

Raw frame data processing for pedestal calculation.

Temperature. Switcher sequence. Error counters (single/double flips)

→ Dedicated talk by Leo Germic

Switchers



Switchers

Storage configuration (readback?)

Sampling mode (single sampling or gated mode)

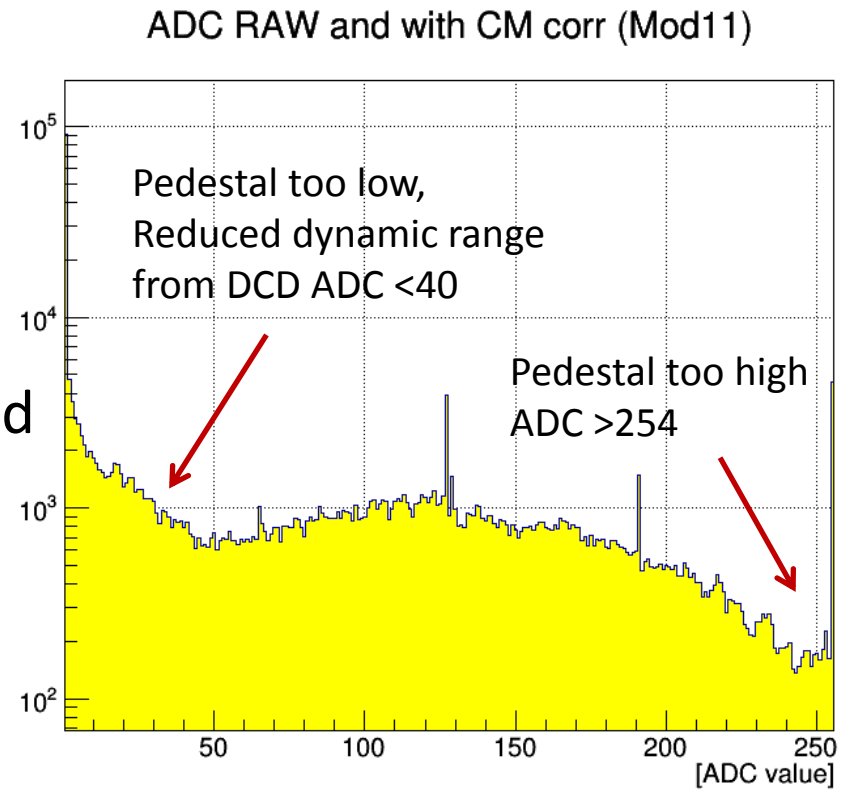
6 Switchers in groups of 2 → Supply voltage (Gate and ClearGate)

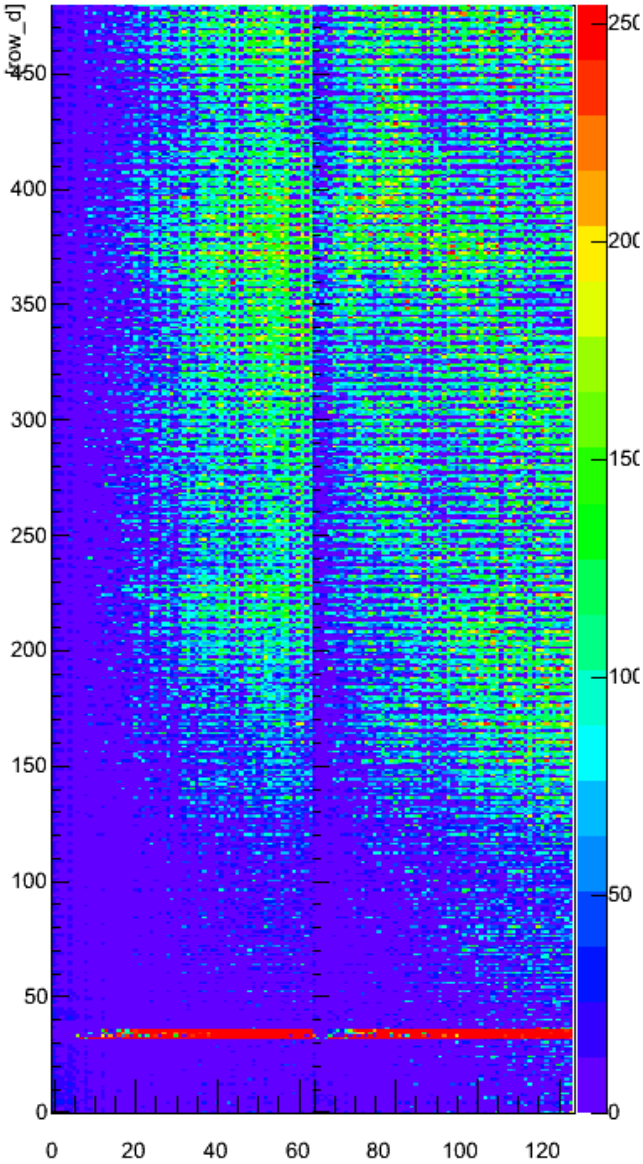
Supply voltage (Clear)

Hybrid 6 Optimization

- **Pedestal distribution of Hybrid 6**
  - Non irradiated
  - Wider distribution than dynamic range of ADC
  - Not all pixel “work” at the same time
  - Known issues from wafer tests + glueing

DCD DACs needed

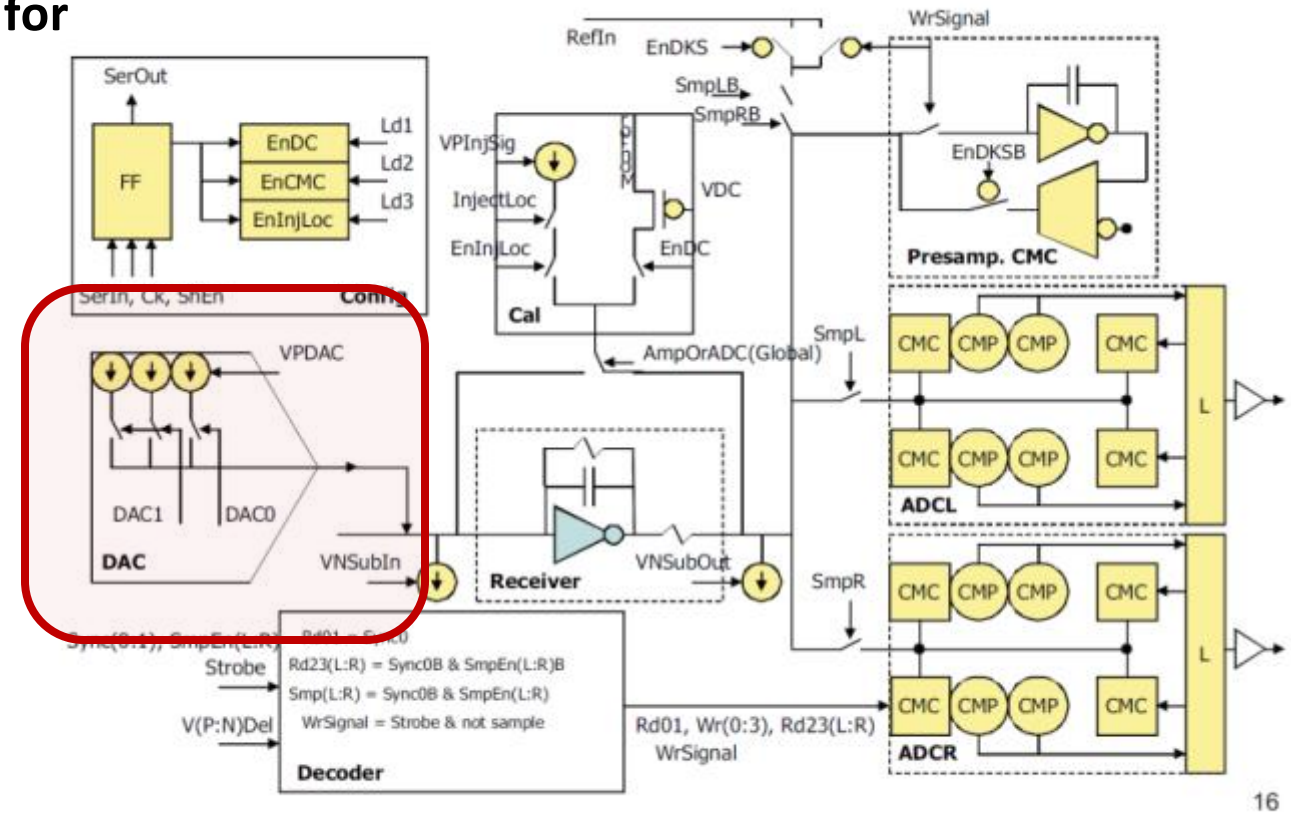




Dynamic DAC Compensation

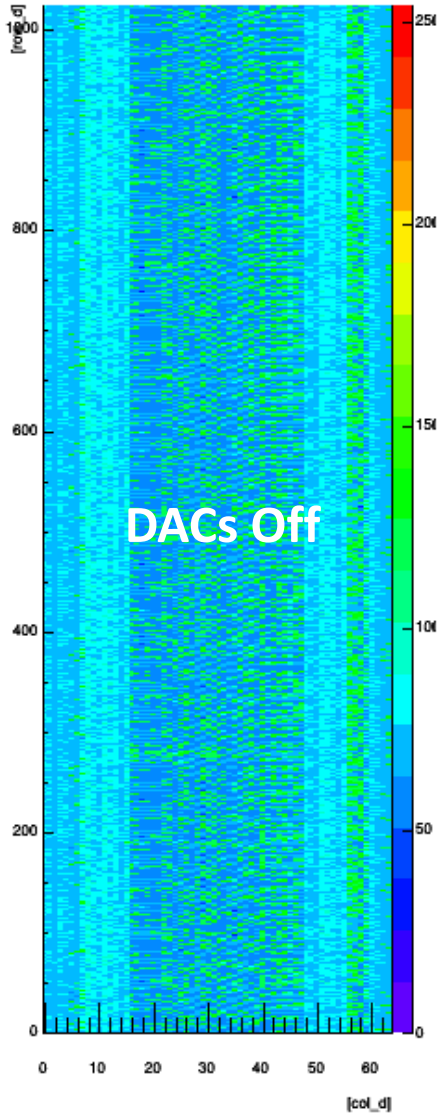
- **Idea: Fold pixels with too low value back into dynamic range**
- **Realized by three switchable current sources. Size of LSB is set by DAC value**

- **Final Task: find best value for**
  - 30k Offset DACs
  - Global DAC
  - Subtraction DAC
  - ~10^{18424} settings
- **First:**
  - Basic function tests
  - Find workaround for DHP Issues

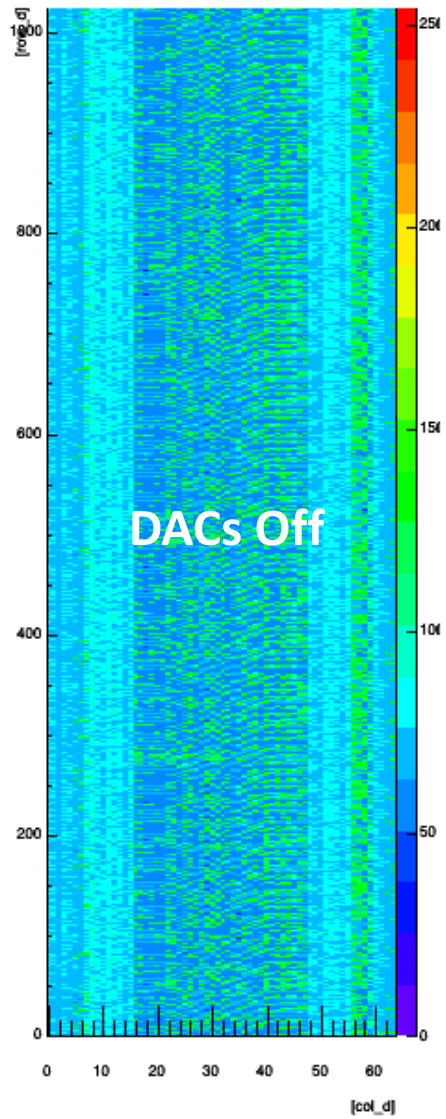


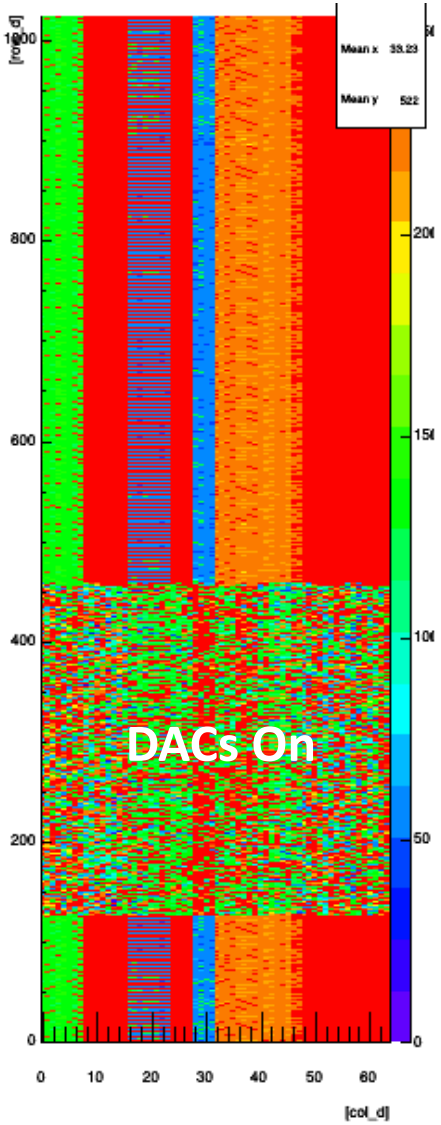
16

DAC Output: DACs off

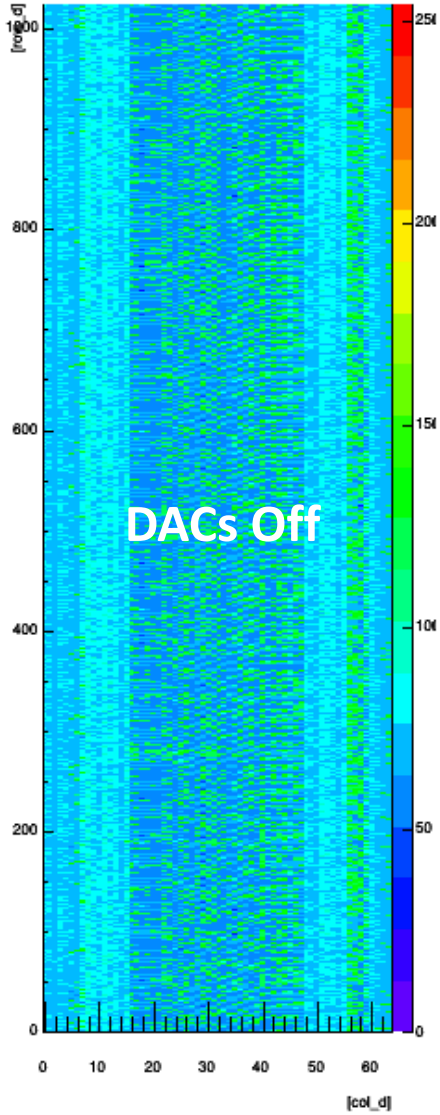


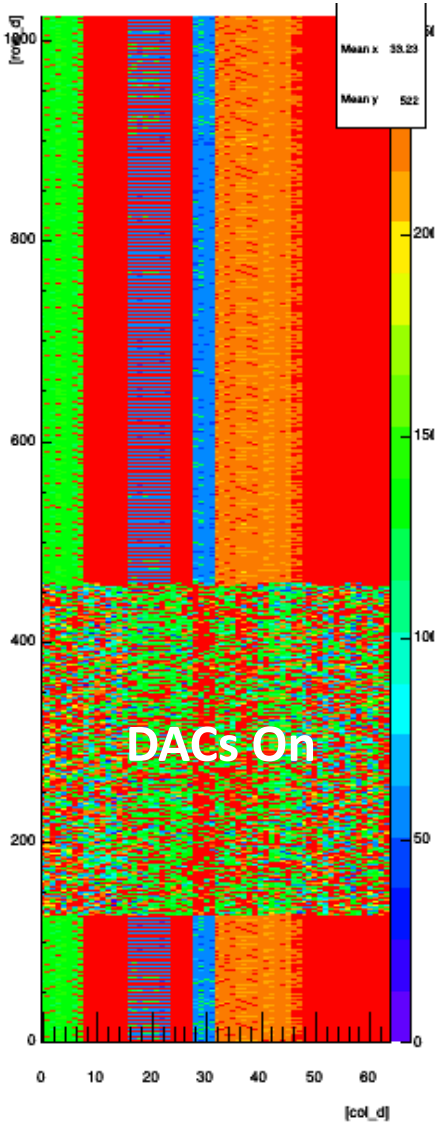
DAC Output: Normal acquisition

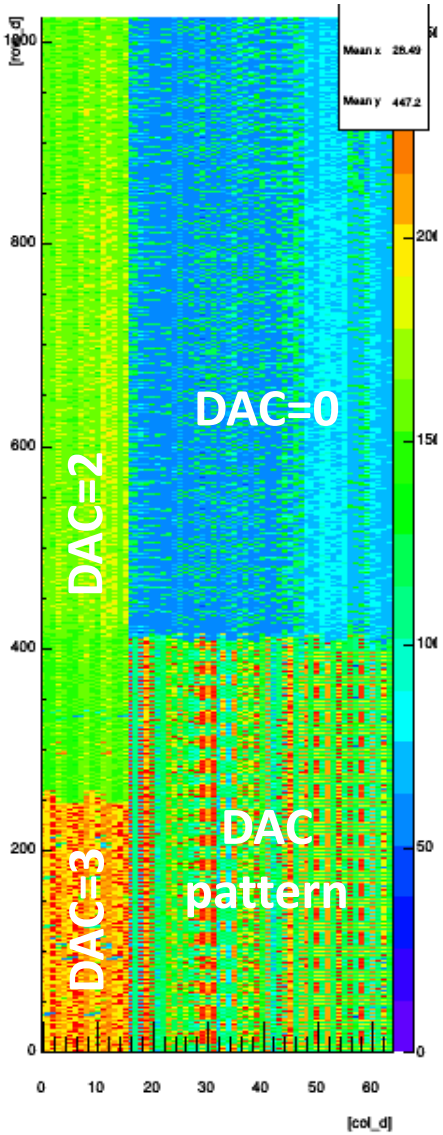




DAC Output: Programmed Memory



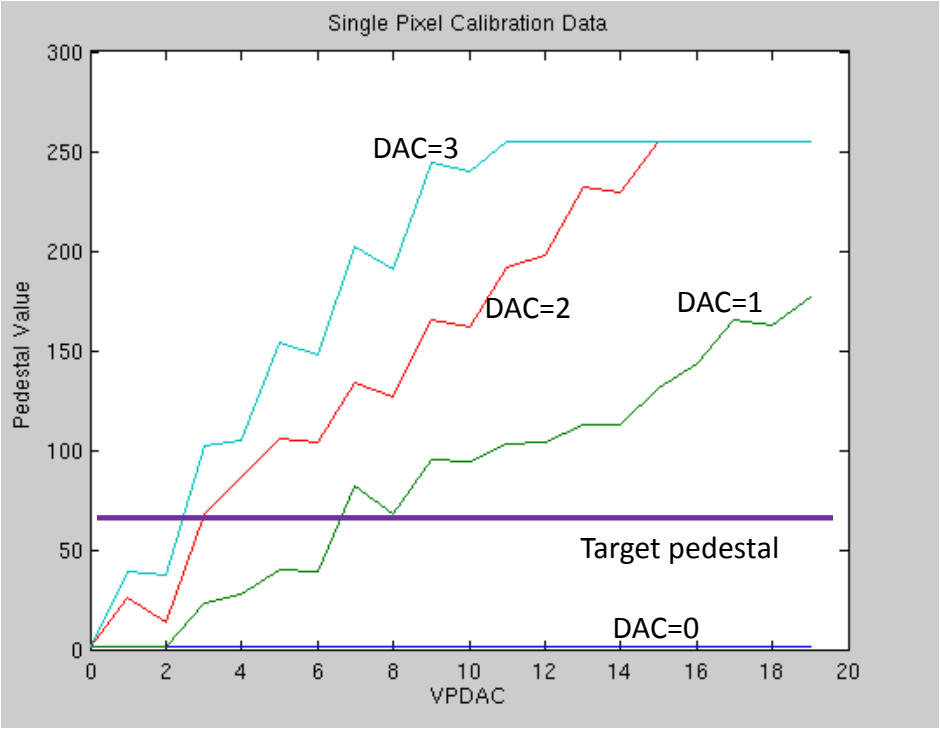




Programmed pattern

Optimize DAC Settings

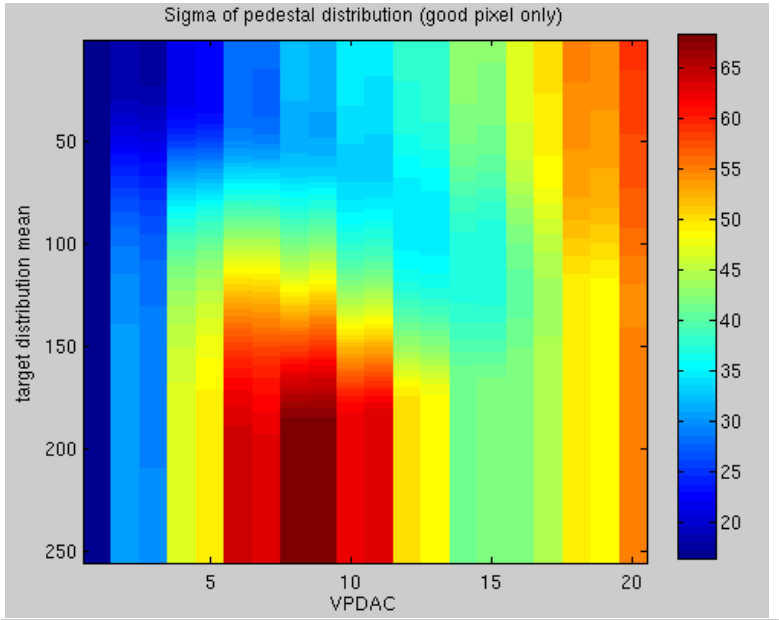
- **Load constant DAC values into memory**
  - Change VPDAC value
- **For each VPDAC value:**
  - Optimize DAC Values to be as close as possible to a certain pedestal value
  - Alternative: try to get pixel to be below certain high threshold while enforce to have them in dynamic range
- **Find best solution in VPDAC - target pedestal space**
  - Ignore bad Pixel!
- **Possible 2nd step for fine tuning**

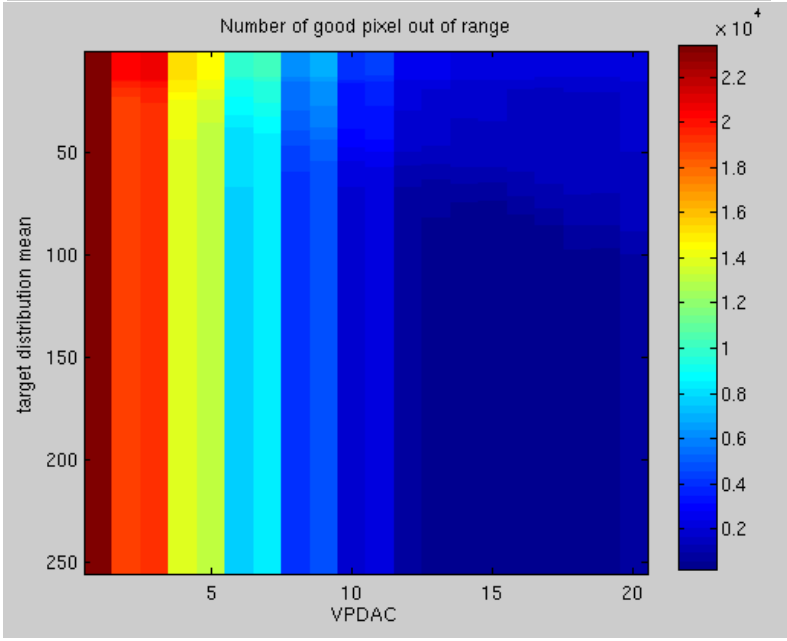


Quality Criteria

- **Criteria:**
  - Distribution width or sigma
    - Optimization can go wrong. All pixel at max or min value is a nice small distribution. -> additional logic needed.
  - Number of Pixel out of dynamic range
    - Not good for final optimization. Very different settings yield the same quality.

- **Convolution of multiple criteria**
  - Normalized sigma + normalized bad pixel count
  - Sigma/# good pixel

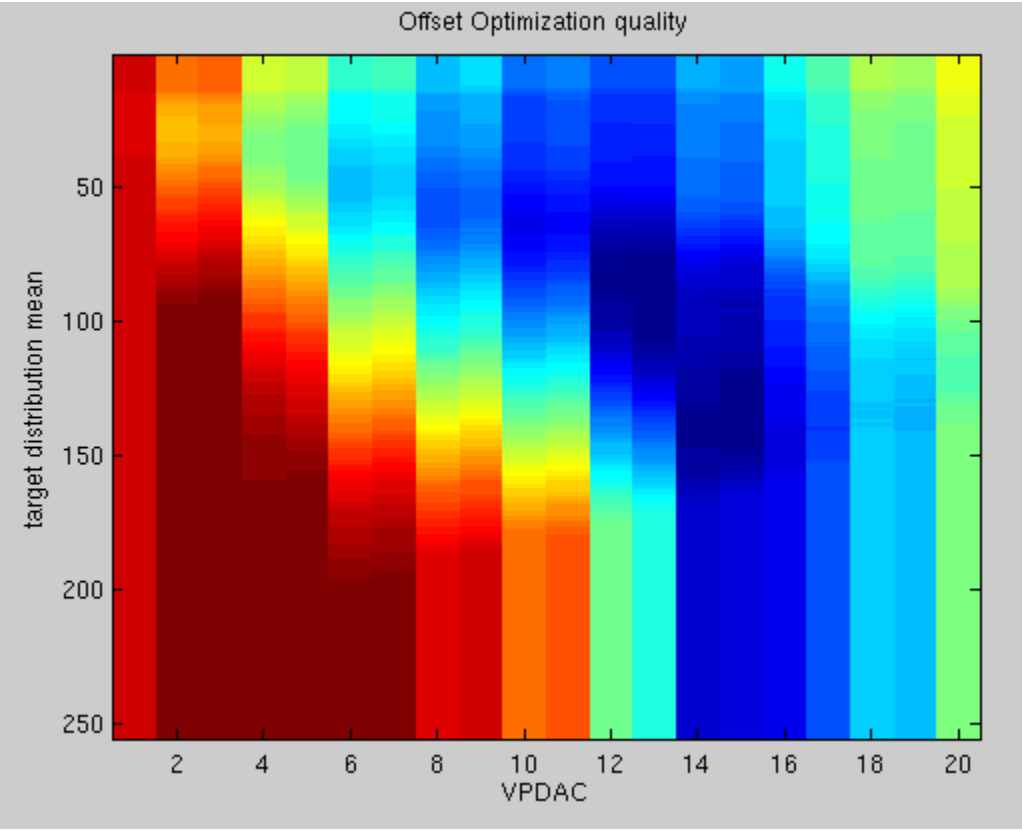


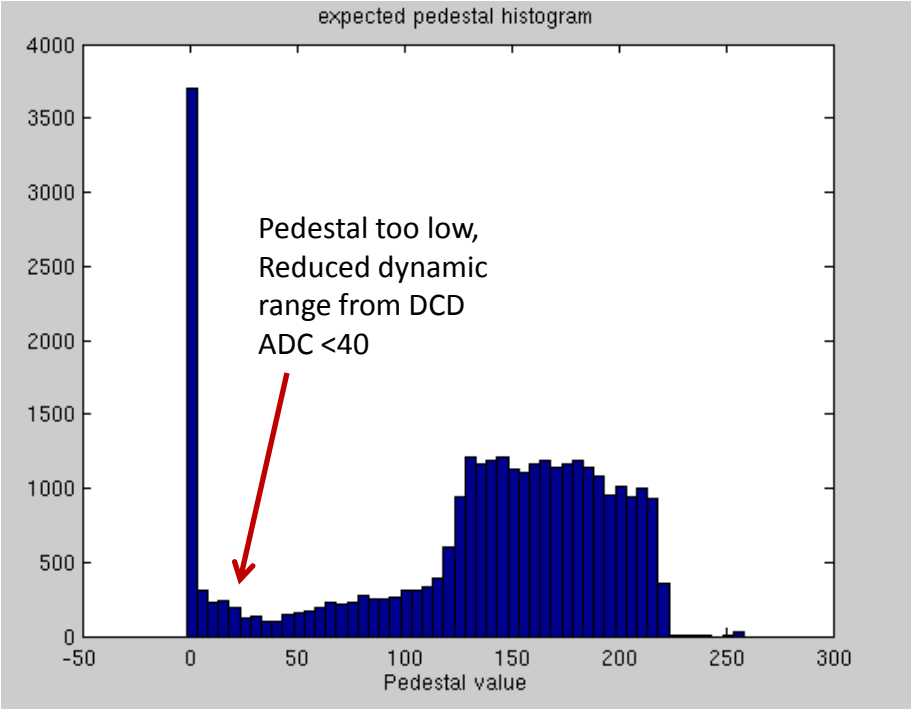


cmarinas@uni-bonn.de

Results

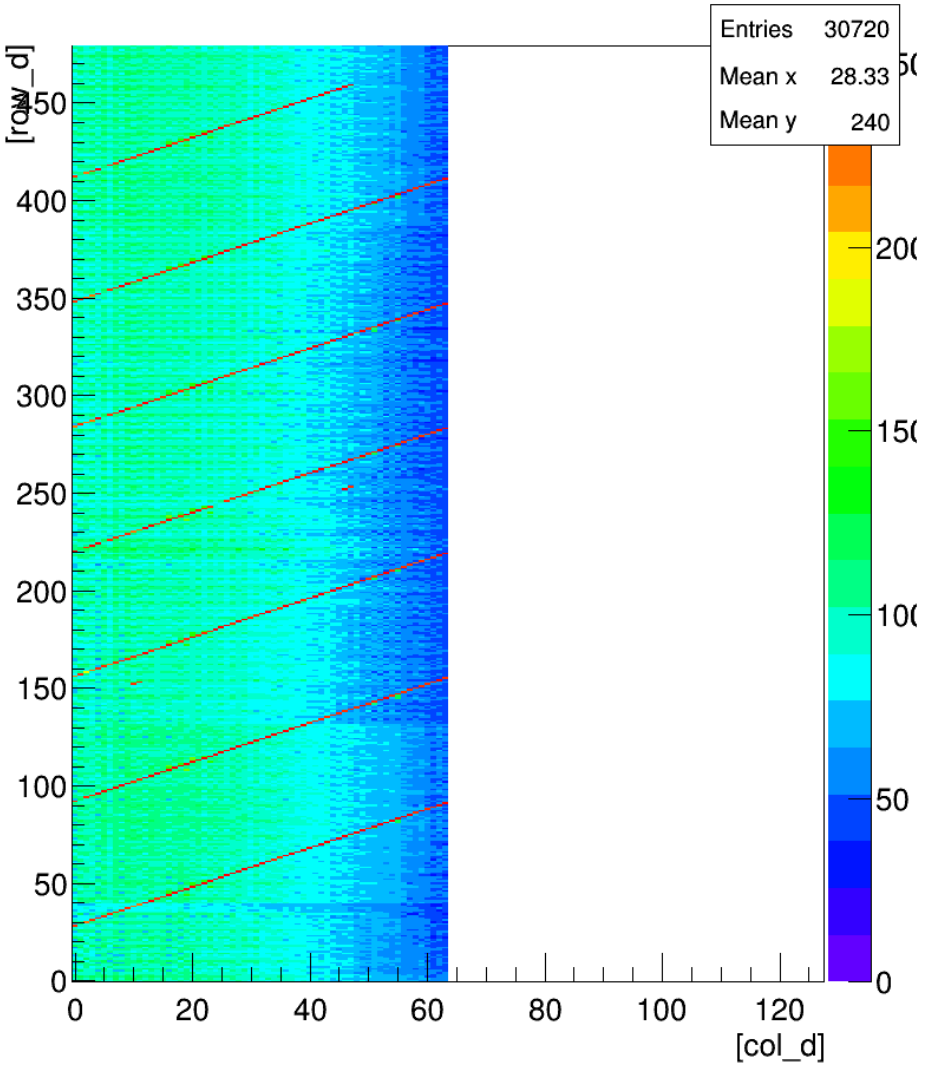
- **Normalized sigma + normalized bad pixel count**
- **Not optimal yet**



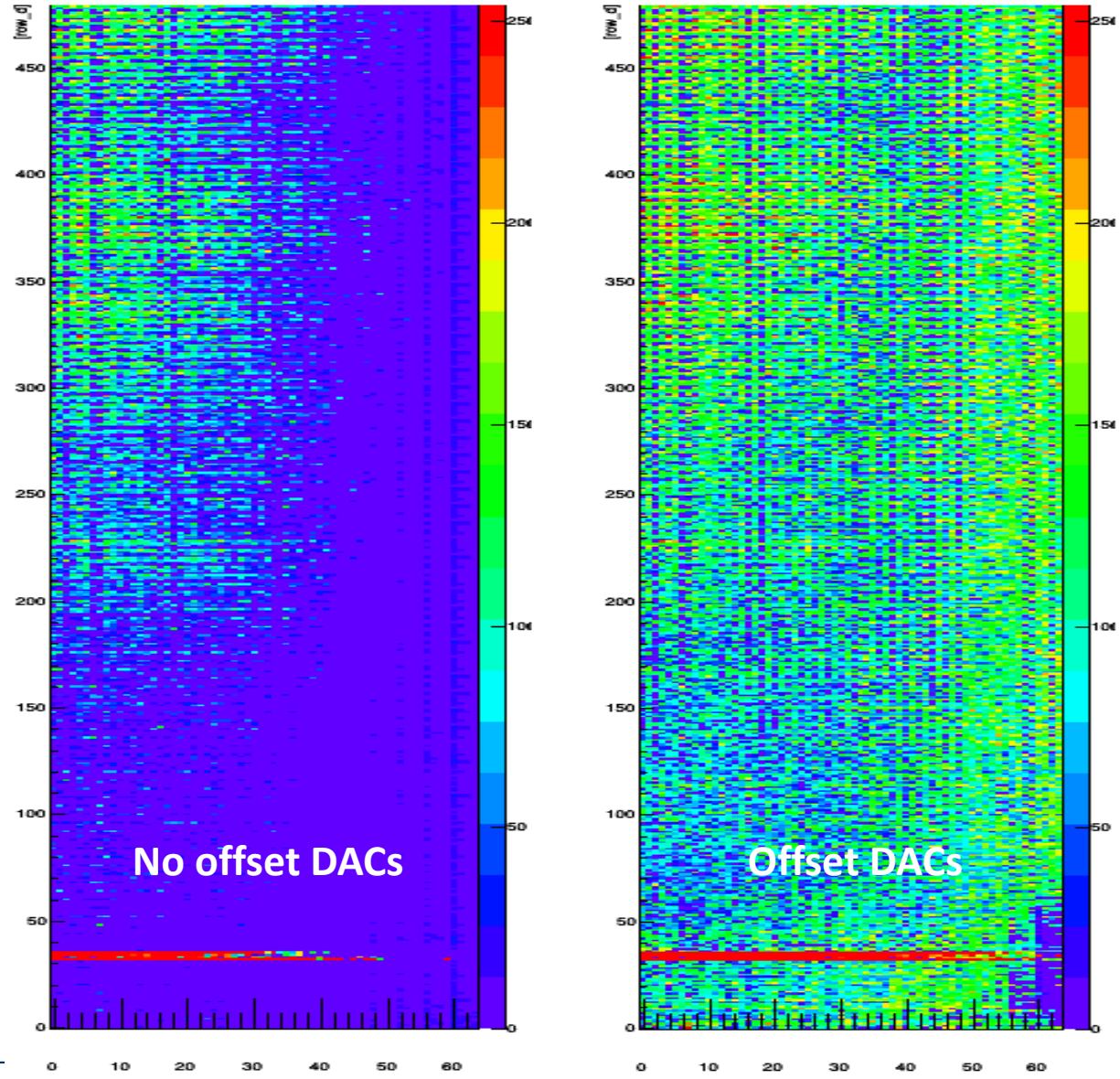


Timing and Mapping

- **Offset DACs finally in operation**
  - Automated data taking
  - Calculation
  - Uploading of right settings
  - Mapping and timing settings

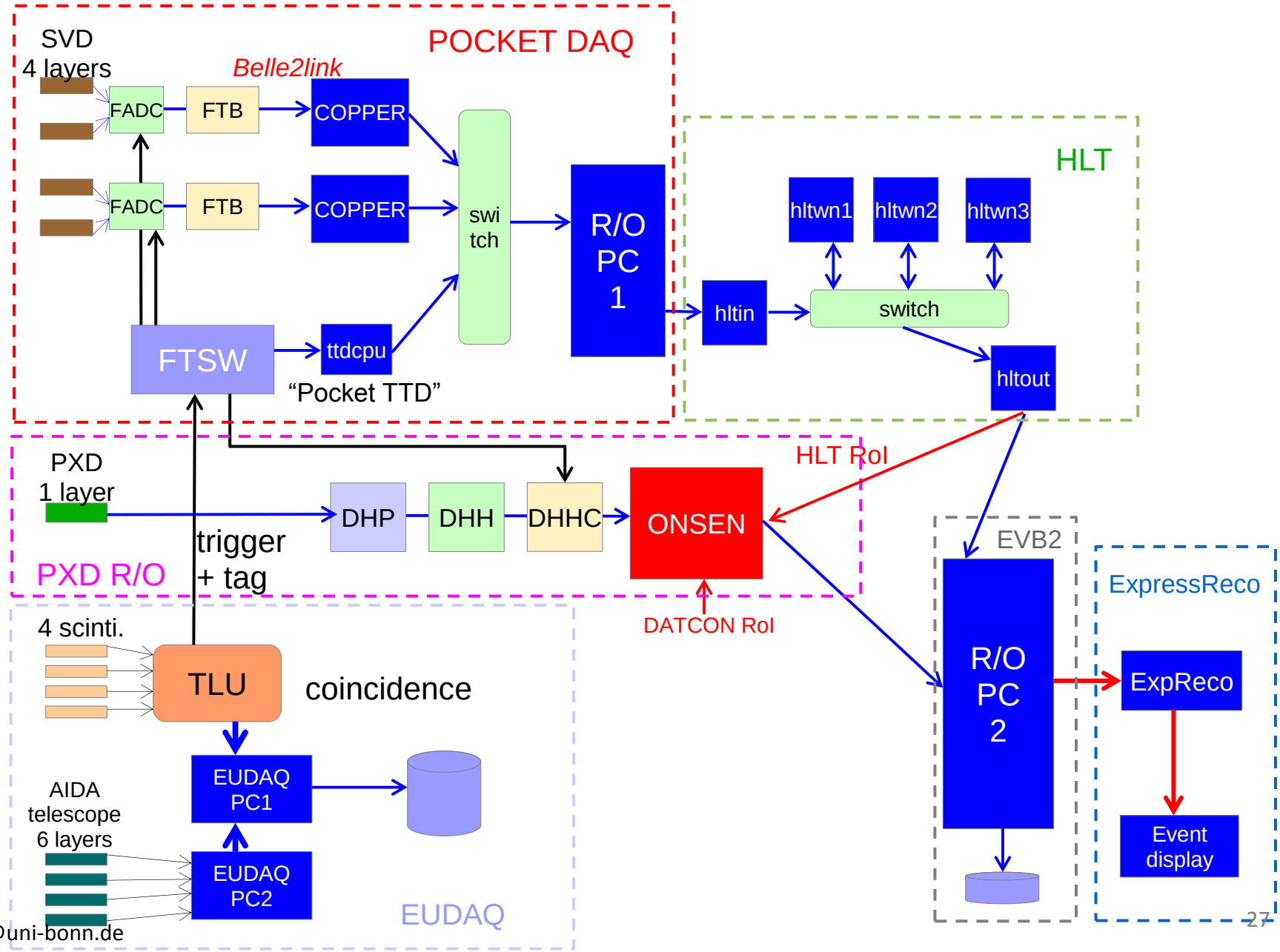


Corrected Pedestal Distribution



Pedestals homogenized with DACs in operation and coarse tunning

Test Beam VXD DAQ Structure



1.- Baseline