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SI LAB
Silizium Labor Bonn

PXD SC meeting

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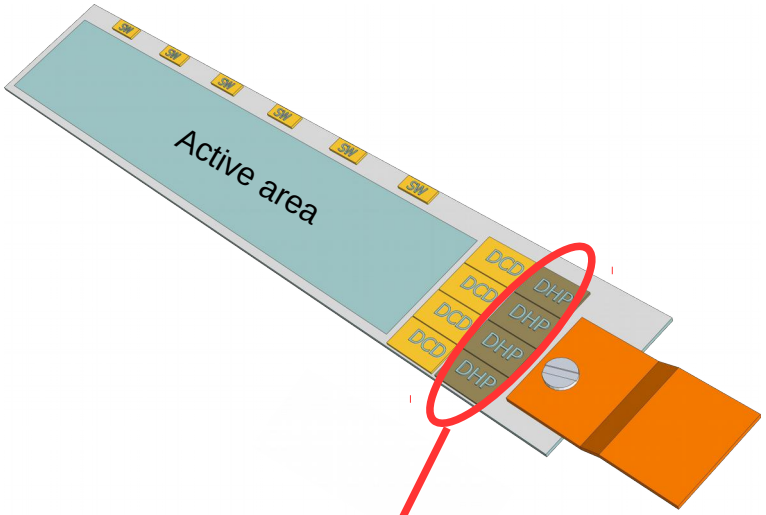
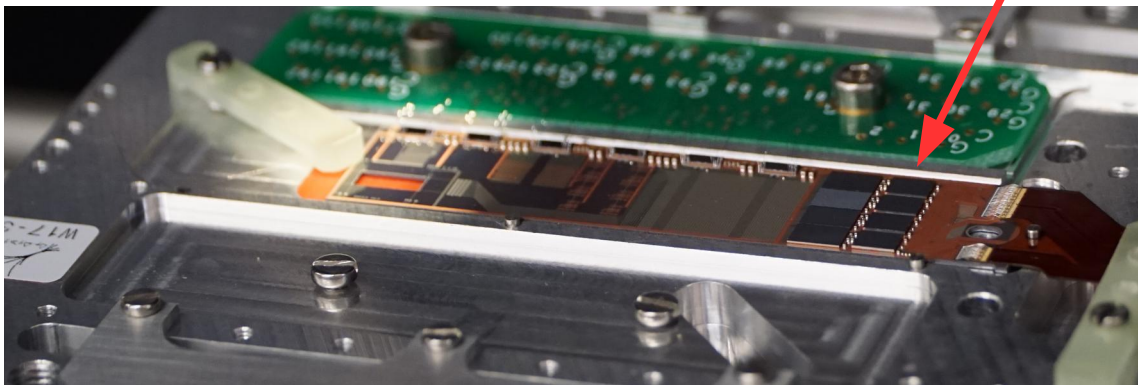
DHP (Data Handling Processor)

- Technology 65 nm TSMC → DHPT
- Two major tasks
  - **ASIC control** on-module
  - **Data reduction/transmission**

- ASIC control:
  - Generates the on-module clocks
  - Controls JTAG chain to the DCD (Drain Current Digitizer)
  - Stores the sequence of the Switchers on chip

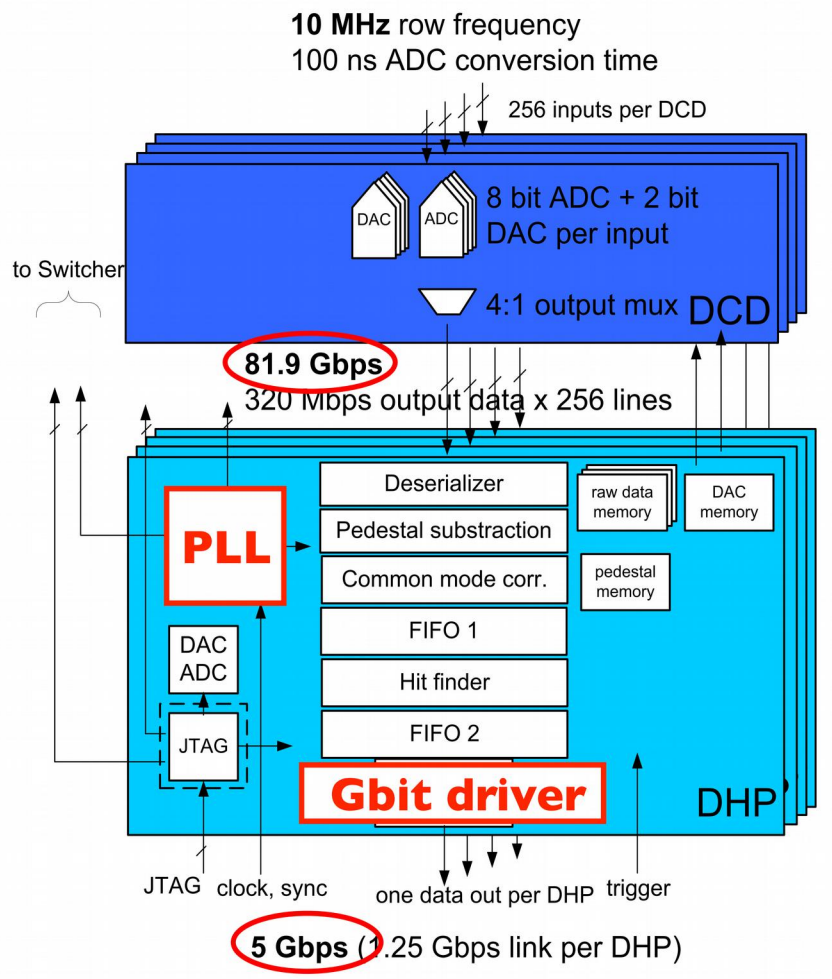




- Data reduction
  from 20.5 Gbps to 1.25 Gbps per DHP
  - Pedestal subtraction
  - Common Mode correction
  - Trigger
  - Hit finder
    - FIFO 1: 64 x (16bytes depth)
    - One hit per one clock cycle
    - FIFO 2: 4096
    - designed for 3% occupancy

- Clock (PLL) spread to DCD and Switchers
  - 76.25 MHz ref. clock
    - to 1.525 GHz output
    - and 305 MHz to DCD

- Gbit serial link (with adj. pre emphasis)



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DHP relevant monitoring

Slow Control:

- Voltages, current consumption
  - VDD 1.2V, DVDD 1.8V
  - time series?
- Temp Sensor (DACs) of DHP
- Read back JTAG registers for check → global / core registers
- Read switcher sequence

Data Quality Monitor:

- Occupancy (assumed 3%) → lose data if too high
- SRAM health → bit error counter (single/double)
- High speed serial link → Bit error rate tests (bathtub plot)