


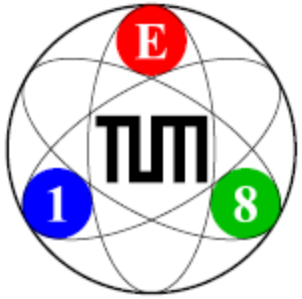

DHH Control

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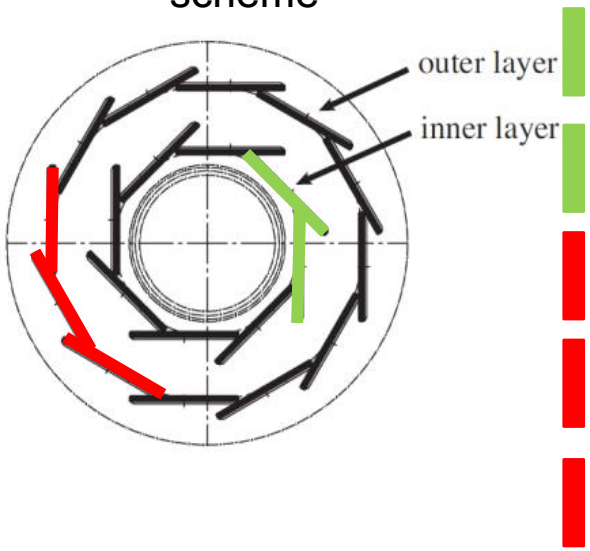
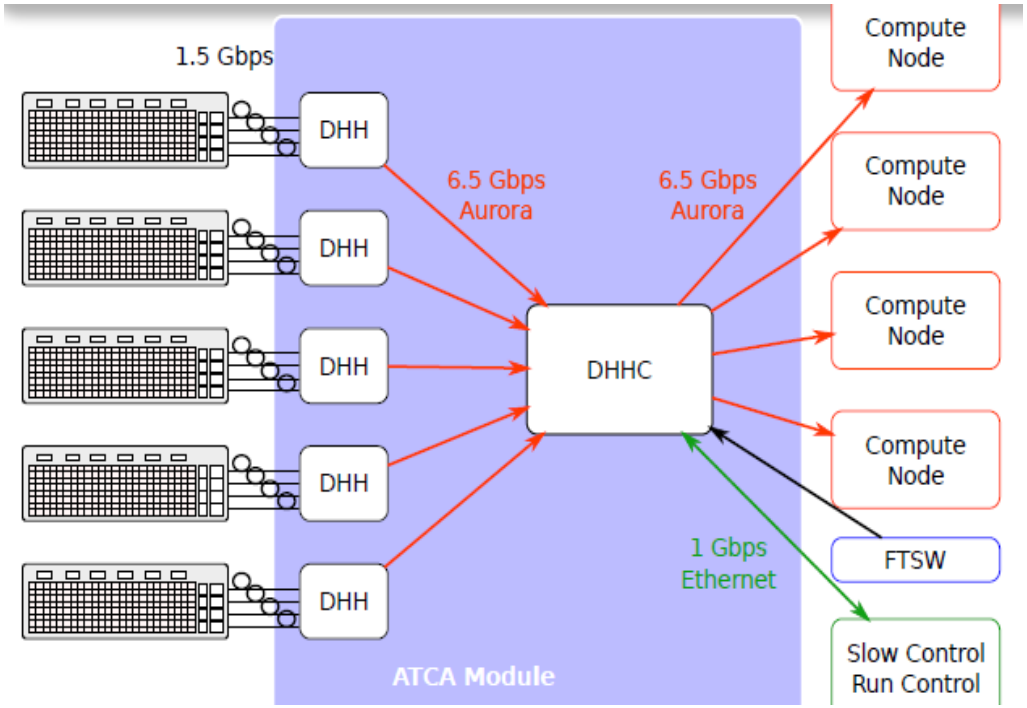
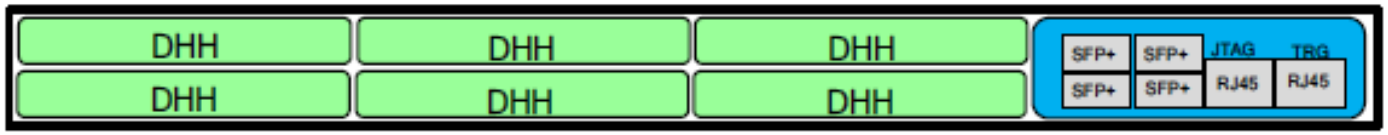
Munich 23-24 of 2014

DHH/DHHC

Readout scheme







ATCA module

DHHC

- 2 Inner + 3 Outer layers
- Data Load balancing : 70% from inner layer
- Maximum data throughput : 1.6 GB/s (3GB/s)
-

Full DHH system

- ATCA module = 5 x DHH + DHHC
- Full system 8 x ATCA modules

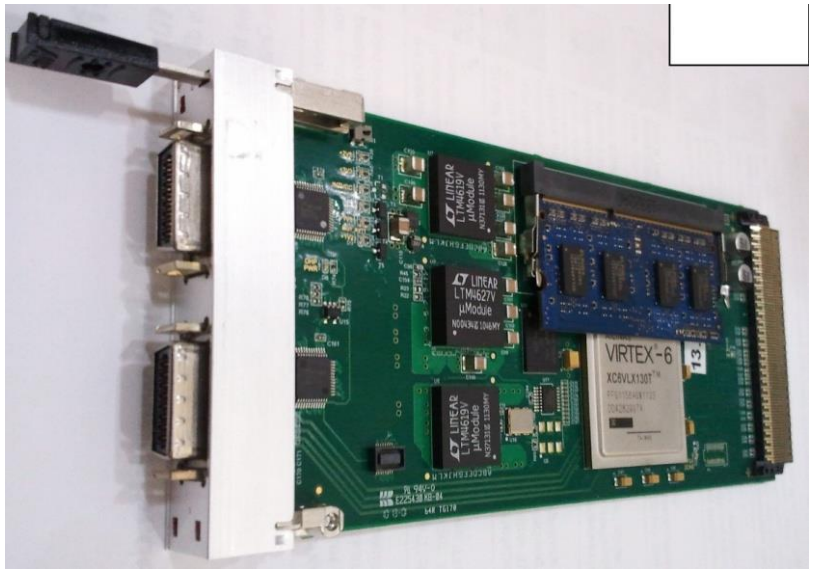
DHH progress

Hardware:

- Fixed JTAG bug in the layout caused by interference with DC/DC
- DHH used for testing EMCM and Hybrid 6 with full chipset :
  4xDCD+4xDHP+ NxSwitchers
- Current monitor tested succesfully

New DHH software:

- Removed redundant code
- Object oriented style instead of functions



Integration of new ASICs:

- DCD pipeline has been integrated
- DHPT has been integrated

Firmware development:

- Handling overlapping events
- DHHC sub-event builder

ATCA management

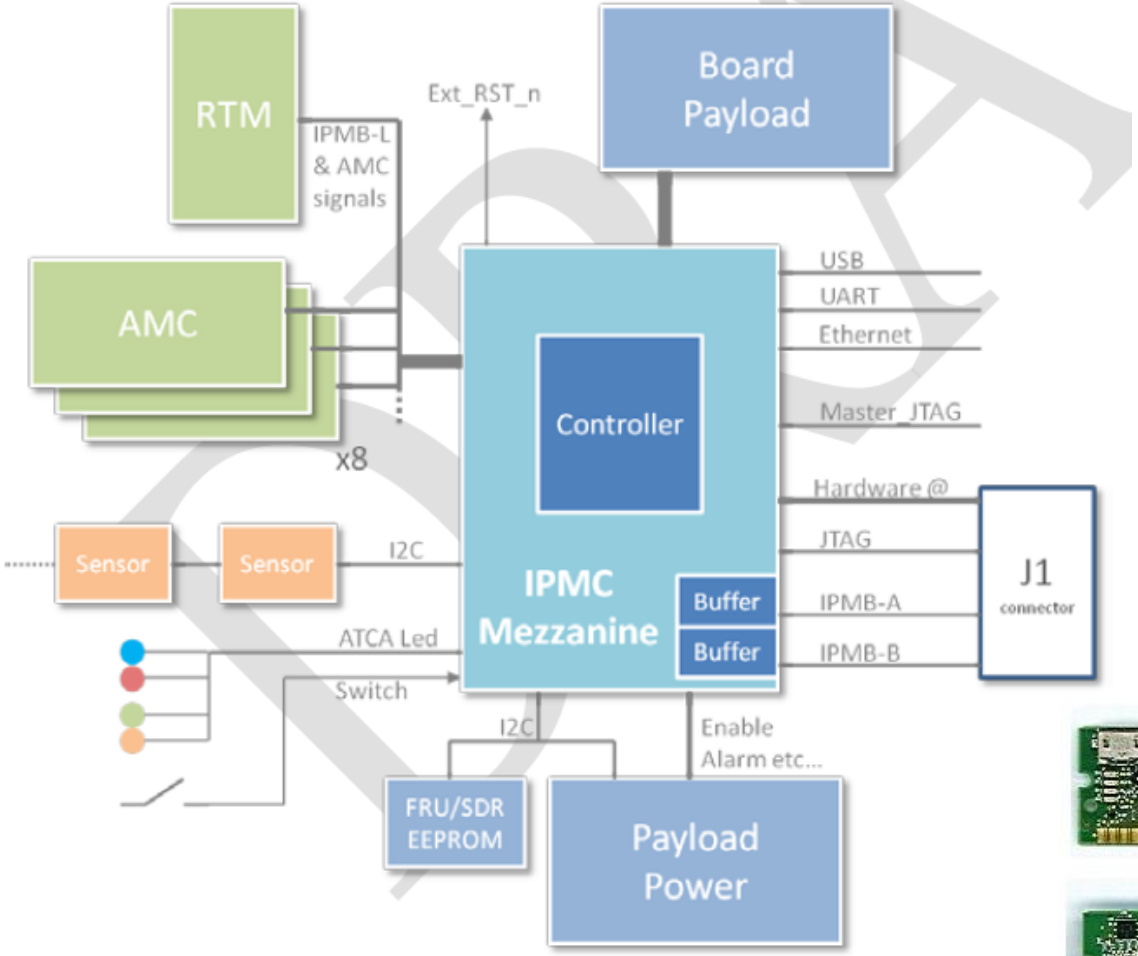
Concept of ATCA shelf management

- Power +48 V, always present
- Shelf manager:
  - FAN control according to power consumption
  - Measures shelf temperature
  - ATCA carrier cards controlled via IPMI
- Carrier card management done by IPMC

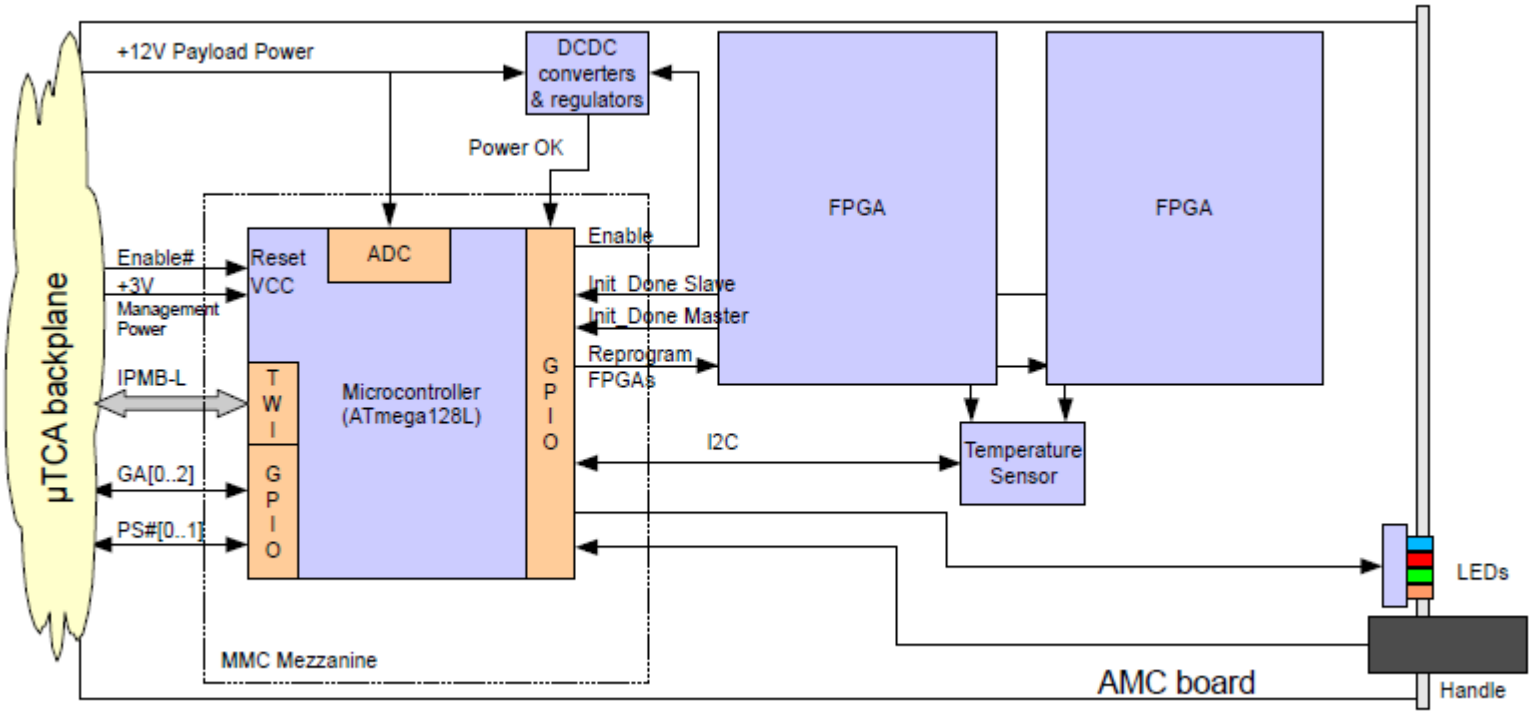
Another standard uTCA shelf
Management done by MCH

IPMC(carrier card manager)

- http://lappwiki.in2p3.fr/twiki/bin/view/AtlasLapp/ATCA



Module Management Controller



MMC development is joint effort of CPPM + DESY + CERN

- Software provided under free GNU license
- CERN produced 50 cards for DHH AMC

DHH++ Slow Control

Done:

- Integration of half ladder + DHH + DHHC into EPICS
- Synchronization of power up sequence with PS
- Visual control of Data Flow

To do:

- FPGA firmware uploading via IPBUS
- System integration
  - extending system to 40 half ladders
  - Automatization of pedestal measurement and uploading
  - Defining and monitoring boundary conditions: T,I, Occupancy, Noise …
  - Interfacing with RUN control