DHH System

Dima Levit

Physik Department E18 - Technische Universität München

Max Planck Institut für Physik München
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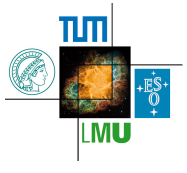
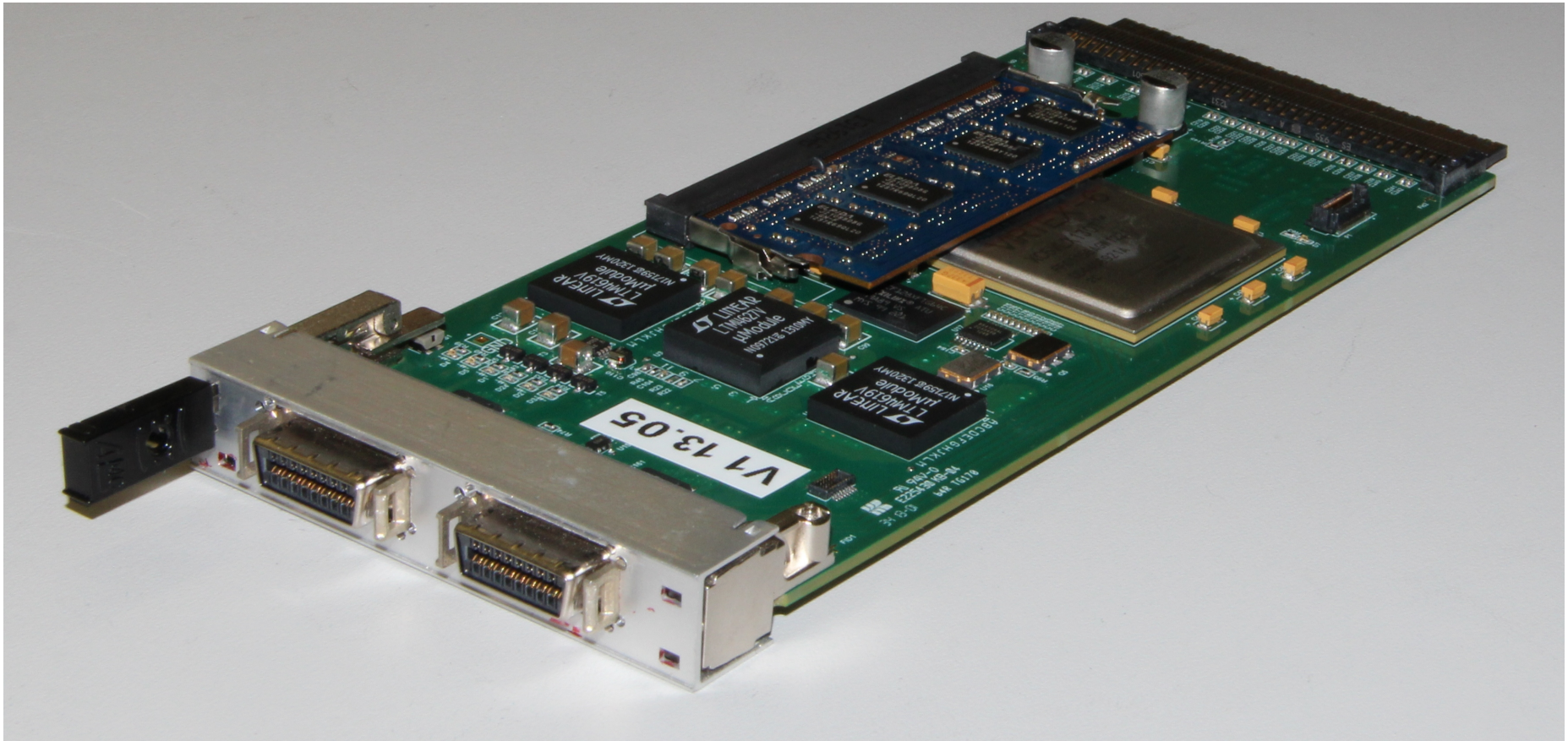
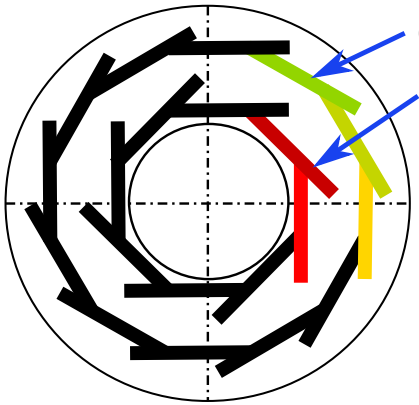


DHH/DHHC Hardware

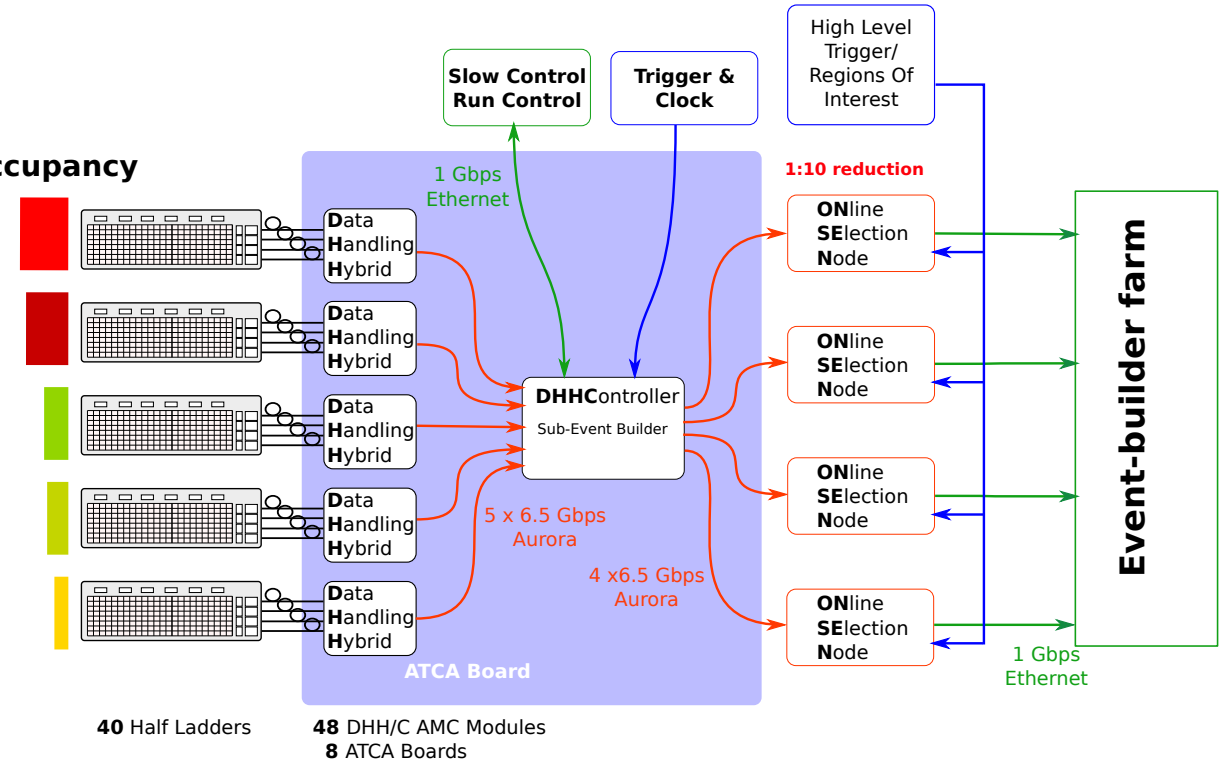


DHH - Data Handling Hybrid

Overview

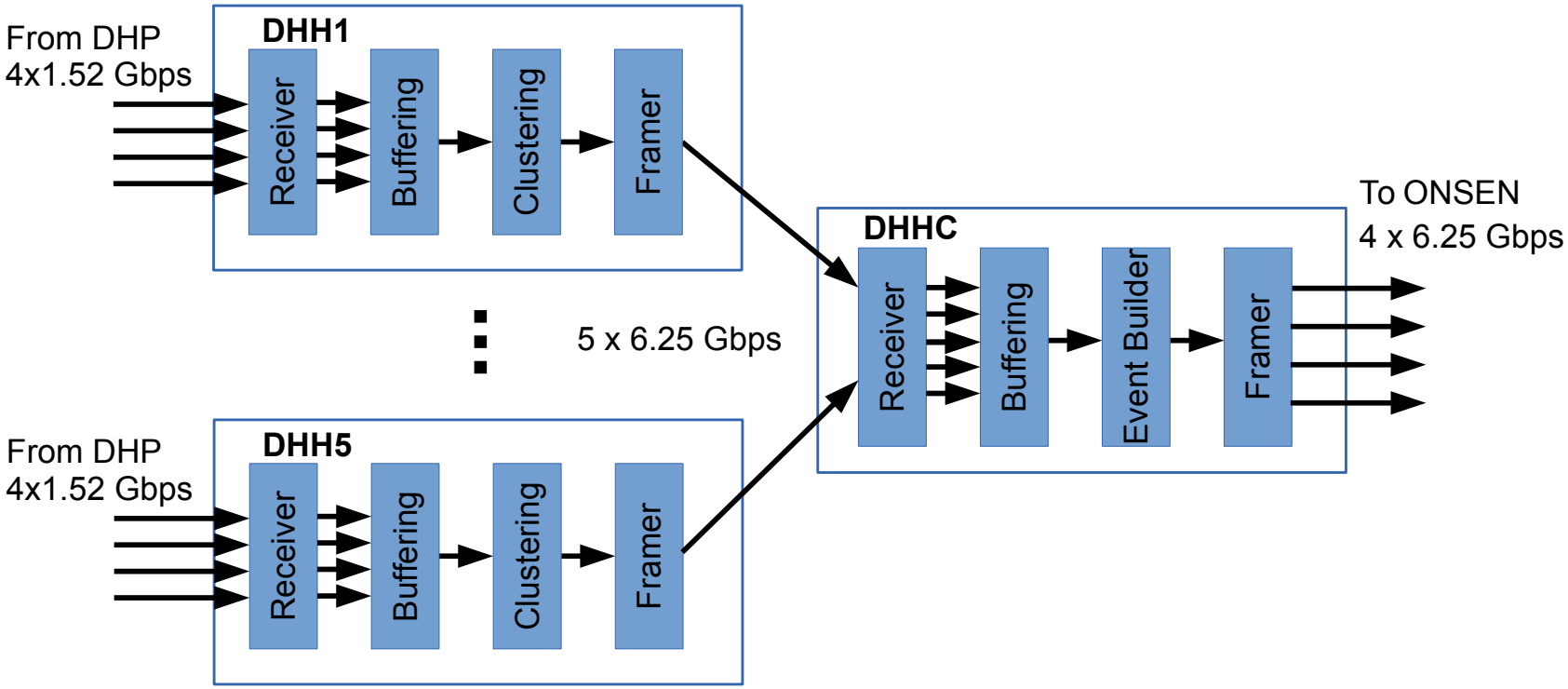


Belle2 Pixel Detector



Outline

Data Path



- 40 DHH and 8 DHHC modules

DHH

- ✓ 4 x 1.52 Gbps Aurora 8b / 10b data lines.
- ✗ Buffering in 4 GB DDR3 memory. Max. latency 5 s.
- ✓ DHH framing: event/error information.
- ✓ Pipelined cluster reconstruction.
- ✗ Neural network based cluster shape analysis.

DHHC

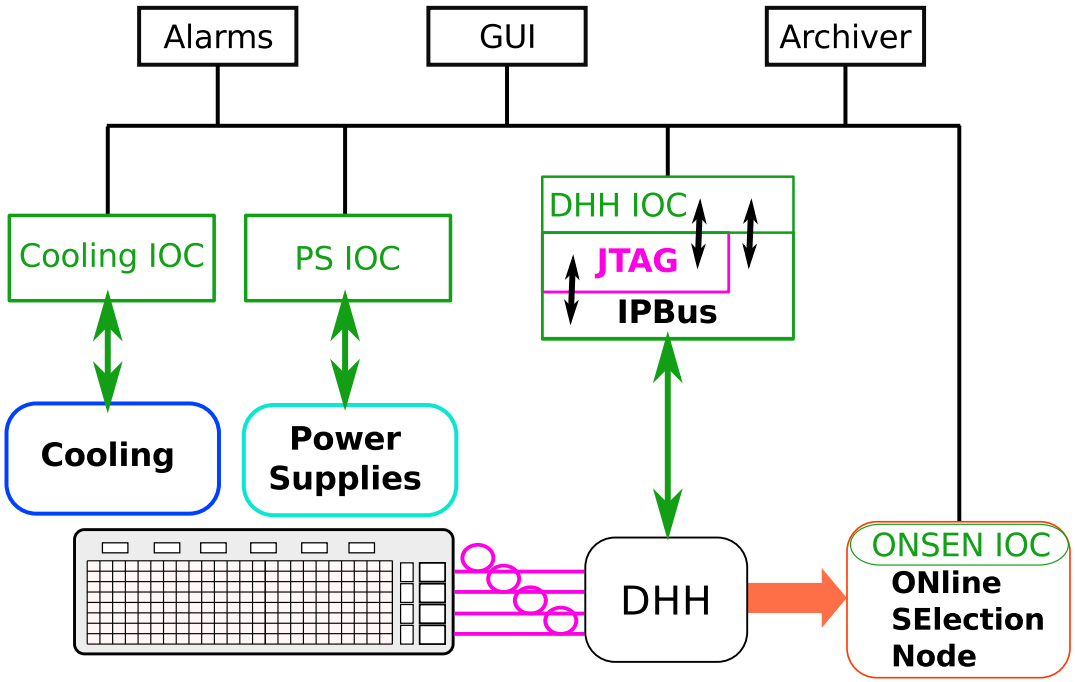
- 5 6.25 Gbps incoming links, 4 6.25 outgoing links
  - sub-event building
  - data rate averaging
- Decision on sub-event distribution to ONSEN modules done in LUT

Outline

Data processing

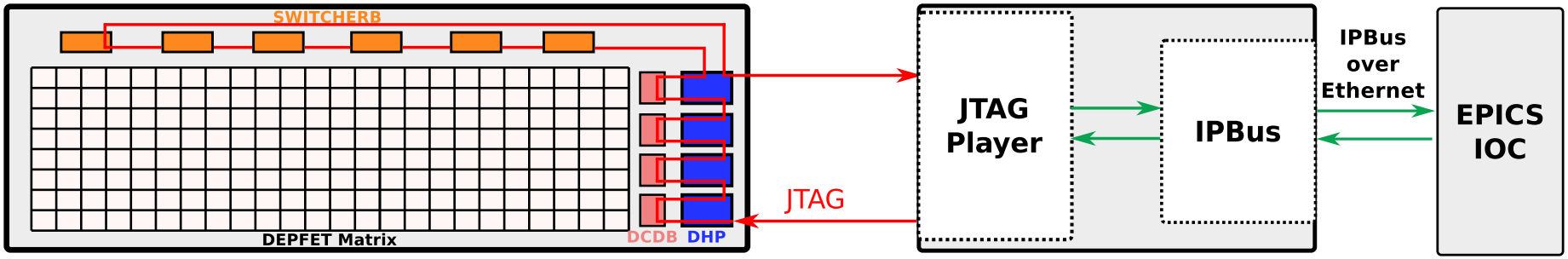
Slow Control

Communication Protocols / EPICS



- Slow control over Ethernet
- PXD ASICs configuration over JTAG
- DHH control over IPBus

JTAG Communication



- **Logical level:** EPICS IOC
  - JTAG registers model
  - bitstream generation
- **Transport level:** IPBus
- **Physical level:** JTAG player in DHH FPGA
  - bitstream execution

Slow Control

ASICs

- ✓ Configuration over JTAG
- ✓ Programming of the DHPT memory to update pedestals / offset DACs for DCD (define dynamic range of the ADC) / switcher sequence:
  - slow access over EPICS
  - fast write access over custom UDP protocol bypassing EPICS
- ✓ Periodical update of the configuration registers
- ✗ Monitoring of the temperature sensor

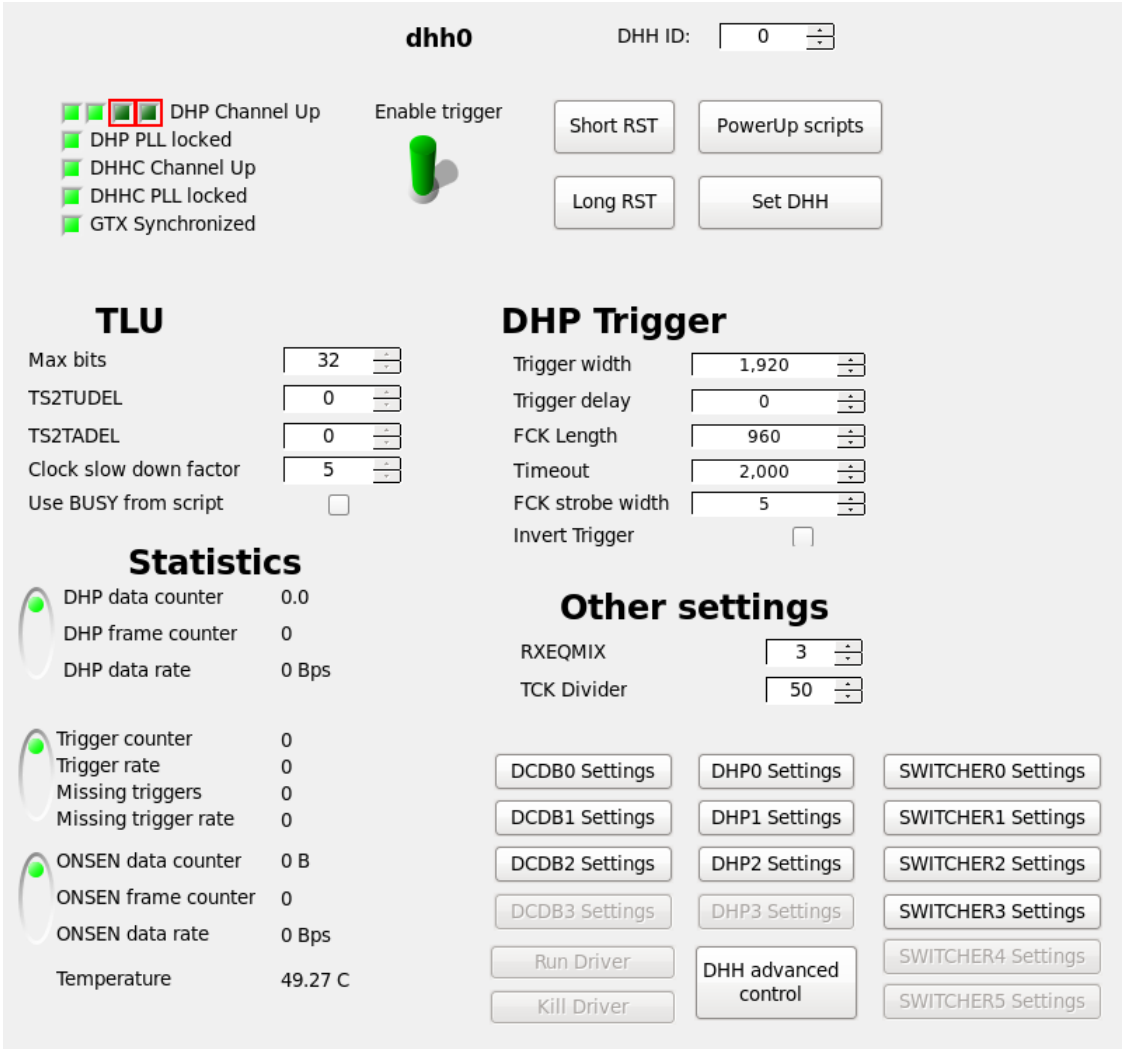
DHH/DHHC

- ✓ Module configuration at the beginning of the run
- ✓ Environment monitoring
- ✓ Monitoring of the data read out
- ✓ Control over current mirror (source) for DCD calibration
- ✗ Interface to PS for automatic power-up sequence

DAQ / DQM

- ✗ Data flow control
  - collecting and monitoring of data processing statistics
  - monitoring of the buffer fill levels
  - recovery of data flow faults
  - visualisation in CSS GUI
- ✗ Updating sub-event distribution LUT in DHHC
- ✗ High level negotiation with triggering system (e.g. if buffers are almost full)
- ✗ Calculation and loading of pedestals / offset DACs. Management of the pedestals memory.
  - triggering full frames
  - receiving full frames from event builders / ONSEN
  - calculation of pedestals / offset DACs
  - programming over JTAG

DHH CSS GUI


dhh0
DHH ID: 0
DHP Channel Up
DHP PLL locked
DHHC Channel Up
DHHC PLL locked
GTX Synchronized
Enable trigger
Short RST
PowerUp scripts
Long RST
Set DHH
TLU
Max bits 32
TS2TUDEL 0
TS2TADEL 0
Clock slow down factor 5
Use BUSY from script
DHP Trigger
Trigger width 1,920
Trigger delay 0
FCK Length 960
Timeout 2,000
FCK strobe width 5
Invert Trigger
Statistics
DHP data counter 0.0
DHP frame counter 0
DHP data rate 0 Bps
Trigger counter 0
Trigger rate 0
Missing triggers 0
Missing trigger rate 0
ONSEN data counter 0 B
ONSEN frame counter 0
ONSEN data rate 0 Bps
Temperature 49.27 C
Other settings
RXEQMIX 3
TCK Divider 50
DCDB0 Settings
DCDB1 Settings
DCDB2 Settings
DCDB3 Settings
Run Driver
Kill Driver
DHP0 Settings
DHP1 Settings
DHP2 Settings
DHP3 Settings
DHH advanced control
SWITCHER0 Settings
SWITCHER1 Settings
SWITCHER2 Settings
SWITCHER3 Settings
SWITCHER4 Settings
SWITCHER5 Settings