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PXD Flex Cable
Prototype Characterization (V2.1/2.2)

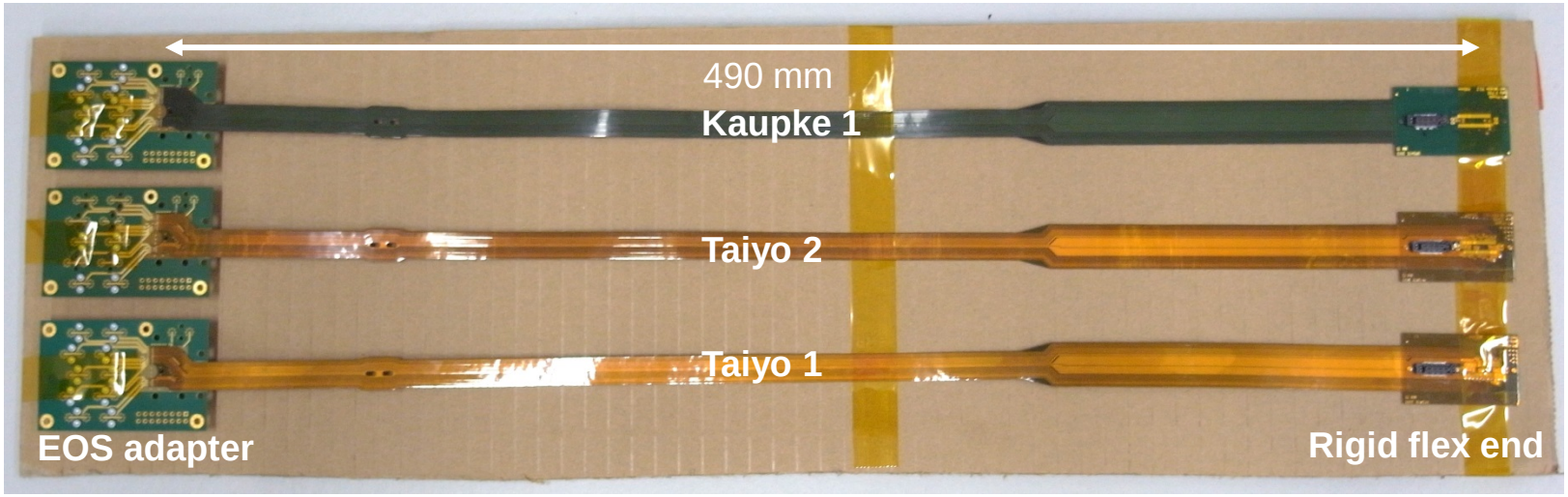
H.Krüger 14.8.2014

Outline

- Devices under Test
  - Taiyo Flex V2.1 (1st production)
  - Taiyo Flex V2.1 (2nd production)
  - Kaupke Flex V2.2
- TDR and TDT Measurements
- Results
  - DC resistance
  - TML impedance
  - Frequency depended attenuation
- Proposed design changes

Flex Cable Prototypes

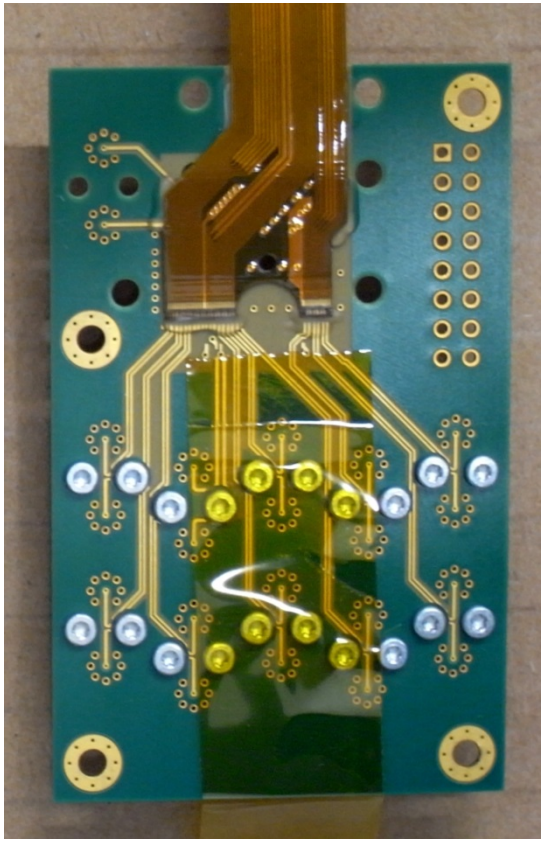
- Same design (MPI) produced by two different manufacturers (Taiyo, Kaupke)
  - length: 490mm
  - layers: 4
- Two productions by Taiyo (identical design data, V2.1)
- Kaupke design data with smaller via hole (0.2mm instead of 0.35mm, V2.2)
- Kaupke and Taiyo apparently use different layer stacks (see measurement data)



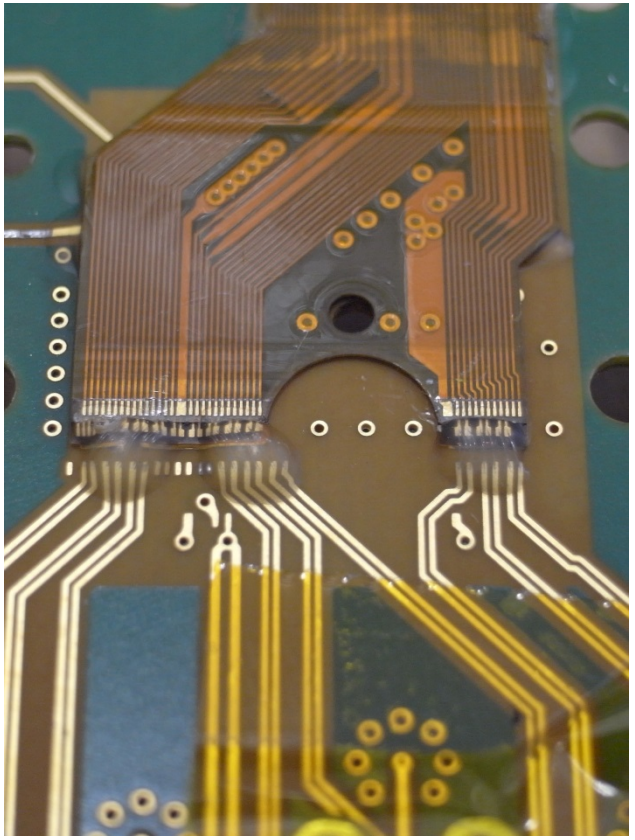
Flex cable prototypes with EOS adapter boards

Flex Cable – Module Side

- Adapter PCB to connect micro coax cables to the flex cable
- Two 25µm Al wire bonds per line, potted



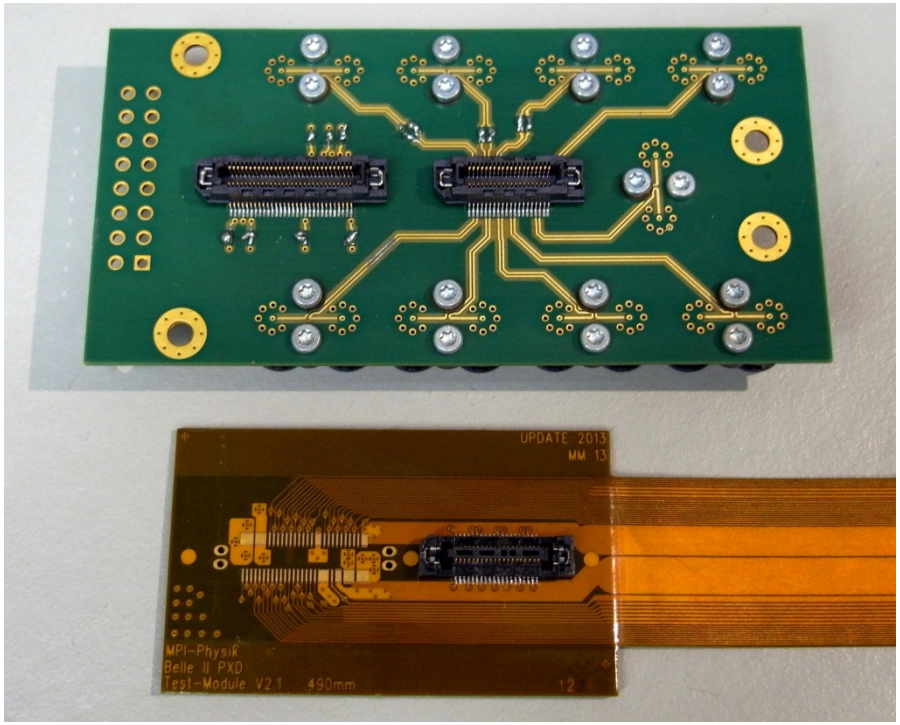
Flex adapter PCB, soldered and wire bonded to flex cable

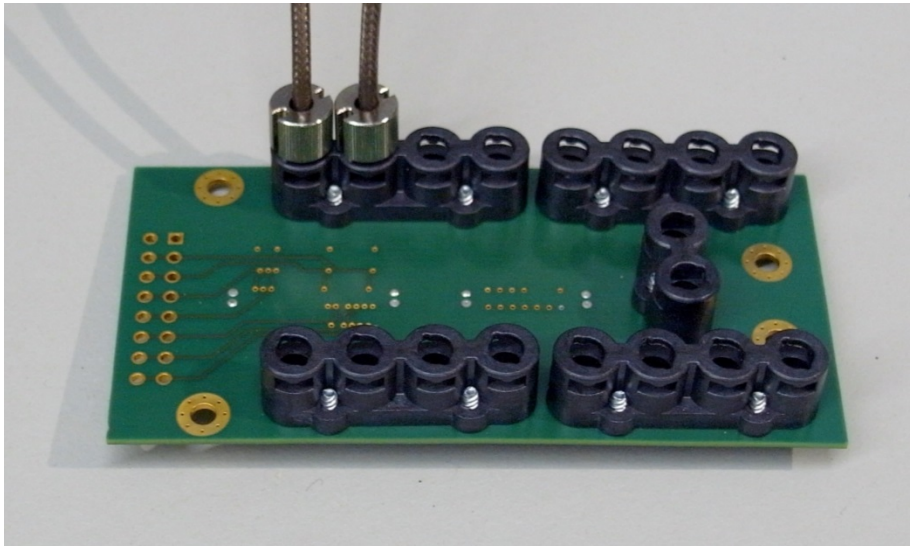


Wire bond detail

Flex Cable – Patch Panel Side

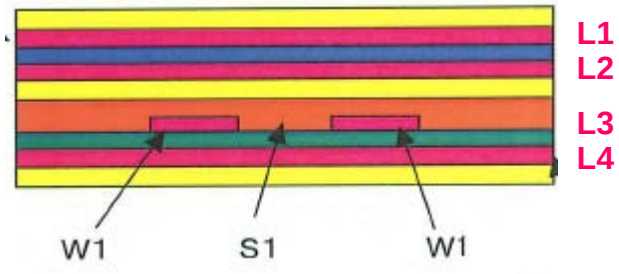
- Adapter PCB to connect micro coax cables to the rigid patch panel



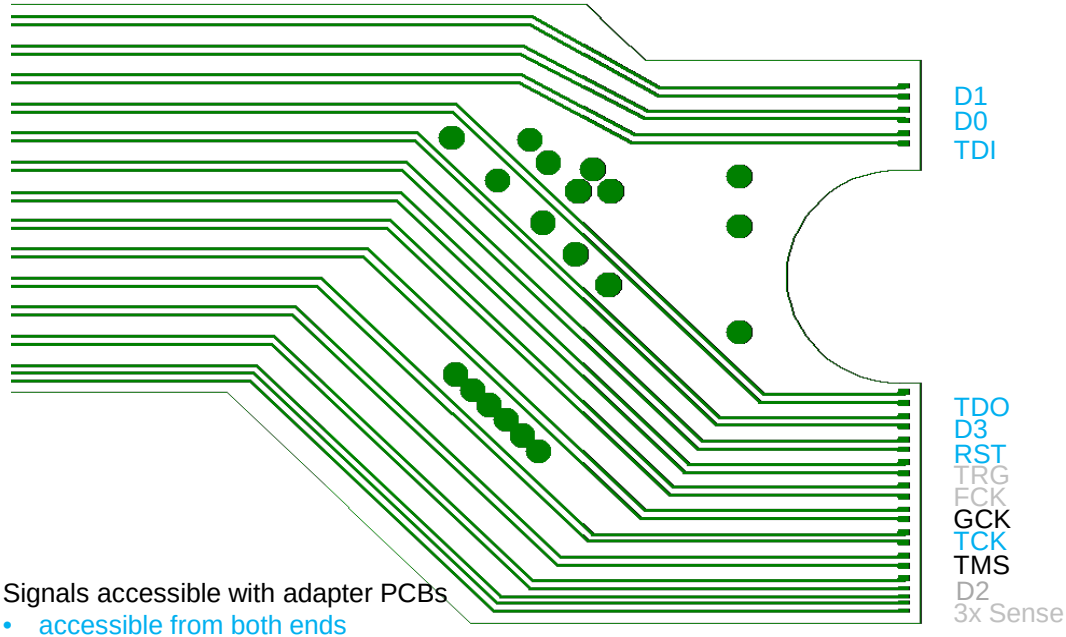


Design Details

- Impedance controlled differential pairs (most critical for Gbit link data lines D[3:0])
- Design goals
  - 100Ω diff. impedance (± 10Ω)
  - low DC resistance (< 8Ω)
  - good x-talk immunity



Layer stack (cross section), width (W) and spacing (S) of diff. lines on layer 3



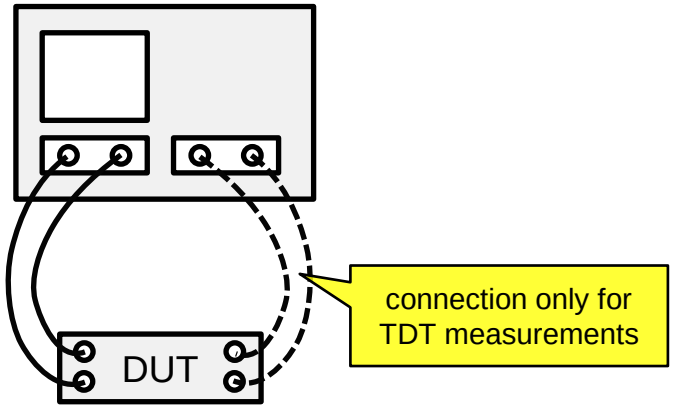
Signals accessible with adapter PCBs
- accessible from both ends
- accessible from module side only
- not accessible

Flex cable layout at module side, layer 3 shown only

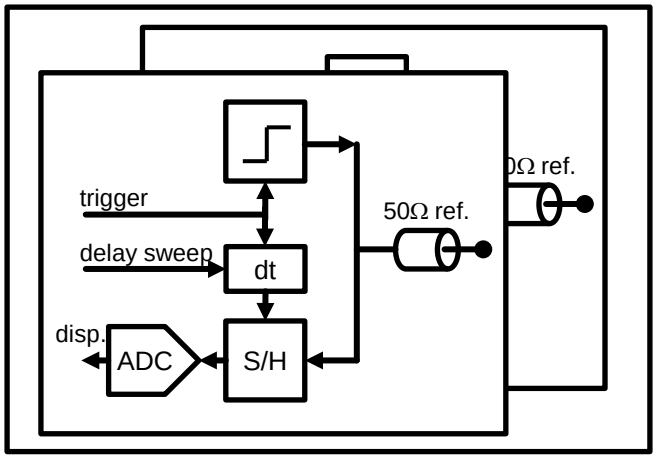
Measurement Methodology

- Digital Sampling Oscilloscope (DSA)
  - Very high input bandwidth (up to 30GHz)
  - Precision sample & hold at inputs
  - High resolution delay sweep of S&H trigger (sub ps)
  - Low speed, high resolution ADC (14 bit, 200ksps)

➔ Very accurate amplitude and timing resolution (works for periodic signals only)



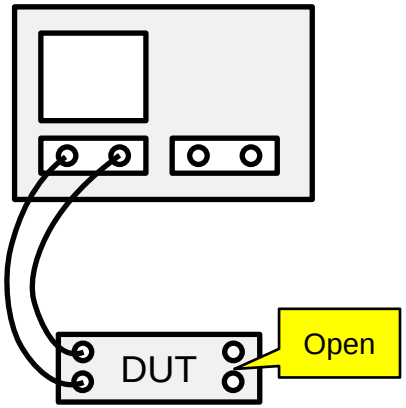
DSA with two dual channel TDR / Sampling modules connected to DUT with differential lines

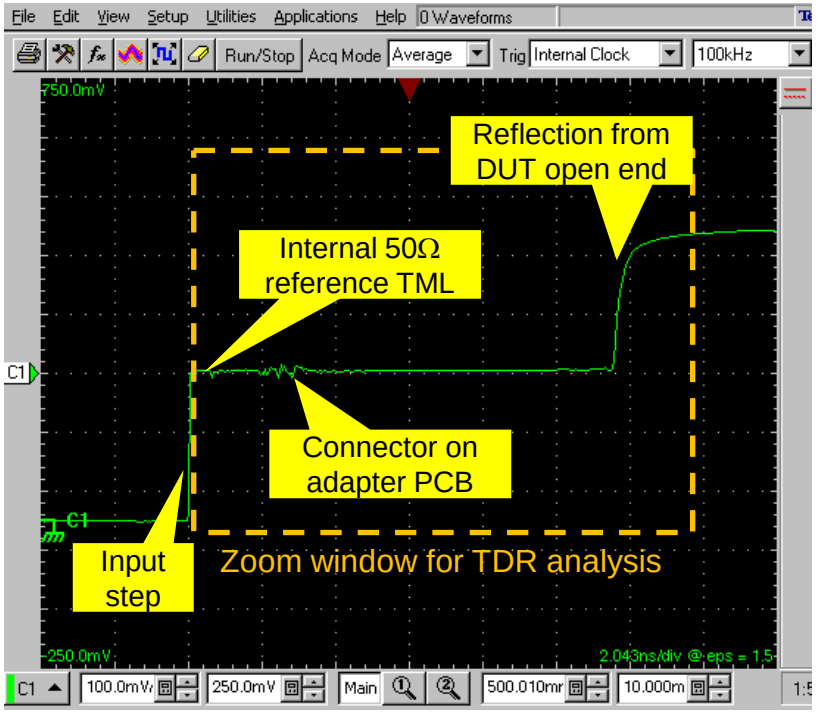


Dual channel TDR / Sampling module (step voltage generator and sampling stage can be activated independently)

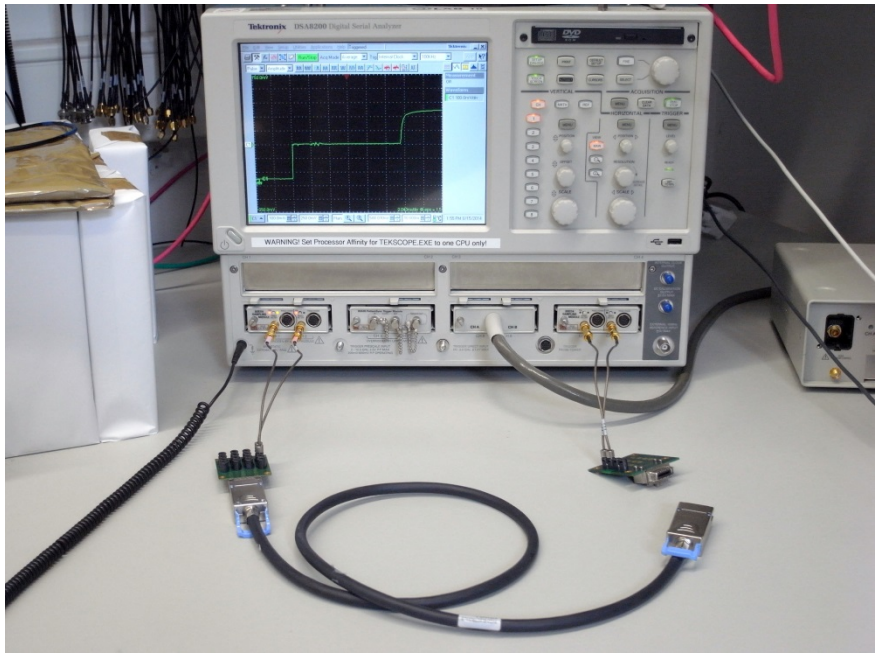
Time Domain Reflectometry (TDR)

- **Same TDR module** generates a voltage step and samples the reflected waveform
- Amplitude of reflected wave is proportional to the **impedance** along the DUT: $V_r(t) \propto Z(x)$





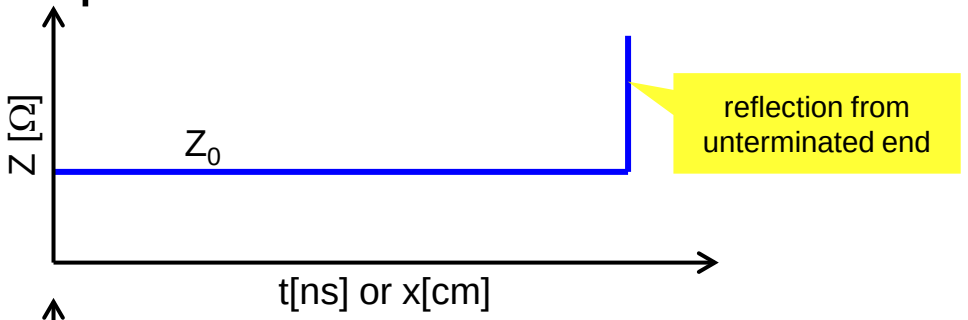
Measured TDR waveform



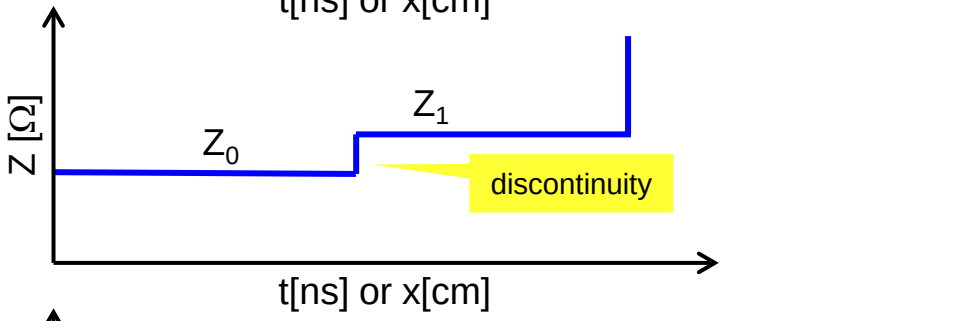
TDR setup with 1m Infiniband cable as DUT

How to interpret TDR Data

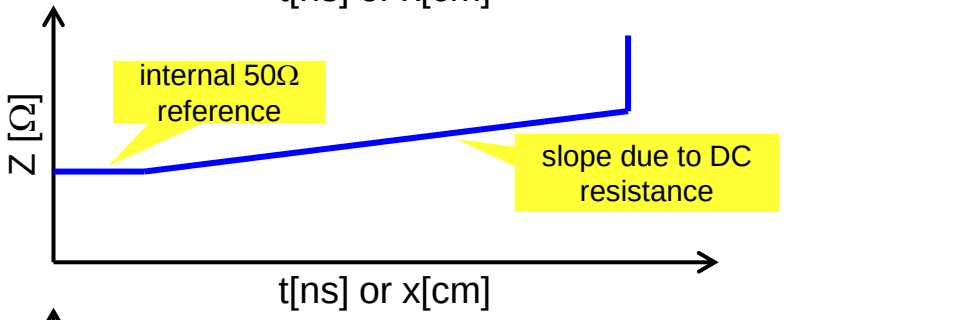
- Ideal transmission line



- TML with change in impedance

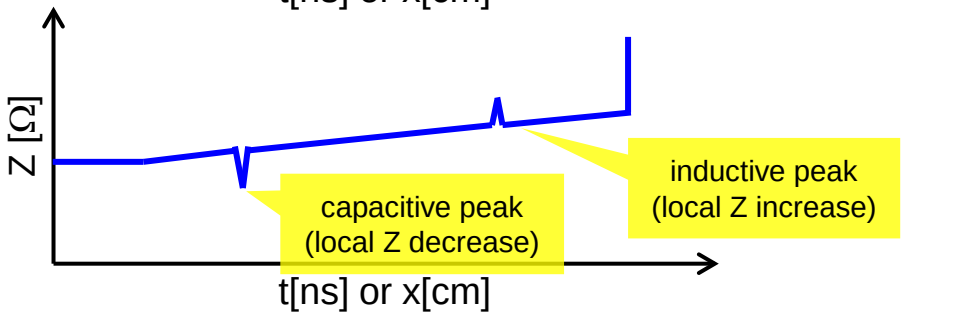


- TML with finite DC resistance



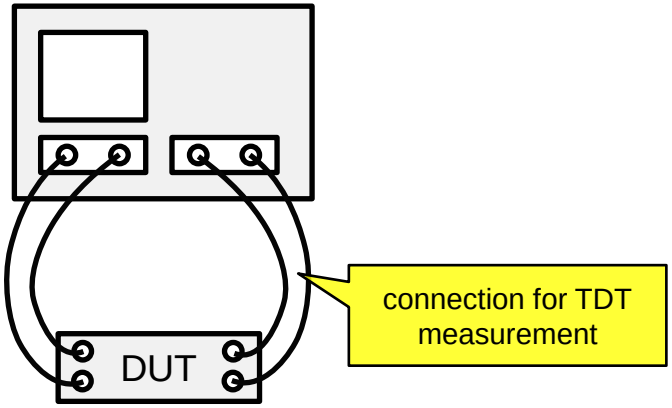
- TML with distortions

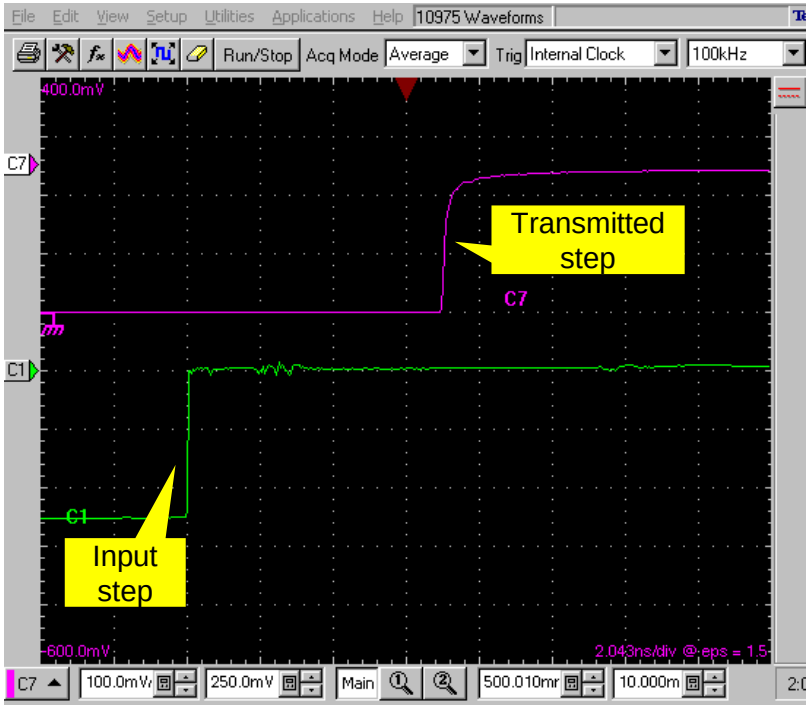
$$Z_0(x) = \sqrt{\frac{L'(x)}{C'(x)}}$$



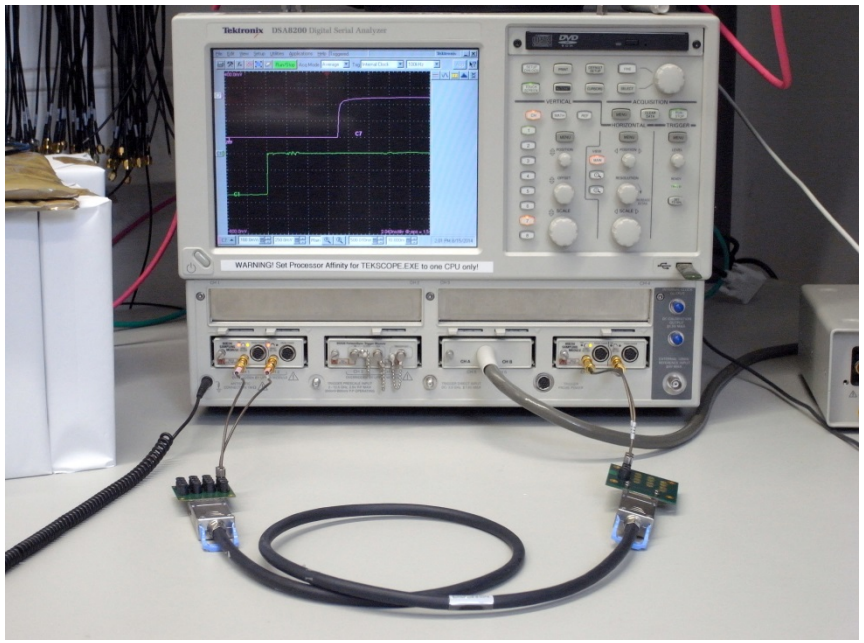
Time Domain Transmission (TDT)

- **One TDR module** generates the voltage step and the **second one samples** the transmitted waveform
- Analysis of input and output step functions yield the **transfer function *H(s)*** of the DUT





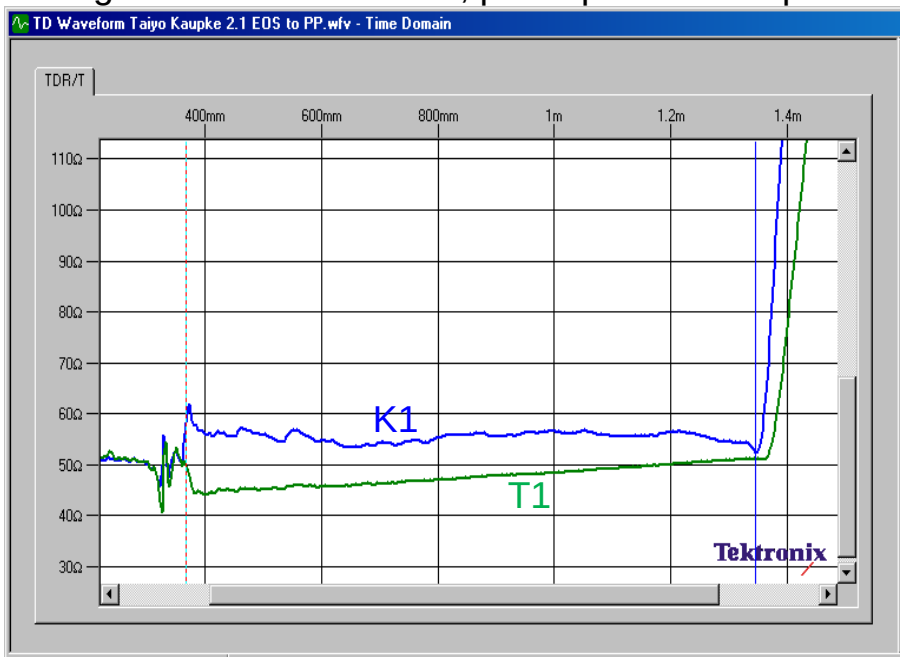
Measured TDT waveform



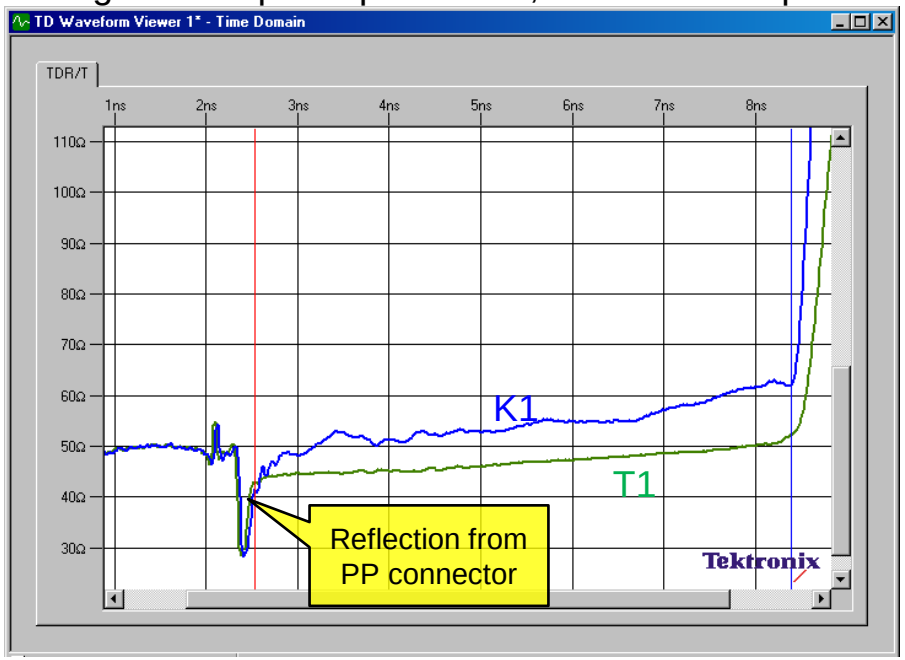
TDT setup with 1m Infiniband cable as DUT

Impedance Measurements (TDR)

Signal from module side, patch panel side open

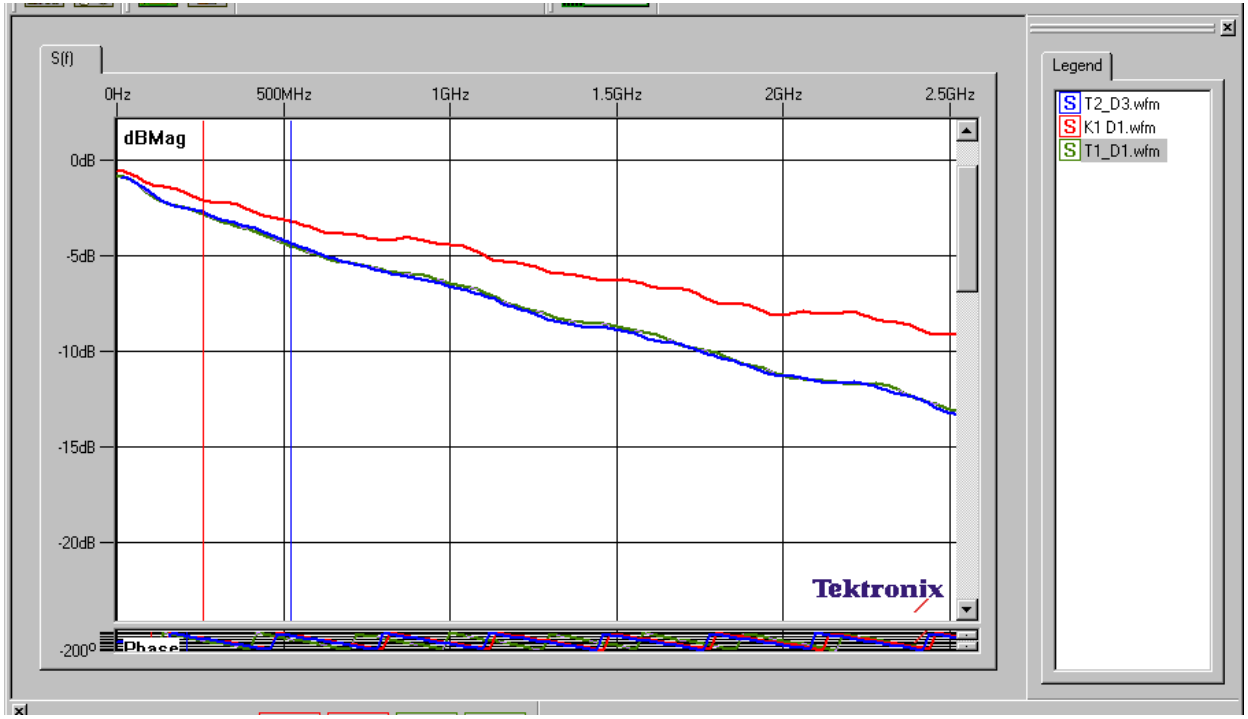


Signal from patch panel side, module side open



DUT	Diff. line impedance	Dielectric constant	Comment
T1 (Taiyo)	89Ω	3.1	Impedance constant along the cable
K1 (Kaupke)	90 - 116Ω	2.8	Impedance increases towards the module side of the cable

Attenuation Measurements (TDT)

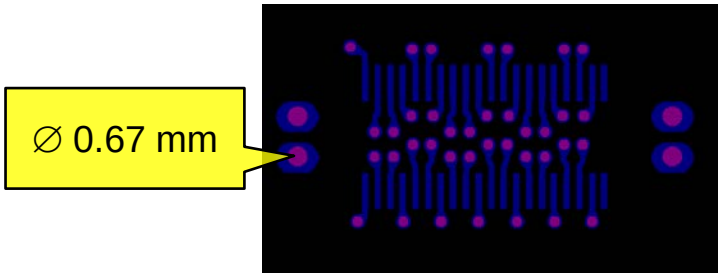


DUT	DC resistance (from DVM)	Attenuation @ 800 MHz	Attenuation @ 1.6GHz
T1 (Taiyo)	7.64Ω	5.75dB	9.03dB
K1 (Kaupke)	6.78Ω	4.19dB	6.55dB

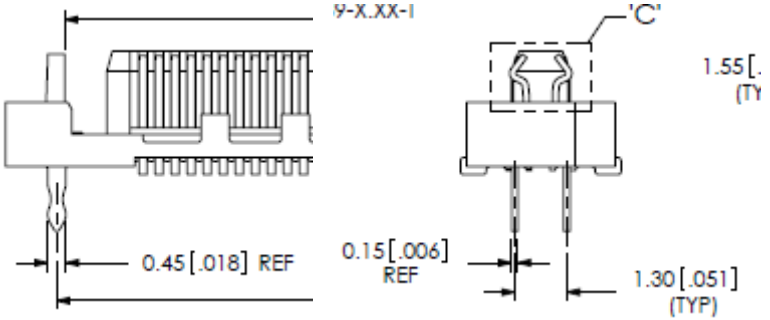
Proposed Design Improvements

- Poor alignment of data and power connectors (SAMTEC ST4) on patch panel
- Mounting holes diameter on PCB (0.67mm) much larger than connectors alignment pins dimension (0.45mm x 0.15mm)

➔ Recommendation: Reduce hole size to 0.5mm



Footprint in current design

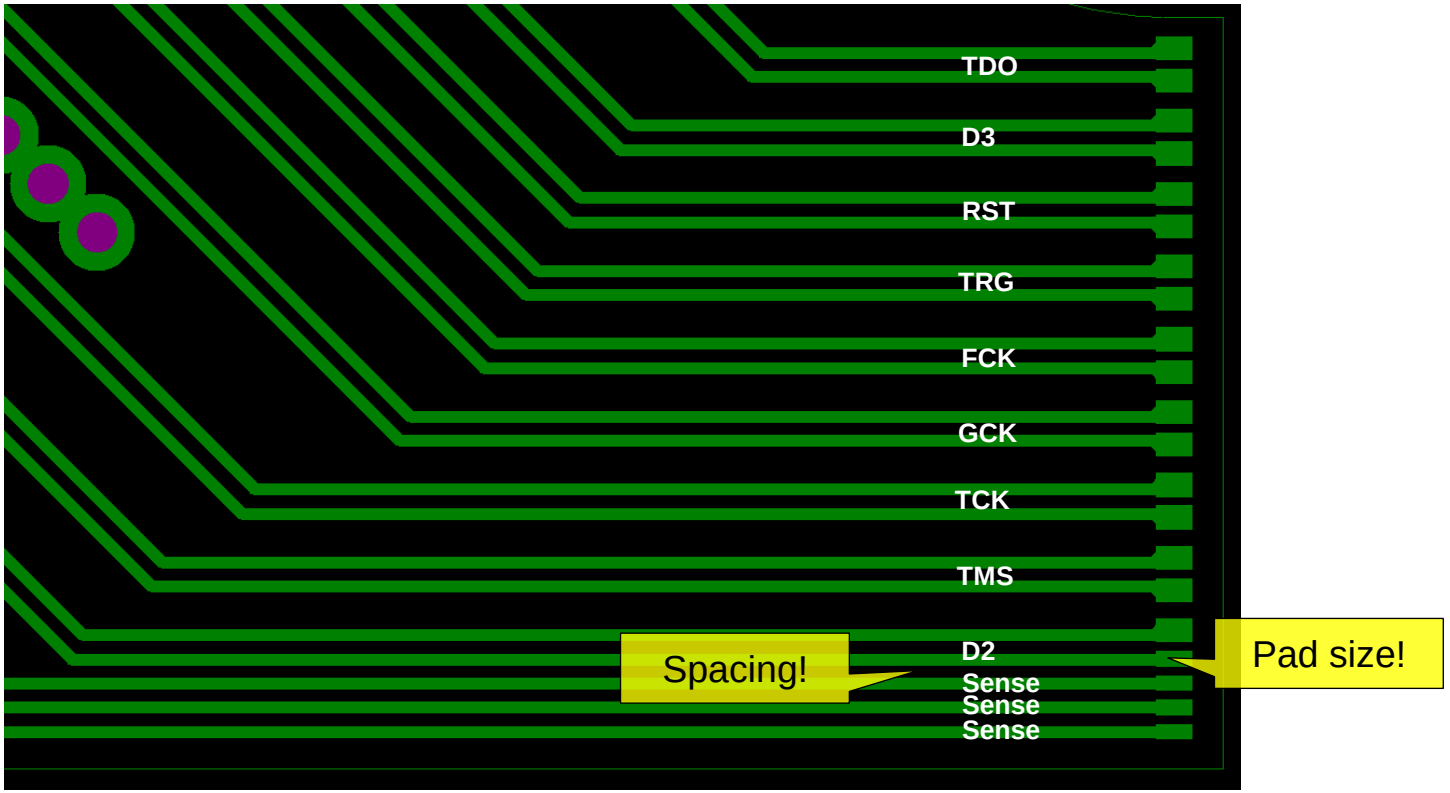


Samtec data sheet

Differential Lines Routing Details

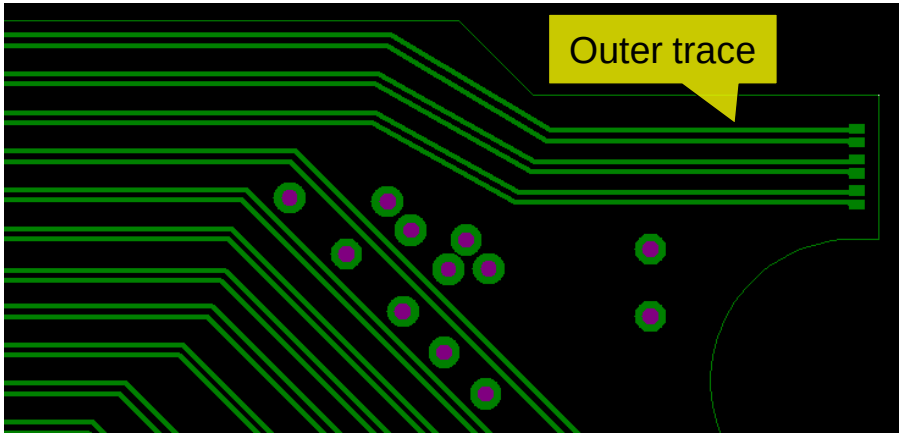
- D2 differential lines with little spacing to adjacent sense lines

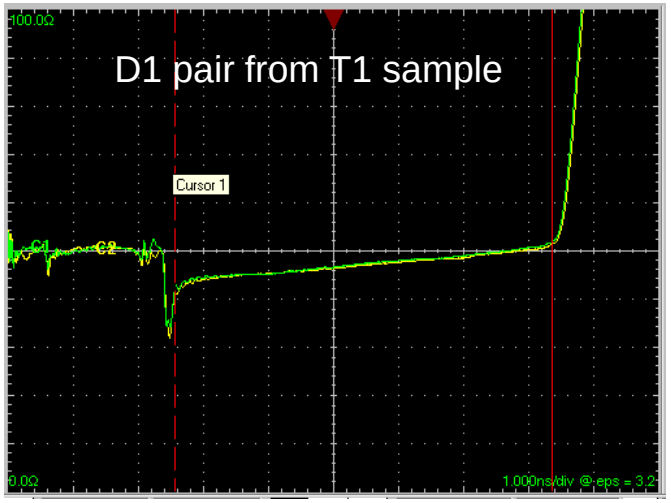
➔ Increase spacing between D2 and sense lines (remove RST and FCK lines)



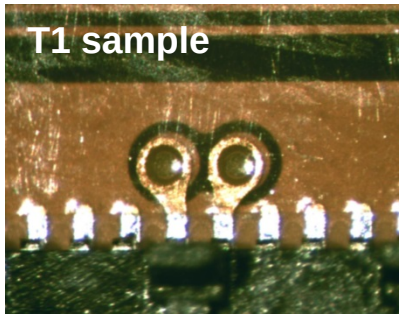
Differential Lines Routing Details

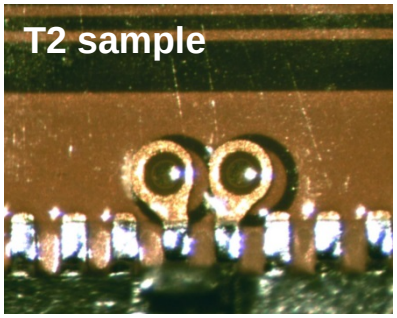
- Lines routed at the edge are critical



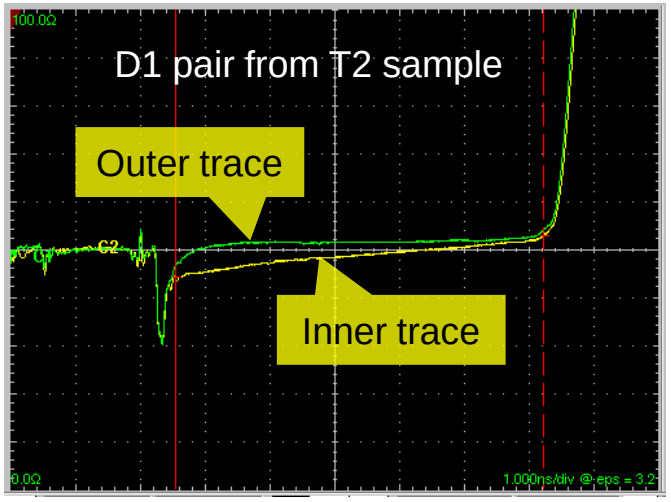


- Layer misalignment?



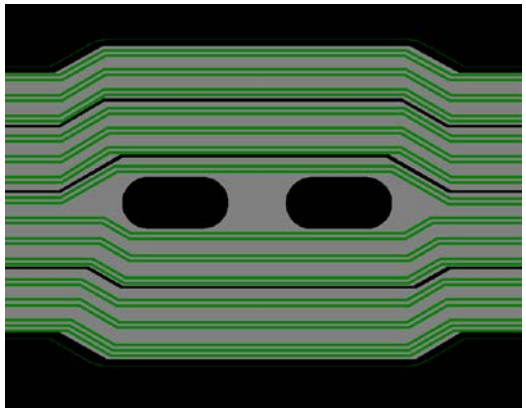


Zoom to PP data connector

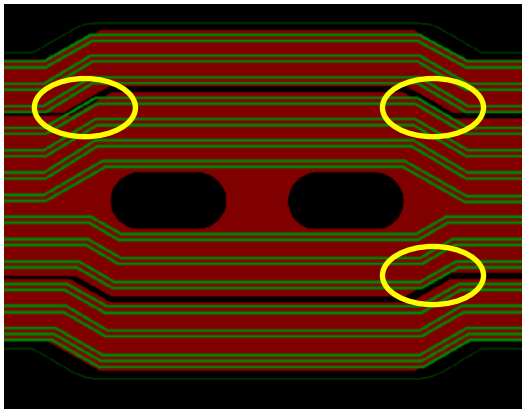


Differential Lines Routing Details

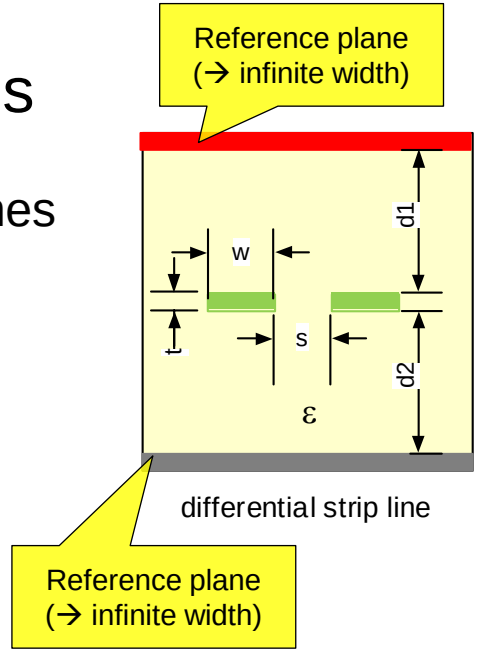
- Non optimal alignment between ground planes and signal lines



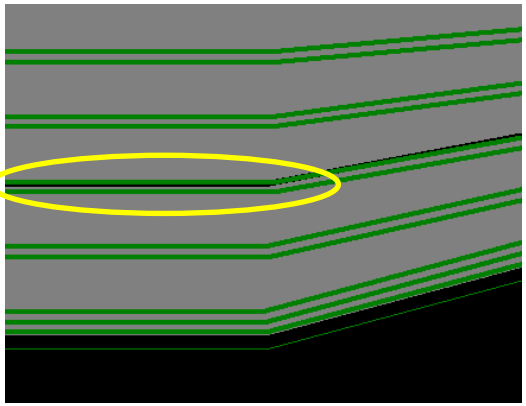
Signal layer vs. layer 4 plane (ok)



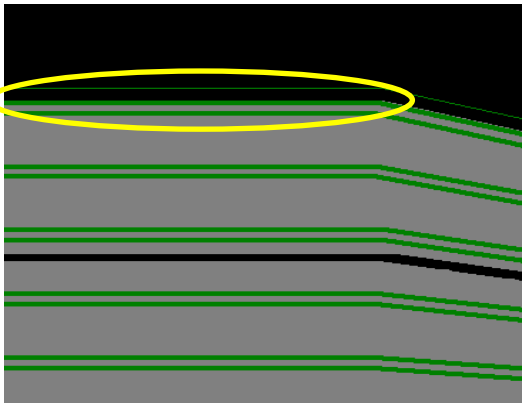
Signal layer vs. layer 2 plane (bad)



- Signal lines too close to the ref. plane edge or split between planes



Diff. pair split between planes (bad)



Diff. pair too close to edge (bad)

Similar details on patch panel and module connector region

Summary

- Taiyo prototypes
  - T1 and T2 samples have very similar electrical properties
  - $Z_0 = 89\Omega$, $R_{DC} = 7.6\Omega$
  - $\varepsilon_r = 3.1$
  - Attenuation @ 800MHz = 5.8dB

- Kaupke prototype
  - $Z_0 = 90\text{-}116\Omega$ (changes along cable), $R_{DC} = 6.8\Omega$
  - $\varepsilon_r = 2.8$
  - Attenuation @ 800MHz = 4.2dB

➔ Kaupke seems to use a different layer stack (cable more rigid and slightly thicker)
  - Less attenuation
  - Higher impedance
  - Lower ε_r

Summary II

- Full cable setup (flex + PP + short TWP + PP + long TWP) needs to be evaluated to assess the overall signal integrity

- High frequency damping (skin effect, dielectric losses)
  - can be partially compensated by pre-emphasis (DHP) and equalization on the receiver side (DHH/FPGA)

- Absolute TML impedance
  - Kapton cable layer stack and line geometry

- Impedance discontinuities (**Pre-emphasis does not compensate this!**)
  - Analyze TDR measurements and check critical PCB layout regions (edges, connectors, vias etc.)