Tests of a Switched Capacitor Array ASIC at 77K

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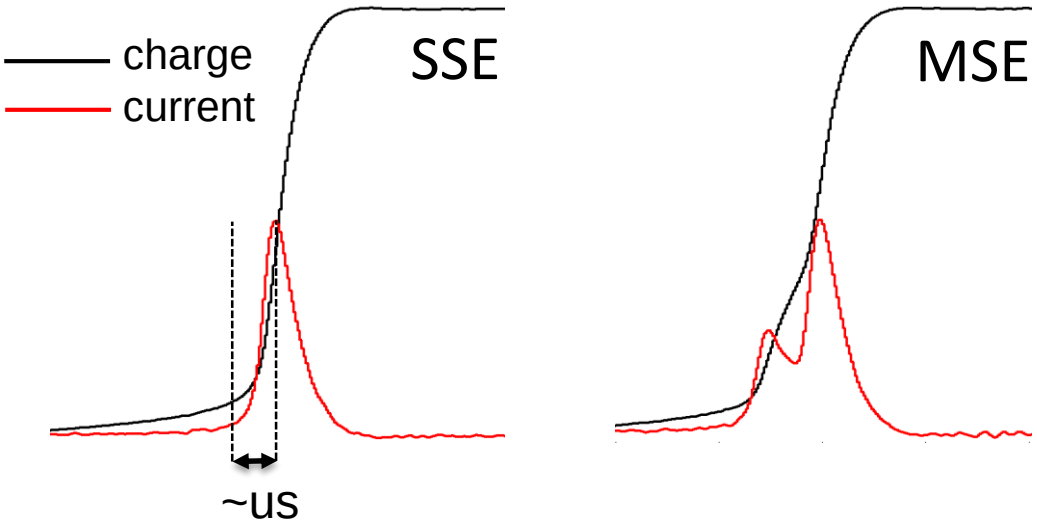
Outlines

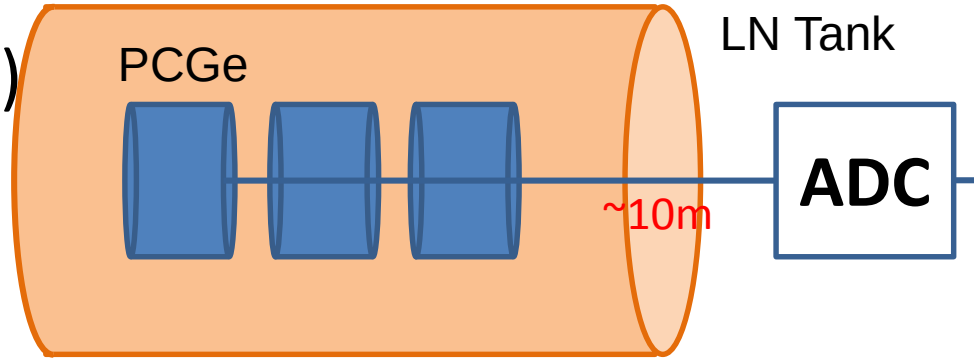
- Introduction
- Readout Architecture
- Test Setup
- Preliminary Test Results
- Summary & Next Step

Introduction

- Experiment need
  - Save the waveform
    - 100M sample rate
  - Distinguish SSE/MSE



- Waveform Scheme Now
  - More long cables (~10m)
    - Hard for Preamp to drive long cable
    - No good for signal to transfer

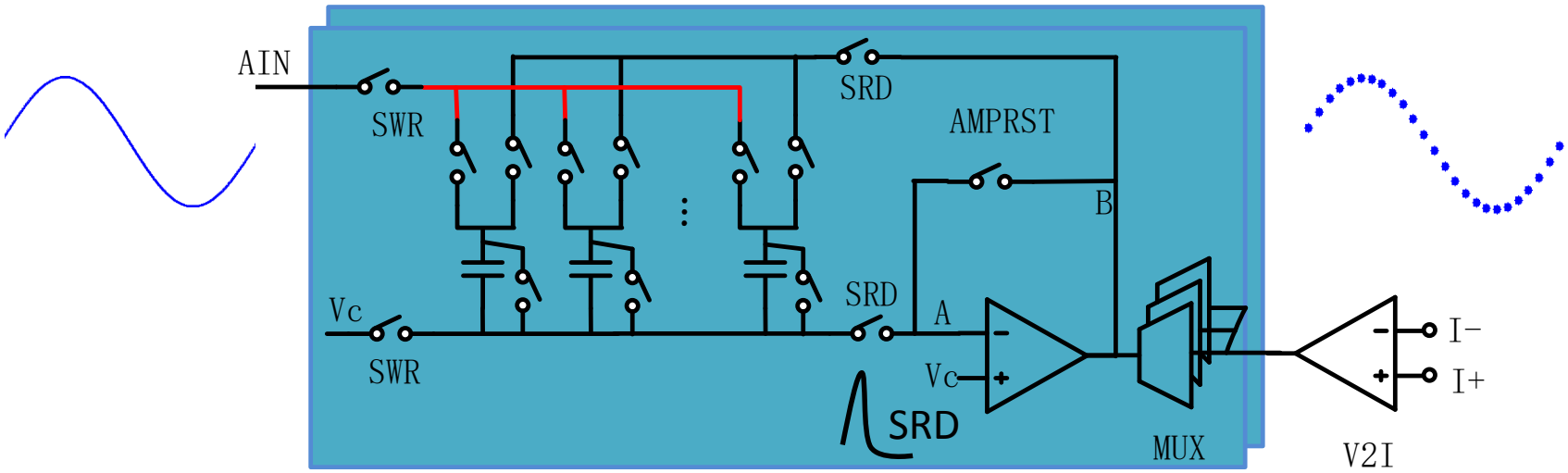


Cryogenic Waveform

- High speed High precision ADC @77K ?
  - NO suitable commercial ADC
    @Cryogenic @100M sample rate
- SCA(Switched Capacitor Array) meets the need
  - Advantage : high channel densities , serial output,
    low power consumption
  - Inferior : sample rate (enough for HPGe @100M)
  - Widely used in High Energy Physical Experiments
    (Gas detector)
- SCA Performance at cryogenic down to 77K?

SCA Principle

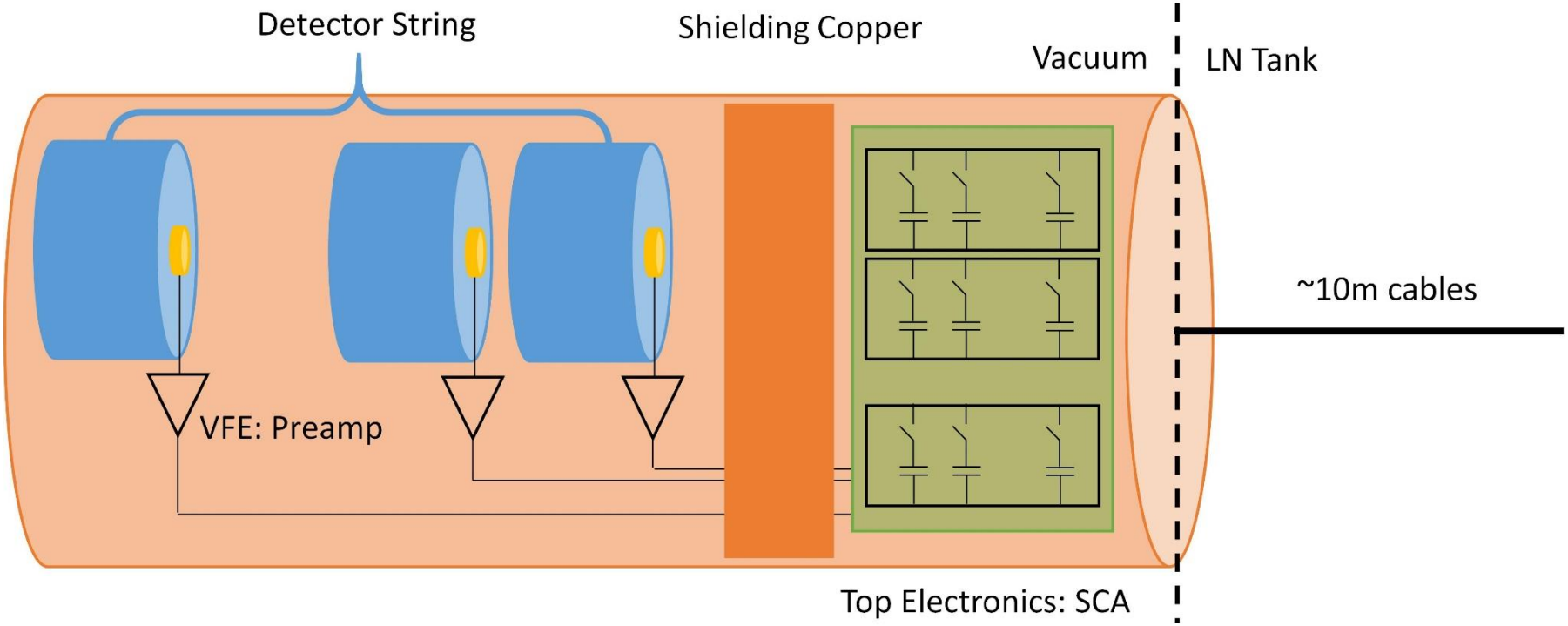
- SCA(Switched Capacitor Array) Diagram



- Sample
  - Capacitor on/off one by one at sample interval
  - Sampling depth : length x interval
- Readout
  - SRD Trigger

Readout Architecture

- Overall readout scheme



VFE:Preamp Prof. Deng has showed

SCA:Switched Capacitor Array

Our SCA Structure

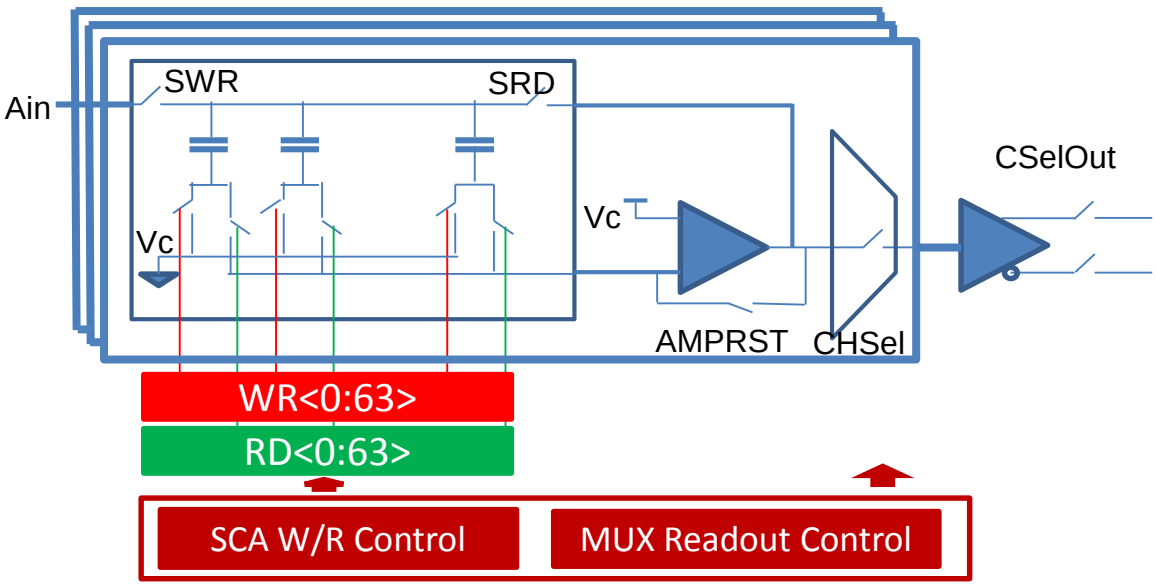
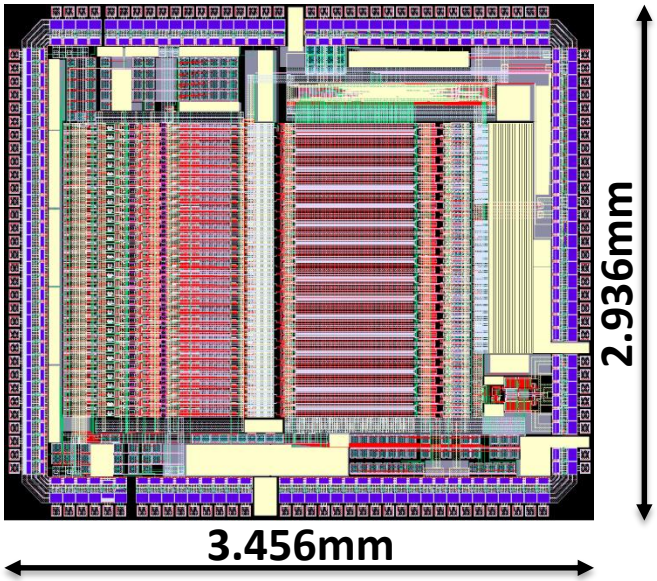
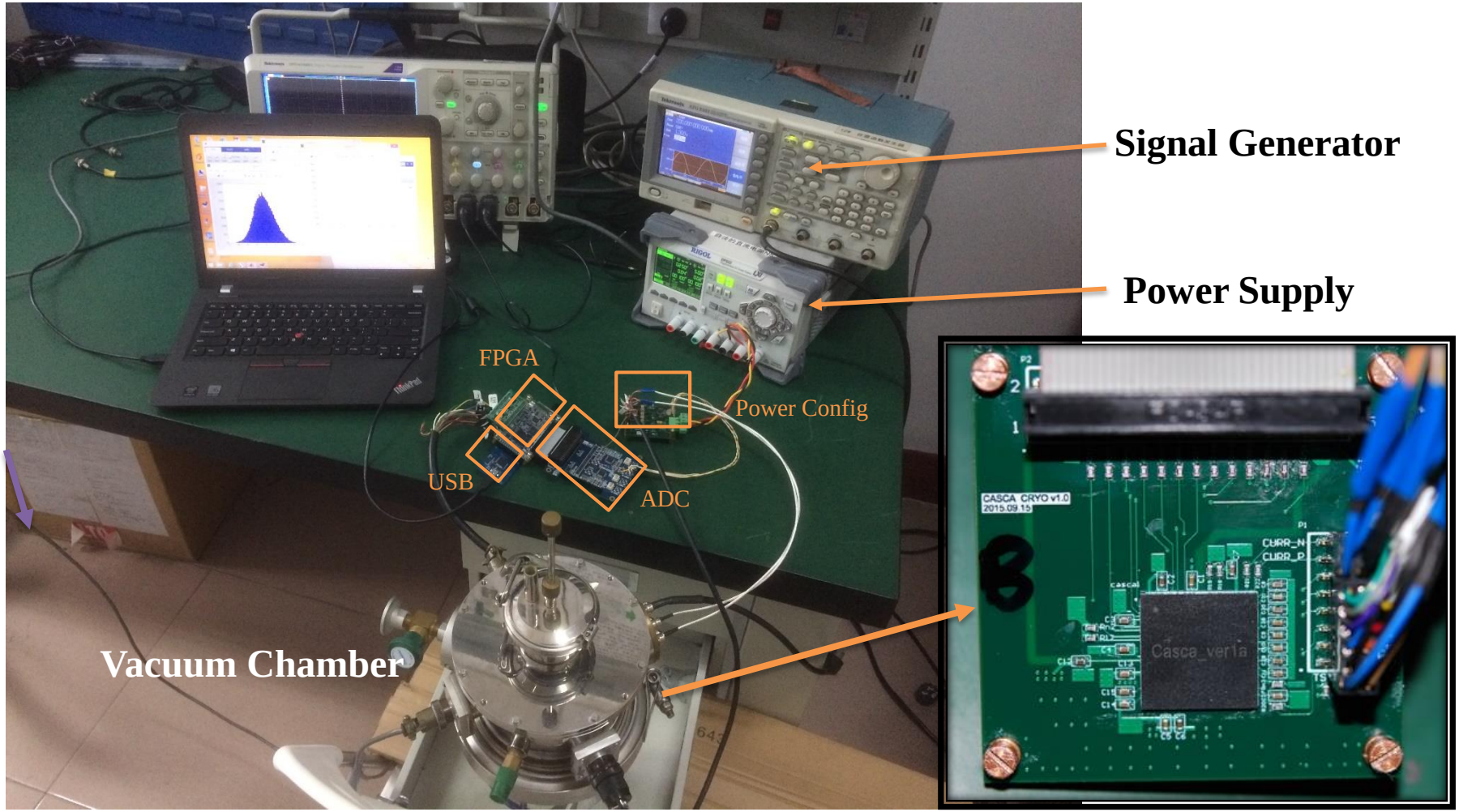


Diagram: Analog output



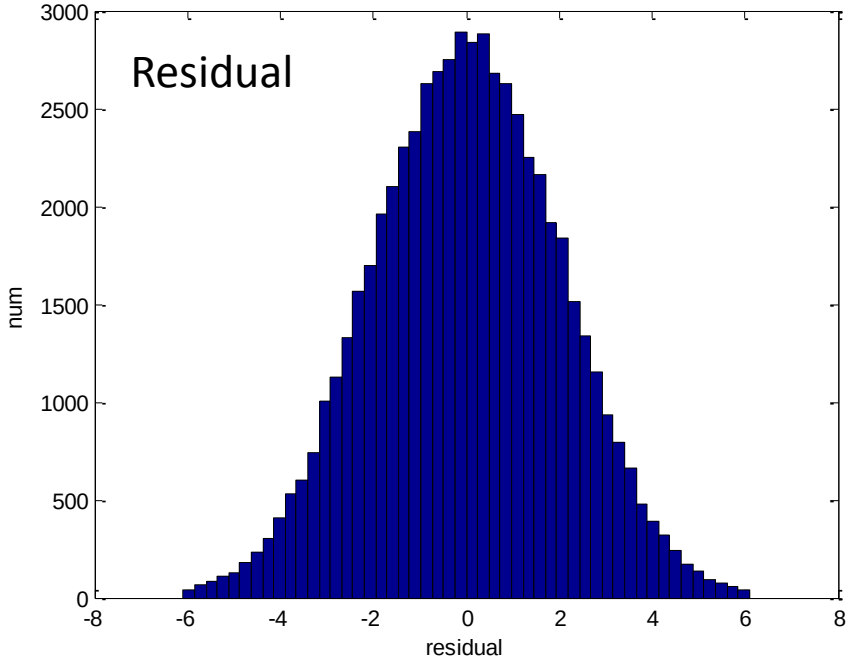
- 64 cell x 32 channel
- Readout resolution: 10bit
- Sampling depth: 1.2 us @50M sample rate
- Process: Charted 0.18um CMOS
- ASIC design has not been optimized for HPGe detector at cryogenic temperature

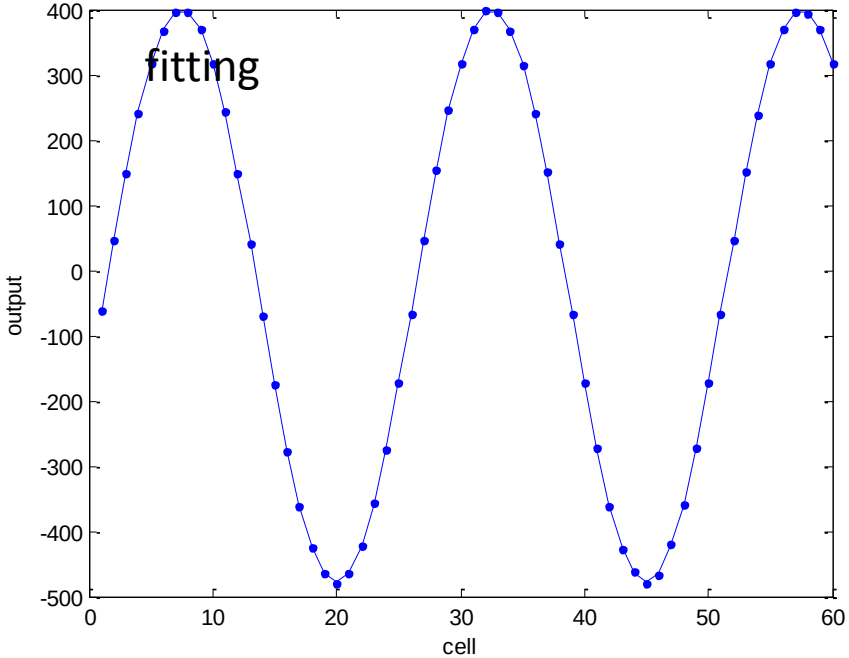
Test Setup


Signal Generator
Power Supply
FPGA
Power Config
USB
ADC
Vacuum Chamber
CASCA CRYO v1.0
2015.09.15
CURR_N
CURR_P
Casca_ver1a

Dynamic Test Scheme

- Sine Input signal :0.3V~1.3V @200KHz





- σ_v

$$\sigma_v = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(Vs_i - Vf_i\right)^2}$$

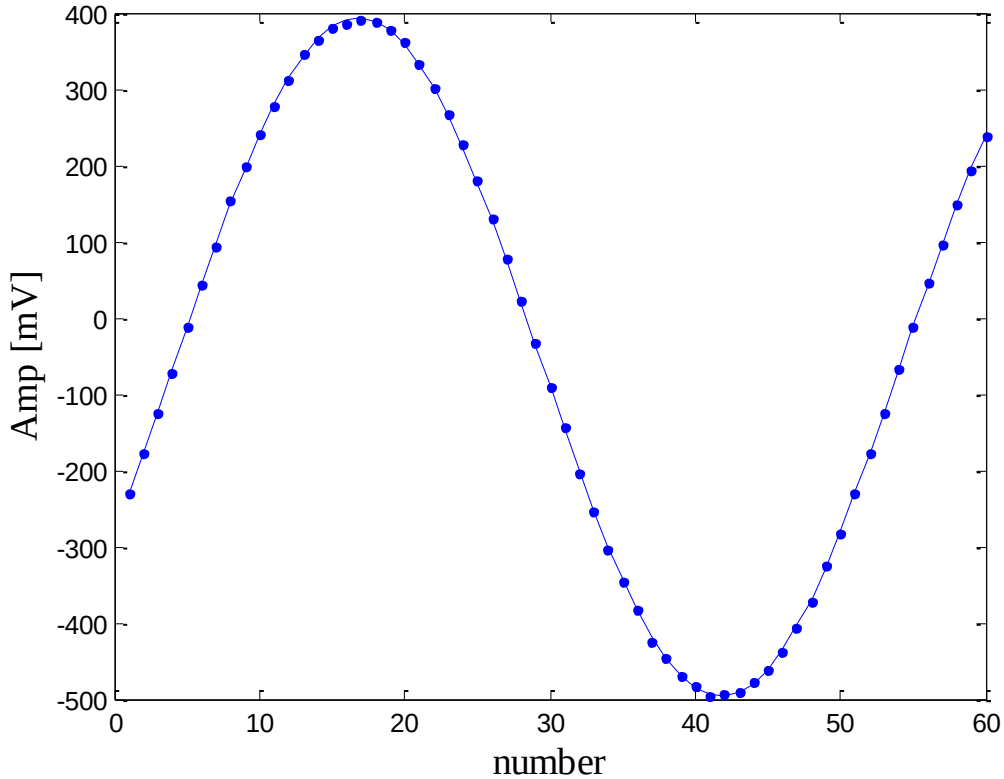
Preliminary Test Results

- Room Temperature Test
  - Input :0.3~1.3V sin.
  - 5.5M readout rate

$$\sigma_v = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(Vs_i - Vf_i\right)^2}$$

σv=2.2mV @25M sample

σv=2.1mV @12.5M sample



Preliminary Test Results

- What will happen at Cryogenic ?
  - Just lower the temperature
  - ➢ It can **work** with larger gain

- σ_v

Sample freq.	Chamber_RT	Cryogenics_18.5uA
25M	2.2mV	3.3mV
12.5M	2.1mV	2.3mV

➢Bias current change from 52uA@300K to 18.5uA@120K
➢Simulation bias current value changed to 11.8uA@120K

Preliminary Test Results

- What will happen at Cryogenic ?
  - Change the bias current to 50uA@120K
    - bias resistor change from 1.4KΩ to 118.2Ω to reach 47.8uA bias current

- σ_v

Sample freq.	Chamber_RT	Cryogenics_18.5uA	Cryogenice_47.8uA
25M	2.2mV	3.2mV	1.9mV
12.5M	2.1mV	2.3mV	1.9mV

Preliminary Test Results

- What will happen at Cryogenic ?
  - Change the bias current to 50uA@120K
    - bias resistor change from 1.4KΩ to 118.2Ω to reach 47.8uA bias current

- σ_v

Sample freq.	Chamber_RT	Cryogenics_18.5uA	Cryogenice_47.8uA
25M	2.2mV	3.2mV	1.9mV
12.5M	2.1mV	2.3mV	1.9mV

Better Performance

Summary & Next Step

- **Summary**
  - Waveform at cryogenic can reduce cables CDEX200 readout scheme
  - SCA Waveform can **work** at Cryogenic with better performance through changing bias current
  - Test condition limits resolution performance
- **Next Step**
  - More detailed test
  - Higher precision SCA design

shorten cable & decrease connectors
better cable for clock
Ability to drive long cable
Temperature