CMOS Preamp Development for PPC HPGe Detector

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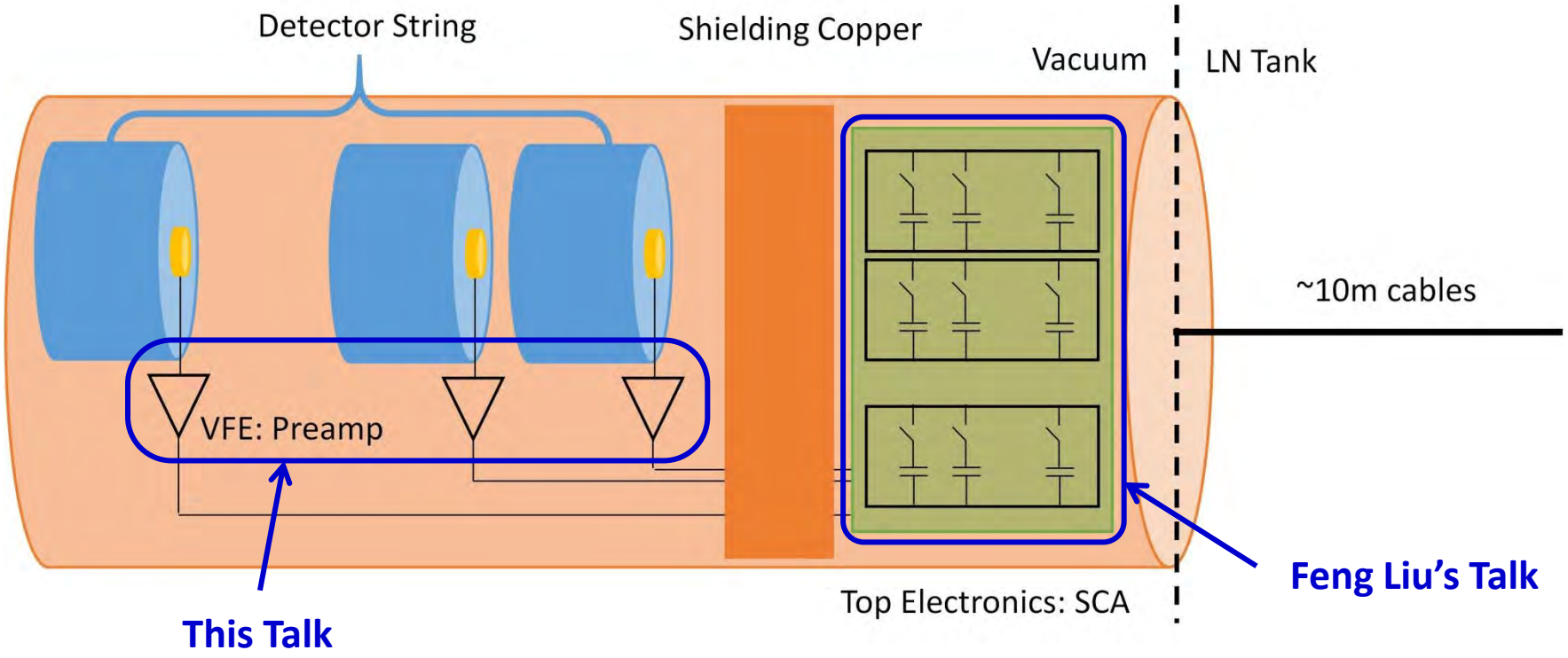
China Jinping Underground Laboratory

Outlines

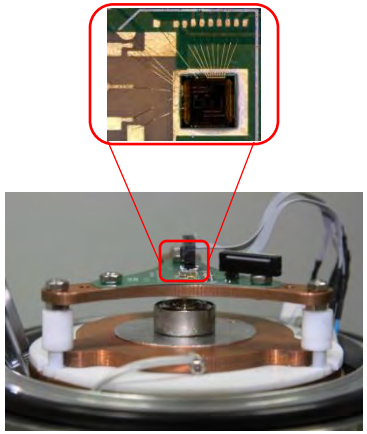
- Introduction
- Circuit Design
- Preliminary Test Results
- Summary

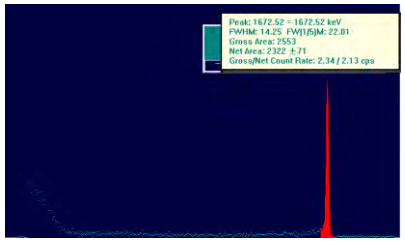
Introduction

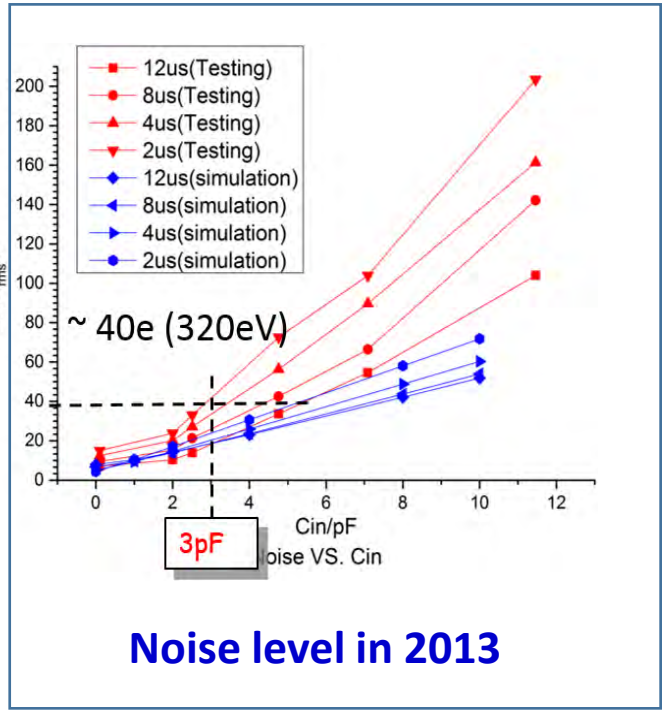
- Possible readout scheme for CDEX-200



- Noise keeps going down in the last years





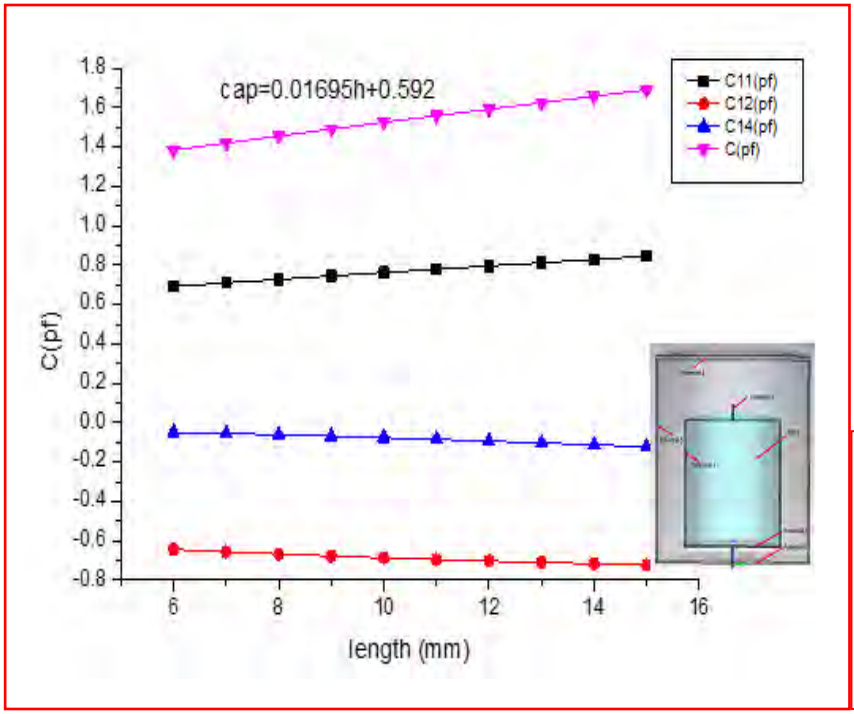


Noise level in 2013

- Best results of ~60eV FWHM noise achieved by JFET preamp for PPC HPGe
- Noise needs to be further reduced by at least 4 times

Towards Sub-10e ENC

- ENC decreases with the input capacitance C_{in}



~0.5pF ~0.1pF

$$C_{in} = C_d + C_{stray} + C_f$$

For a 1kg ppc-HPGe crystal with 0.5mm diameter needle, the connection capacitance is 1.38-1.69pF for 6-15mm length

- With smaller C_{in} …

Without any filtering

Capacitance/Farad	kTC noise/e
1a	0.4
10a	1.26
100a	4
1f	12.6
10f	40
100f	126
1p	400
10p	1260

With optimum filtering

$$ENC_{sw+p,opt}^2 = 16kT\sqrt{\frac{a_1 a_3 \gamma C_{in} \tau_e}{R_p}} \propto \sqrt{C_{in}}$$

$$ENC_{sf,opt}^2 = 4a_2 K_F C_{in}$$

For C_{in}=2pF:
$ENC_{sw+p,opt}$ ~ 5e @ I_D=1pA, T=77K, τ_e=10ps
$ENC_{sf,opt}$ ~ 14e @ K_F=10^{-25}J

- What if C_{in} → 0.1pF?

For C_{in}=0.1pF:
$ENC_{sw+p,opt}$ ~ 2.4e @ I_D=1pA, T=77K, τ_e=10ps
$ENC_{sf,opt}$ ~ 3.1e @ K_F=10^{-25}J

ENC_{total} ~ 4e

HOW?

- Cannot simply reduce the point electrode size
- Pixelating the point contact
- Reducing the interconnection

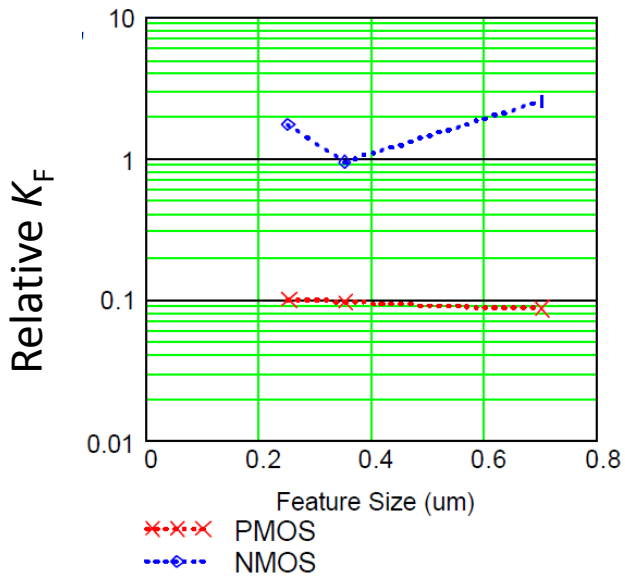
- More advanced CMOS process

$$ENC_{sw+p,opt}^2 = 16kT\sqrt{\frac{a_1 a_3 \gamma C_{in} \tau_e}{R_p}}$$

τ_e decreases with technology generation and hence ENC_{sw} can be reduced with more advanced process

$$ENC_{sf,opt}^2 = 4a_2 K_F C_{in}$$

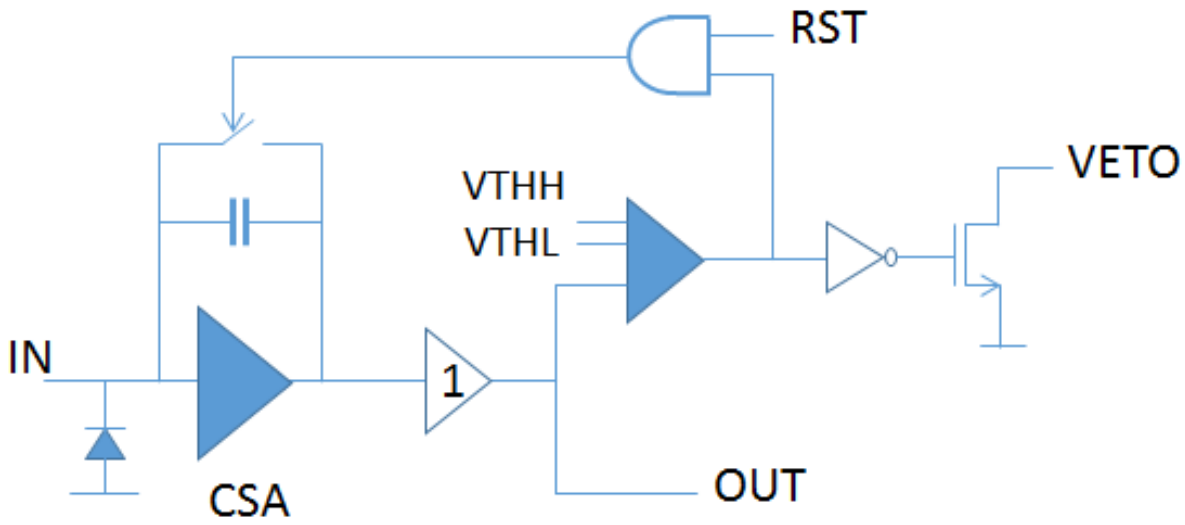
Different story for 1/f noise:
K_F deteriorates with technology generation, especially for PMOS transistor (becoming surface channel device)



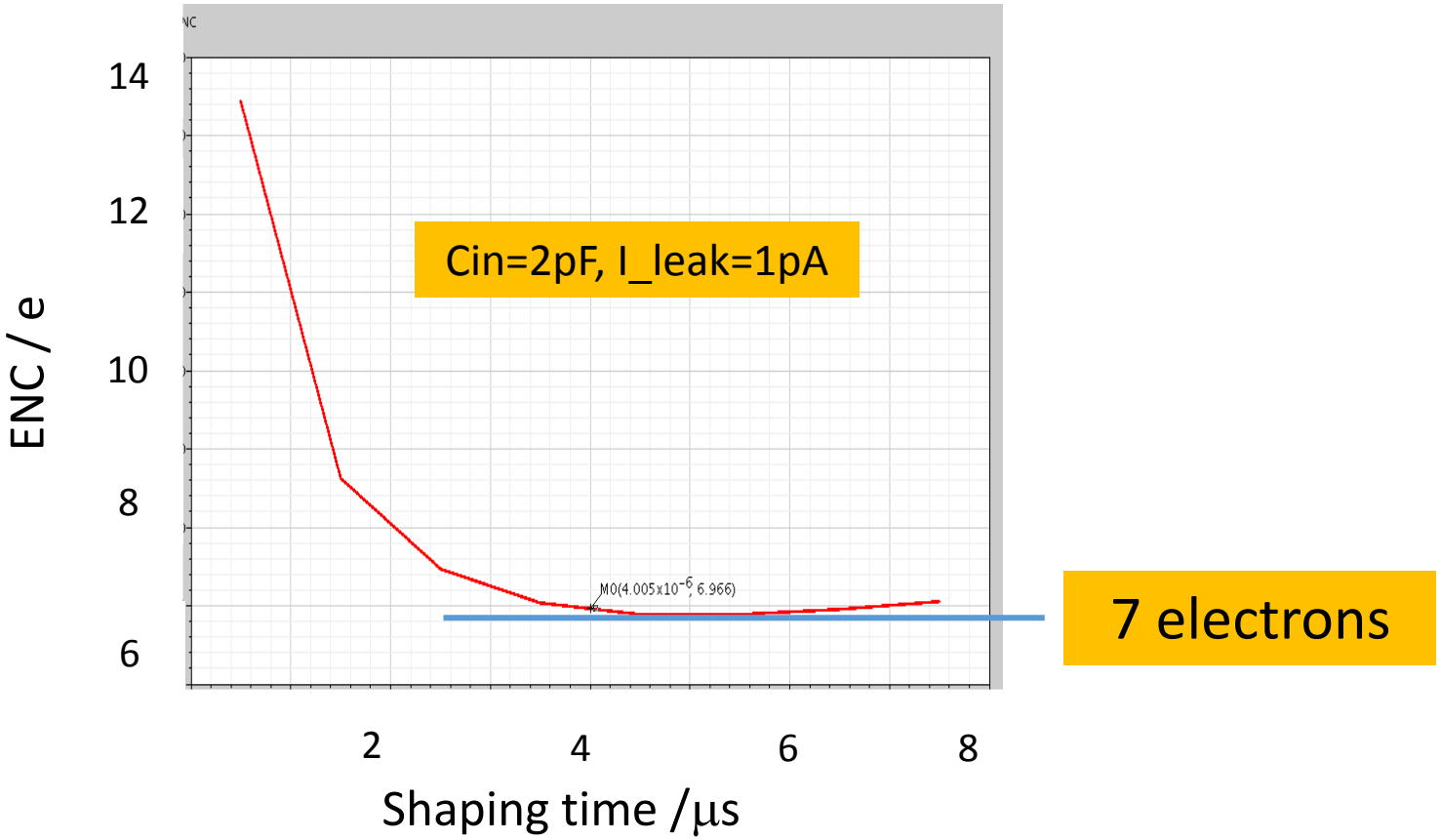
Measured 1/f noise coefficient for several submicron CMOS processes

Circuits Design

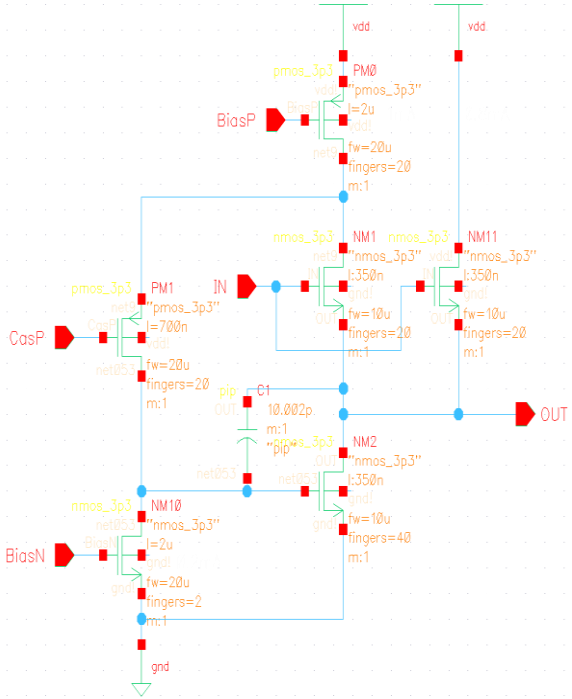
- Architecture

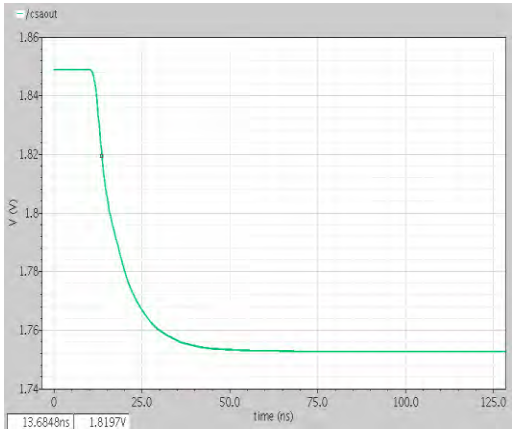


- Noise optimization (simulation results)

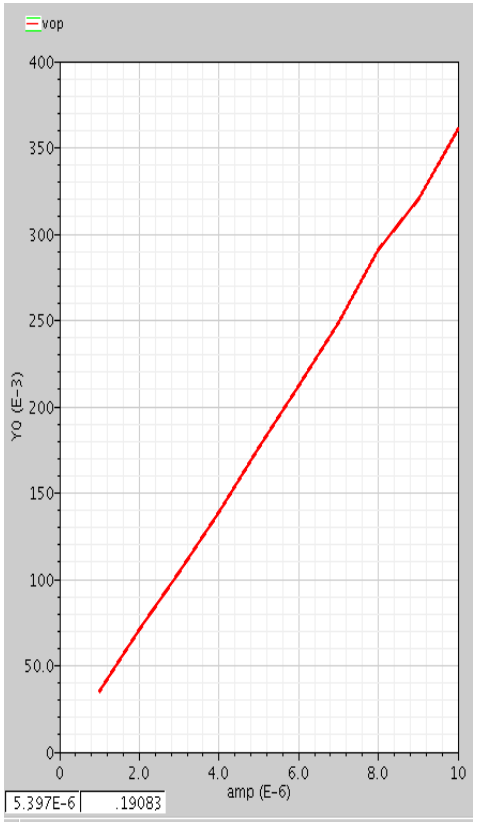


- Output stage





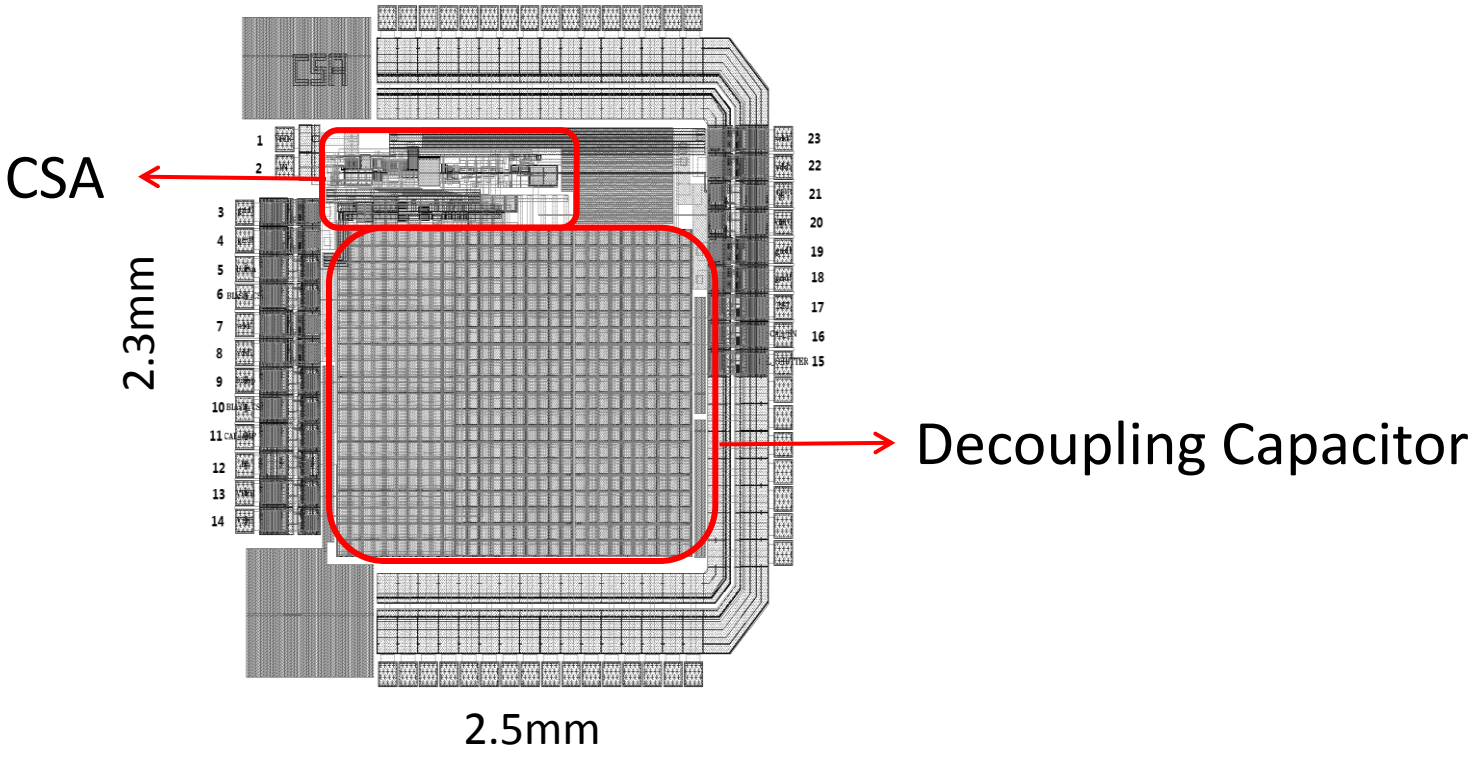
Tr~10ns @ 50Ohm//100p



50Ohm//100pF, 5-50fC input

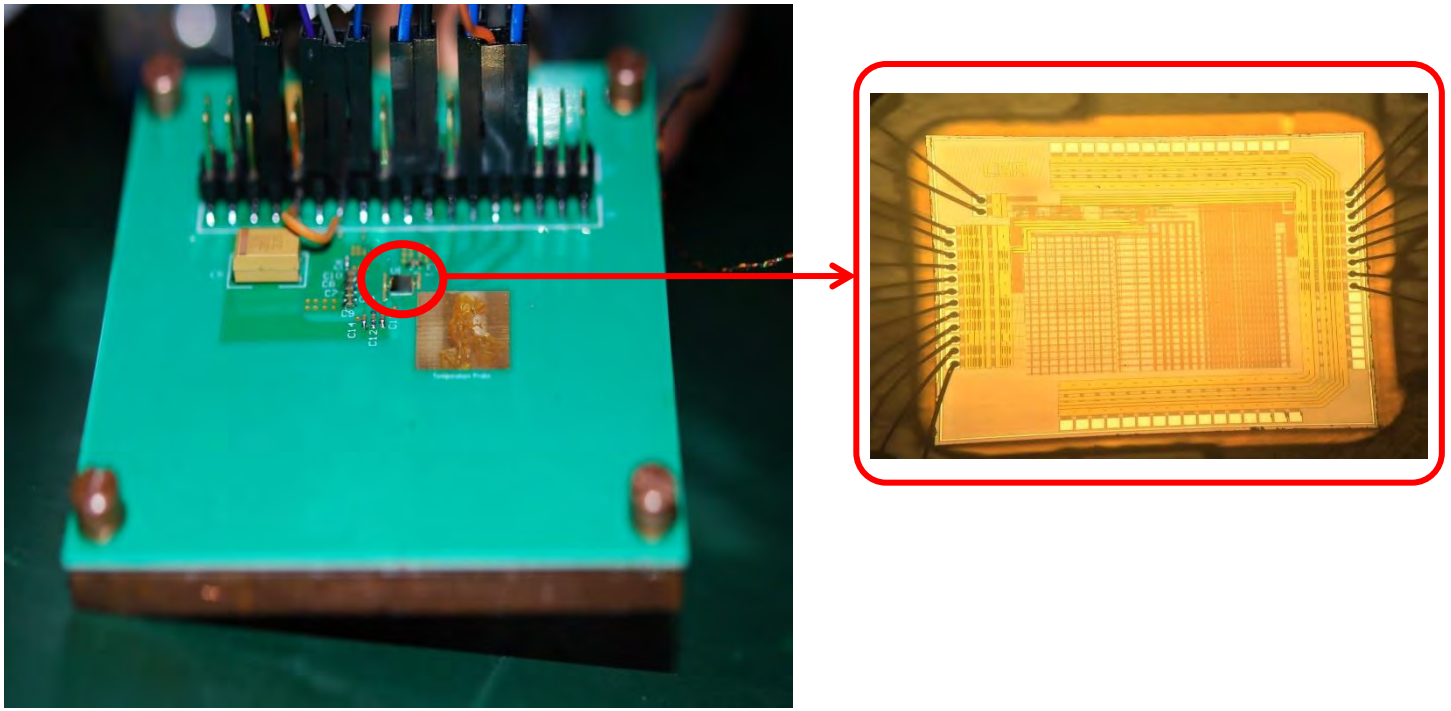
Pullia A, Zocca F. IEEE NSS Conference Record 2009

- Layout with on-chip decoupling



Preliminary Test Results

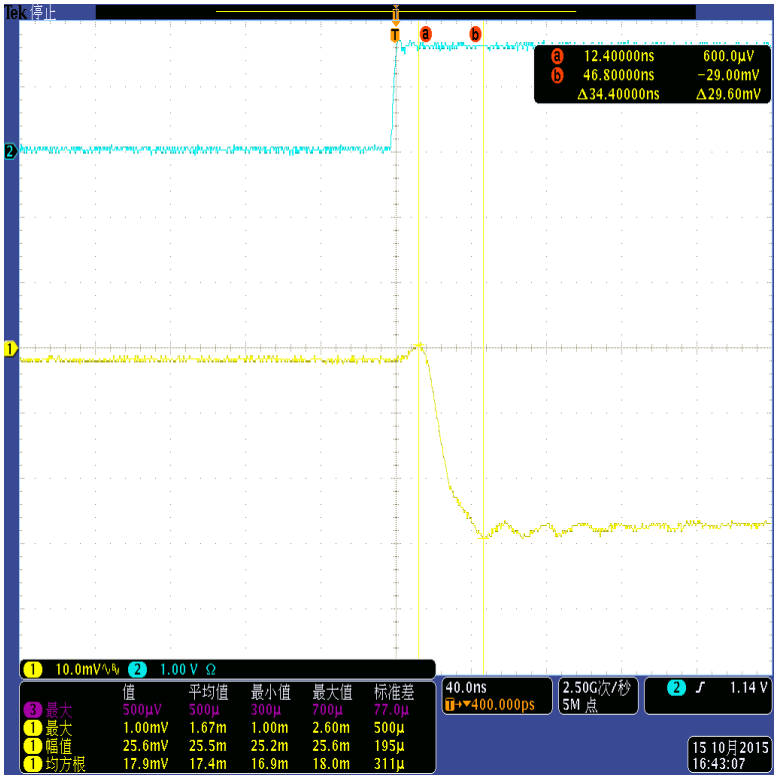
- Setup



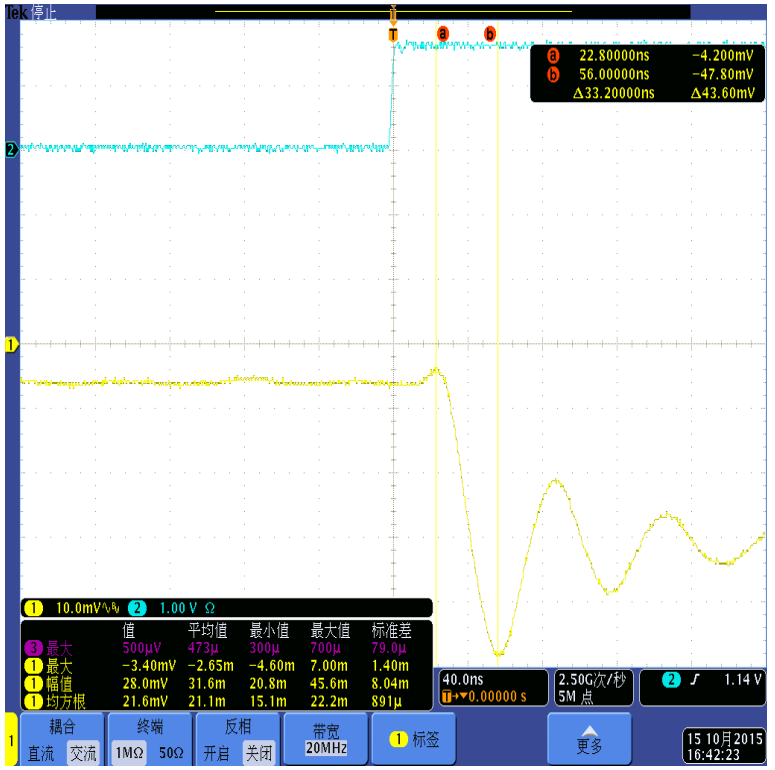
- Basics

Bias = 105uA
Leakage current = 6.9fA @ R.T.

- Rise time



30 cm cable

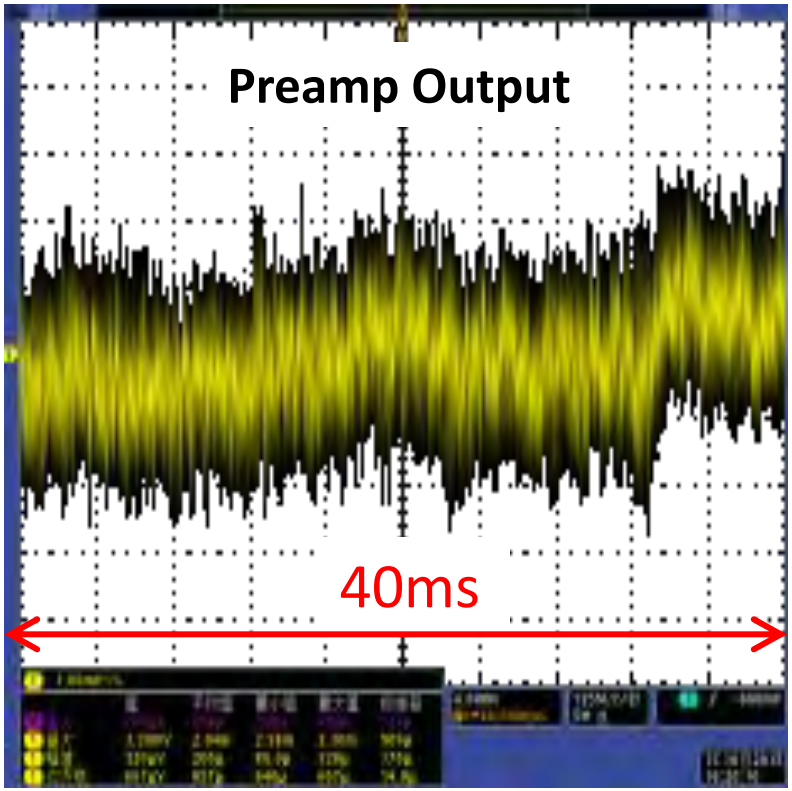


300 cm cable

- Preliminary noise test results

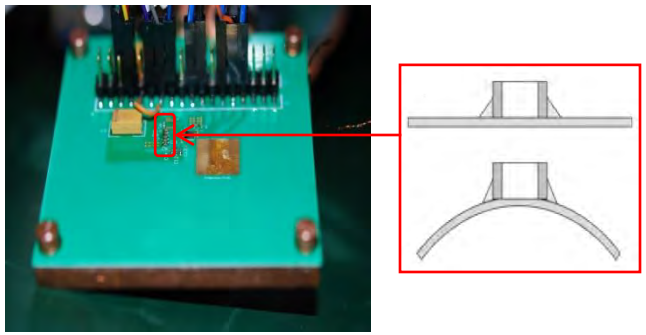
Shaping time (us)	Output(V)	Noise(mV)	ENC(e)
0.5	0.843	3.4	226
2	6.25	24.2	215
8	2.81	17.3	346.5

- Low frequency noise



- After removing some decoupling capacitor

Shaping time (us)	Output(V)	Noise(mV)	ENC(e)
0.5	0.259	1.33	128
2	0.482	2.54	132



Microphonic noise due to the piezoelectric effect of the ceramic capacitor

Summary

- Sub-10e ENC may be achievable by CMOS preamp, even for 1-2pF capacitance detector. It can be further reduced to <5e if we can reduce the input capacitance down to ~0.1pF.
- The new version prototype preamp has been developed and tested. The measured ENC (~130e) was much higher than the simulation results (~7e) and we believe it is most likely due to the PCB design and some passive components.