Belle II PXD ASIC review

The review should assess the production readiness of the three ASICs used in the Belle II PXD. The schedule requires a submission of the final AISCs early 2015. In order to achieve this one has to assess:

* The maturity of the chip design.
* Completeness and quality of documentation.
* Status of performance tests (stand alone and on system level).
* Known problems and mitigation/correction plans.
* Missing measurements and tests.
* Work plan (responsibilities, milestones).
* Schedule for next submission .
* QA strategy.

It is likely that the review will conclude that there as till some issues to be resolved before a submission can be done. In this case the risks for the detector performance need to be evaluated. A clear strategy should be developed how to achieve the goal of timely submission.

Following issues need to be discussed

* General introduction in the chip design and specifications
* Summary of tests and performance information
* Design changes planned for the next submission
* Information on QA strategy (information on yield expectations, test program, status of test equipment

Two full days are foreseen for the review (October 27/28), starting Monday at 10:00 till Tuesday 16:00. The review will take place at MPI für Physik, Munich.

Gary Varner will be internal (Belle II) reviewer. We will try to find external reviewers as well.

It is expected that the reviewers will receive necessary information at least one week ahead of the review: documentation and test results.

Outline of the agenda:

Monday:

Introduction; charge of the review.

Introduction into Belle II PXD, performance requirements and specification.

Switcher (2 talks: Circuit Design & Measurements ).

DCD (3 talks: Circuit Design, Measurements, Plans and QA).

DHPT (3 talks (3 talks: Circuit Design, Measurements, Plans and QA).

System performance (EMCM tests).

Closed session of reviewers.

Tuesday:

Questions and discussions.

Closed session.

First evaluation.

The final report should be ready within a week after the review (at the time of the B2GM)

For the contributions I would ask Hans Krüger to organize the DHPT part, Ivan Peric the DCD and Switcher part and Christian Koffmane the EMCM and Gated Mode contributions.

Please inform me which talks you propose and by whom.