

# ASICs for Belle II DEPFET Pixel Detector

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## I. INTRODUCTION

**D**EPFET pixel modules will be readout in 'rolling shutter mode', which means that the rows (precisely 4-row matrix segments) are selected consecutively and all columns are read out in each readout cycle. Three different ASIC types will be used for the readout.

The SWITCHER steering chips are selecting and clearing the DEPFET 4-row segments by generating their external gate- and clear voltages. The readout of the columns is done by Drain Current Digitizer (DCD) chips, placed at the bottom of each half-module matrix. These chips receive, process and digitize the current signals generated by the DEPFETs of the selected matrix segment. The eight-bit ADC codes are then sent to the Data Handling Processors (DHPs) that perform data processing, compression, buffering and fast serialization.

All the chips will be mounted directly on the detector module using bump-bonding and flip-chip techniques leading to fully-silicon modules.

## II. SWITCHER

The SWITCHER steering chips will be mounted on the about 2 mm-wide, inactive 300  $\mu\text{m}$ -thick edge rim of the DEPFET module. These chips provide fast (10 ns into 50 pF) voltage pulses of up to 20 V-amplitude to activate gate rows and to clear the internal DEPFET gates. SWITCHER is implemented in standard AMS 0.18  $\mu\text{m}$  or 0.35  $\mu\text{m}$  HV technology. One SWITCHER will be able to 'address' 32 different DEPFET matrix segments (row groups), for this purpose it will have 32 'channels' with a clear- and a gate-driver each. One row group is selected by pulling the external gates at a negative voltage which switches the pixels on. Clearing is achieved by pulling the clear diffusion of the selected DEPFETs at a positive voltage. The SWITCHER channels and their drivers are activated consecutively. Readout of one DEPFET half-module with 192 row groups (768 pixel rows) would require six SWITCHERS.

All required SWITCHER control signals and power run on the only 2 mm-wide module rim. The number of I/O signals has therefore been minimized and an unusual bump pad geometry has been chosen to simplify routing on the module - the bump array is placed in the middle of the chip.

In order to simplify system design, the SWITCHERS have a floating digital ground and use fast, low power level shifters. A JTAG interface allows for interconnectivity tests on the module.

The design of the SWITCHER versions optimized for Belle-II requirements (SWITCHERB18 in 0.18  $\mu\text{m}$  and SWITCHERB in 0.35  $\mu\text{m}$ ) has been finished. Both chips have been successfully tested. Radiation hardness of at least 37 MRad has been demonstrated.

## III. DCD

The currents generated by a selected DEPFET row-group are routed out via column lines and readout by the DCD chips placed at the bottom of each half-module matrix. Each DCD has 256 analog inputs. Since one row-group consists of 1024 DEPFET pixels (four rows with 256 pixels each), four DCDs will be needed to readout all the columns in parallel. There will be therefore eight DCD chips on a module. DCD is implemented in UMC 0.18  $\mu\text{m}$  CMOS technology using special radiation hard design techniques. The chip occupies 3.2 mm  $\times$  5 mm area. Chip size and input pitch have been adapted to the specific Belle-II requirements. DCD-B uses bump bonding on the UMC technology provided by EuroPractice.

DCD has 256 analog channels each housing an input stage and two ADCs. The analog input stage performs various tasks. It keeps the column line potential constant (necessary to achieve fast readout), compensates for DEPFET pedestal current variation, amplifies the signal and provides shaping for noise reduction. For these purposes the input stage offers programmable gain and bandwidth, a two-bit DEPFET pedestal current compensation (using digital data from the DHP) and sampling of the pedestal current. The analog signal is digitized using current-mode cyclic ADCs, two of them placed in every channel. A large synthesized digital block decodes and derandomizes the ADC raw data which are then transmitted in a well sorted sequence to the DHP chips using fast parallel 8-bit digital outputs. The digital timing and data protocols have been simplified and adapted for communication with the DHP. Two operation modes using single sampling or double correlated sampling are possible. The baseline is single sampling.

Due to the expected quite significant power dissipation of up to 600 mA per chip, voltage drops on the internal power buses are a significant concern. This has been addressed by various methods like the use of separate power buses for sensitive parts, high power supply rejection and the use of the extra redistribution metallization of the bumping technology for additional power routing.

The DCD chip optimized for Belle-II requirements (DCDB) has been designed and successfully tested. Radiation tolerance of at least 7 MRad has been proven.

Photomicrograph of the DCDB chip that is produced with solder bumps is shown in fig. 1.

## IV. DHP

The DHP chip is introduced on the Belle-II module to reduce the amount of data which must be sent off module via multi Gb/s differential signals. The DHP receives data from the DCDB on 64 single ended digital inputs running at 400

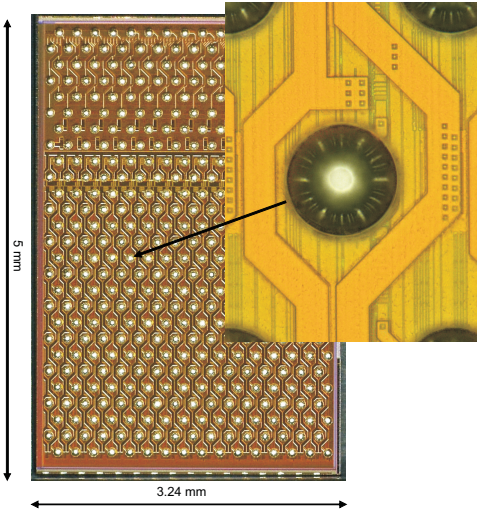


Fig. 1. Photomicrograph of the DCDB.

MHz. This data stream is corrected for common mode and fixed pattern noise. Hit clusters are identified by a thresholding operation and the hit data is sent out serially.

## V. READOUT CYCLE

In this section we will explain the DEPFET readout cycle. The readout cycle starts with the selection of a DEPFET row-segment performed by a SWITCHER chip. The corresponding SWITCHER channel is enabled by setting a single enable bit in the SWITCHER's shift register and by confirming the selection using fast STROBEGATE signal. The SWITCHER control signals are generated by a 'master' DHP. Upon the selection is confirmed, the low-voltage binary signal is translated to a required gate-on voltage that switches the DEPFETs on. The DEPFET currents flow then through the column-lines into the DCDs.

The current receivers in the DCDs are based on the transimpedance amplifiers. They hold the column-line potentials at a constant level (virtual mass) and in this way make the readout speed independent of the large column-line capacitances (around 50 pF). (Since the potentials of the lines are constant, the signal currents flow directly into the DCDs rather than 'fill' the large line capacitances.) The current receivers can also amplify the current signals and act as low-pass filters to reduce the noise. The amplified and shaped signals are then processed by the current-mode cyclic ADCs; two of them are placed in each DCD channel to achieve the necessary sampling frequency of at least 10 MSamples/s. The shaping time and the gain of the current receivers are programmable, a larger shaping time leads to a better S/N and a lower readout speed. Larger gain leads to an increased S/N and a decreased input-signal dynamic range.

Although DCD is able to support, both, double- and single sampling, we will for the moment assume the later. In the case of single sampling, the formerly stored pedestals are subtracted in the readout chip.

If no variable pedestal correction is applied in the DCD, the input-signal dynamic range must be large enough to cope with the pedestal dispersion. (Typical particle signals are significantly lower than the pedestal dispersion. The constant part of the pedestals can be easily compensated by subtracting an offset current from the input signal.) For the case of an excessive pedestal dispersion, the DCD has a two-bit DEPFET pedestal current compensation in every channel. The required two-bit pedestal values for every DEPFET pixel are previously measured, stored in DHPs and continuously transmitted to DCDs. Using the pedestal compensation, the DCD dynamic range can be increase by roughly factor of four.

The use of two-bit pedestal correction in the DCD will not be enough to reduce the remaining part of the pedestal dispersion to a level that allows an effective signal recognition and zero suppression. For this reason, an additional pedestal current compensation will be performed in the DHP on the digital codes received from DCD. DHP will also calculate the average of the signals received from every DEPFET row-segment and subtract this average part from the signals itself and in this way compensate for any average-signal ('common mode') fluctuation.

The final DCD prototype can optionally perform such common mode correction in its analog front end. The analog common correction can cope with common mode fluctuations that are by far higher than the ADC range.

## VI. DCD - DETAILED

The overall chip architecture is shown in fig. 2. The chip contains the following main blocks: 256 analog channels with signal receivers and ADCs.

### A. Digital Block

Fully synthesized digital readout- and control block that performs randomizing and compression of the ADC codes and contains JTAG interface for accessing the configuration shift registers. Global configuration block that contains two configuration shift registers and the DACs for bias voltages. Pad frame that contains digital input- and output pads.

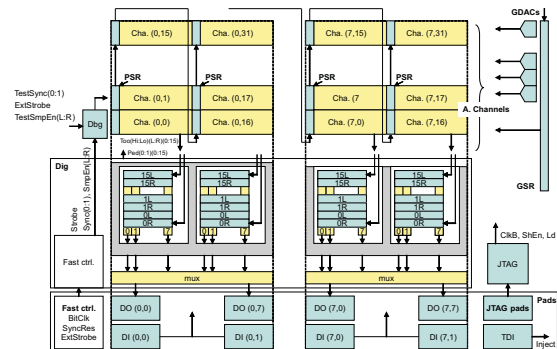


Fig. 2. The chip architecture.

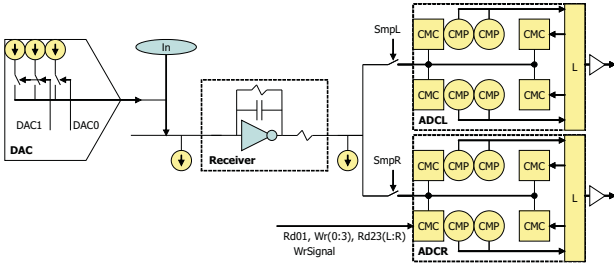


Fig. 3. Block diagram of the DCDB analog channel.

### B. Analog Channel

The block diagram of the analog channel is shown in fig. 3. The main circuits of the block are:

Current-receiver based on a trans-impedance amplifier with a "bleeding resistor" on its output that amplifies the DEPFET current. Two current-mode cyclic ADCs (ADCR and ADCL) based on current-memory cells (CMC). Two-bit DAC for pedestal correction. Decoder for generating of the control signals for the ADC.

1) *Signal Receiver*: The schematic of the current-receiver is shown in fig. 4. The heart of the block is a trans-impedance amplifier (amplifier A with feedback resistors  $R_f$ ) that receives DEPFET current  $I_{in}$  and converts it into voltage  $V_{out}$ . A "bleeding resistor"  $R_s$  is connected between  $V_{out}$  and the input of the ADC. Since the ADC holds its input at a constant potential, the current flowing into the ADC is proportional to  $I_{in}$  with the current gain  $G = R_f/R_s$ . Clearly, if  $R_s$  has a smaller resistance than  $R_f$ , current gain  $G$  will be higher than 1.

The settling time of the current receiver ( $T$ ) can be adjusted by changing  $R_f$  and  $C_f$  values. It holds  $T = C_f \times R_f$ .

As already mentioned the amplifier can operate in the mode to suppress common mode variations and amplify only the difference from the common mode signal. For this purpose transistors TCM1 and TCM2 are used to regulate voltages at nodes in and out. Nodes CM1, CM2 and AmpLow are connected from channel to channel. More details will be presented in a separated paper.

Novel voltage-drop insensitive current sources with enclosed NMOS transistors have been used for sensible currents like ISF in fig. 4.

2) *ADC*: Beside the current-receiver, a channel contains two cyclic- current-mode ADCs that take samples alternately. The ADCs employ redundant signed-digit (RSD) cyclic conversion. The algorithm involves following operations: Subtraction of reference signal, multiplication by two and comparison with a threshold. These operations are usually implemented in analog way using switched-capacitor amplifiers. We have decided to use current-mode memory cells instead from the following reasons. Current-mode cells do not rely on good matching between capacitors and do not need floating switches. This allows smaller layout and use of only-PMOS switches which ensures higher radiation tolerance.

The (RSD) cyclic conversion is based on the division principle (Formally said, the input signal is divided by a reference

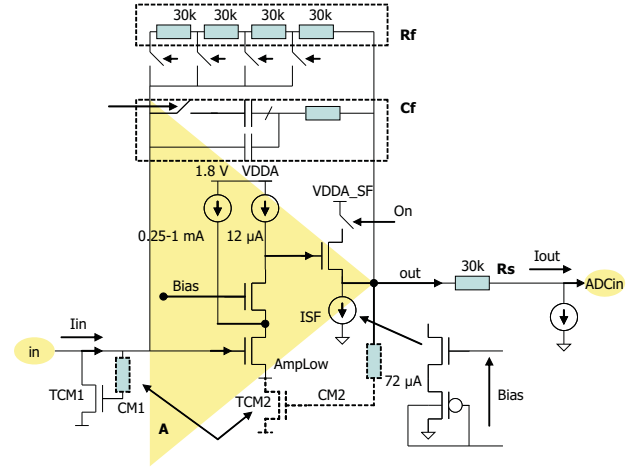


Fig. 4. Schematics of the current-receiver.

value) developed by Sweeney, Robertson, and Tocher also referred to as SRT division [3], [4]. The algorithm starts with the comparison of the input signal with two thresholds, one positive and one negative. If the input signal is larger than the positive threshold, the pair of output code bits is set to 10, meaning +1, and a reference current is subtracted. If the input signal is lower than the negative threshold, the output code is set to 01 (-1) and the reference is added. If the input signal value is between the thresholds, the bits are set to 00 (0) and no arithmetical operation is carried out. The residue signal is multiplied by two and the result undergoes the same operation for the next bits. It is interesting to note that the conversion is not influenced by the comparator offsets, providing the offsets are not larger than half of the threshold.

Current-mode memory cells are used in analog signal processing (such as the cyclic A/D conversion) to memorize and copy currents, they can serve as a good alternative to more complex switched-capacitor circuits.

The block diagram of the current-mode memory cell is shown in fig. 5.

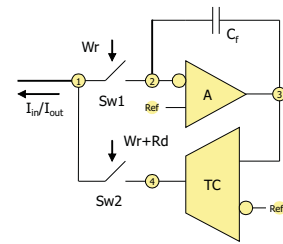


Fig. 5. Current memory cell.

Capacitor  $C_f$  is used as the memory element. Transconductor TC is employed to convert the voltage across  $C_f$  into current. Switch Sw1 is used to freeze the voltage across  $C_f$ . Switch Sw2 is used to disconnect TC from the input when necessary.

In the following analysis we assume that A has infinite gain and no offset.

In write state, Sw1 and Sw2 are closed. There is a negative

feedback generated by A and TC. Potentials  $V_1$  and  $V_2$  are constant, signal independent, and equal to  $V_{ref}$ :  $V_1 = V_2 = V_{ref}$ . In the presence of input current,  $V_3$  takes the value for which TC can drain the input current completely, so that no current flows into  $C_f$ .

Upon opening Sw1, the voltage across  $C_f$  remains frozen.

In read state, Sw1 is opened and Sw2 is closed. The copy of the input current  $I_{in}$  flows out then of the cell.

The memory cell is explained in [1]

Current-mode Realisation of the cyclic ADC

The block diagram of the ADC is shown in fig. 6.

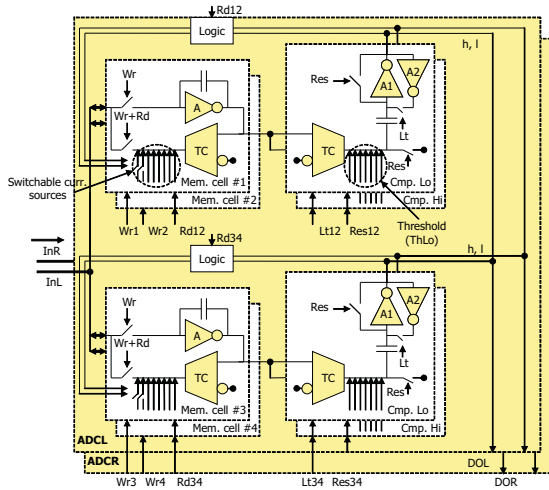


Fig. 6. The block diagram of the ADC.

The ADC consists of 4 current-memory cells (Memory cell 1 - 4) and two blocks with two comparators each (Comp Lo and Comp Hi). The first comparator block is connected to the voltage output (node 3 in fig. 5) of the first memory cell. The second comparator block is connected to the voltage output of the third memory cell. Cells 2 and 4 do not drive comparators. All memory cells have additional switchable current sources that can be used to add or to subtract the reference current.

The A/D conversion is performed in the following way:

State 1: The input signal is written in cell 1. The comparators connected to this cell are in reset state.

State 2: The input signal is written in cell 2. The comparators connected to cell 1 are in compare state.

State 3: Comparators connected to cell 1 are latched, cells 1 and 2 are read out. Results of comparison ( $h, l$ ) are used to decide about adding, subtracting or disabling the switchable reference sources in cells 1 and 2, according to the cyclic conversion algorithm. The residue currents flowing out of the cells have half of the full signal range provided the input signal is within  $\pm 2R$  ( $R$  is the reference current) as shown in fig. 5. Hence the residuals can be summed and the sum fits into cell 3. Since residue currents are equal, the summing is equivalent to multiplication by two. Cell 3 is in write state, the comparators connected to this cell are in reset state.

State 4: Sum of the residue currents is stored in cell 4. The comparators connected to cell 3 are in compare state.

From now on, states 1 - 4 repeat with the difference that the sum of the residue currents flowing out of cells 3 and 4 is written into cells 1 and 2 and not the input signal. The comparators generate one digital output-pair ( $h_i, l_i$ ) in every second state.

To evaluate final conversion result  $D$ , bit streams  $h_i$  and  $l_i$  must be subtracted:

$$D = 2^7(h_7 - l_7) + \dots + 2^0(h_0 - l_0).$$

This is done in the digital readout block placed on the bottom of the chip.

In this way an 8-cycle quantization of the input signal gives as result a discrete number  $D \times R/128$ , where  $D$  takes all integer values between  $-255$  and  $255$ ; in other words,  $D$  is the 8+1-bit binary representation of the analog input  $S$ . To simplify the digital data transfer, we neglect the LSB of  $D$  and transmit only 8-bit digital codes.

Fig. 7 shows the detailed transistor-level schematic of the used ADC- current-mode memory cell. For explanations see [1]. Fig. 8 shows the detailed transistor-level schematic of the comparator.

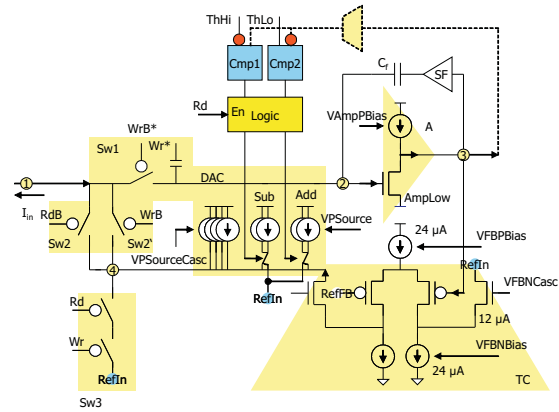


Fig. 7. Transistor-level schematic of the current-memory cell used in the ADC.

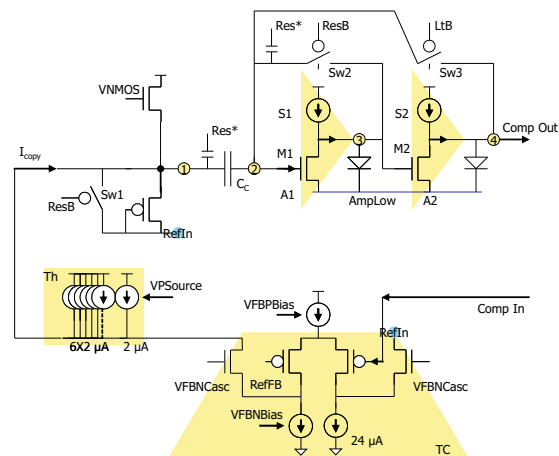


Fig. 8. Transistor-level schematic of the comparator used in the ADC.



## VII. SWITCHERB - DETAILED

The SWITCHERB steering chips will be mounted on the longer edge rim of the DEPFET module, the so called balcony. These chips are able to generate fast (10 ns into 70 pF) voltage pulses of up to 50 V amplitude to activate DEPFET rows and to clear signal charges. Two variants of SWITCHERB chip have been implemented in two HV CMOS technologies, 0.18  $\mu\text{m}$  and 0.35  $\mu\text{m}$  AMS. Readout of one DEPFET half-module with 768 pixel rows will require six SWITCHERBs, each with 32 channels.

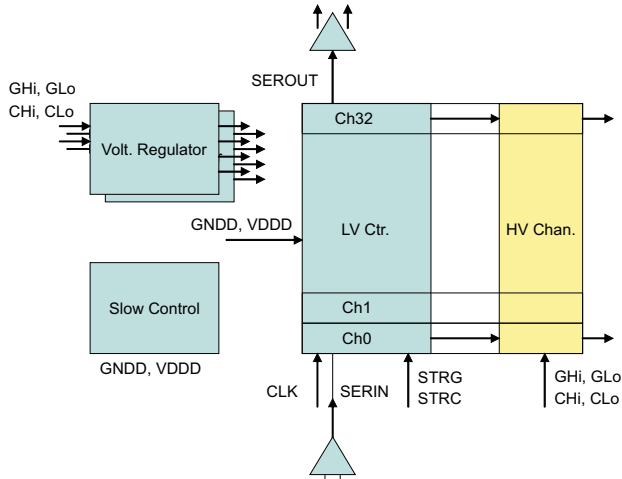


Fig. 9. Block diagram of SWITCHERB chip.

The block diagram of the chip is shown in fig. 9. The basic blocks are:

- 32 high-voltage channels (level shifters) that generate each two high-voltage signals. These blocks implement fast high-voltage output drivers. Static current consumption in idle state is several  $\mu\text{A}$ .
- Low-voltage control block (based on shift register) used to select the high-voltage channels.
- Voltage regulators (two per chip) each generating 4 auxiliary high-voltage supplies out of four externally generated main supply voltages.
- Slow control block based on JTAG.

The outputs of high-voltage channels switch between upper (CHI, GHI) and lower voltages (CLO, GLO), respectively. The voltage swing can be up to 50 V for SWITCHERB in 0.35  $\mu\text{m}$  and 20 V SWITCHERB in 0.18  $\mu\text{m}$  technology. The low-voltage control block and the slow control part are supplied by an additional "floating" 1.8 or 3.3 V supply (GNDD, VDDD). Channels are activated one after other by means of a shift register which a part of low-voltage control. It is fed with a single "1" externally through its serial input. This "1" is clocked through the channels. The high-voltage drivers are activated for the selected channel by fast STROBE signals. Several chips can be daisy chained by connecting the serial output to the serial input of the next chip. The chip is bump bonded to the sensor. Fast timing is provided by a few differential control signals.

Photomicrographs of two SWITCHERB versions are shown in fig. 10. As we can see SWITCHERB in 0.18  $\mu\text{m}$  technology is significantly smaller. Other advantages of this version are faster switching, lower power consumption and higher radiation tolerance.

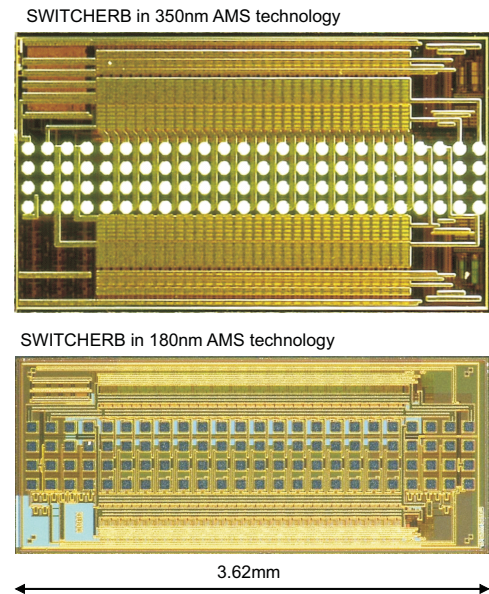


Fig. 10. Photomicrograph two SWITCHERB versions. Upper picture shows the chip implemented in 0.35  $\mu\text{m}$  AMS technology, lower picture shows the chip in 0.18  $\mu\text{m}$  technology.

### A. High-Voltage Channel

The block diagram of a high-voltage channel is shown in fig. 11

Each channel contains a digital low-voltage control block (LV ctrl.), a CMOS-to-differential-current convertor (C), two high-voltage MOSFETs (Tn and Tp) with their gate drivers.

The block diagram of a high-voltage switch is shown in fig. 11.

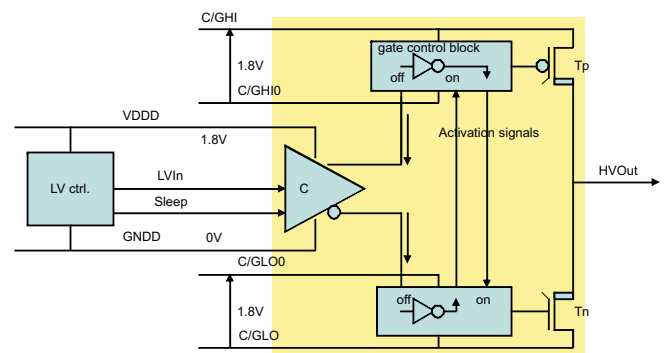


Fig. 11. The block diagram of a high-voltage channel.

The CMOS-to-differential convertor - C uses the 'floating' 1.8V supply and receives two input signals, Sleep and LVIn from LV control.



do not switch between states, only a small current is enough to assure that internal voltages are well-defined.

The digital control block receives clear and gate strobes - StrClr and StrGate, and the shift clock - CLK. The block generates signal Sleep that puts the HV switch into standby mode and GateOn and ClearOn signals that are used to activate the HV switches. The implemented logic allows skipping of channels and overlapping of active GateOn signals in consecutive channels.

The schematic of the digital LV-control block is shown in fig. 13.

The waveform diagram of the most important signals is also shown.

StrGate signal is used to activate the channel that is currently being selected by the shift register. If StrGate is not issued between two CLK signals, one channel will be skipped. GateOn is activated at the leading StrGate edge and deactivated either at the next leading StrGate edge or at the falling CLK edge, see fig. 13. If the falling CLK edge occurs after the leading StrGate edge, the next channel will be activated (by its GateOn) before the previous is deactivated. The overlap time is equal to the skew between falling CLK edge and leading StrGate edge.

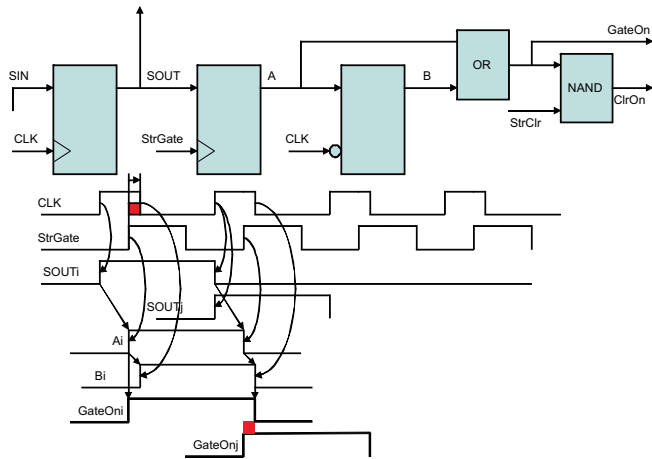


Fig. 13. Schematic of the digital LV-control block and waveform diagram of the most important signals.

### B. DHP - Detailed

## VIII. EXPERIMENTAL RESULTS WITH DCD AND SWITCHER

In order to test the ASICs with attached small DEPFET prototype sensors, we have developed both standard- and modular PCB systems. In the case of the modular system, DCD, SWITCHER and the DEPFET prototype sensor are mounted on separated small PCBs. These PCBs can be connected to a "mother-board" PCB using 100-pin connectors. The photograph of the PCB system is in fig. ?? . Since DCDB and SWITCEHRB are produced only with bump-bonds, silicon adapters are used to allow-wire bonding to PCBs. These adapters are produced at MPI, Munich. The ASICs are bump-bonded to adapters using

gold studs. We present here preliminary results. Average DCDB input-referred noise on the modular system is 60nA. Average peak to peak nonlinearity is 200 nA.

We have also tested a DCD on an single PCB hybrid board, with a thinned DEPFET matrix attached to the ASIC. We measure an average noise of only 35 nA, which corresponds to less then 100 e. Assuming a realistic DEPFET signal of 5000 e, we expect SNR of 50. SWITCHER chips have been extensively tested as well. We have irradiated the chips up to 30 MRad. More results will be presented in a separated paper.

## IX. EXPERIMENTAL RESULTS WITH DHP REFERENCES

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