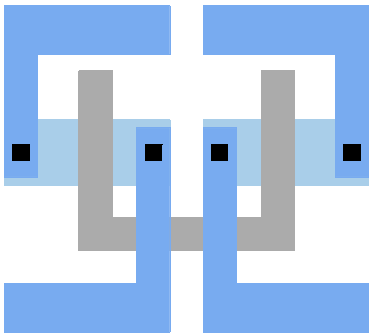
UNIVERSITÄT
HEIDELBERG

Switcher Tests



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Chip Review Meeting

Munich

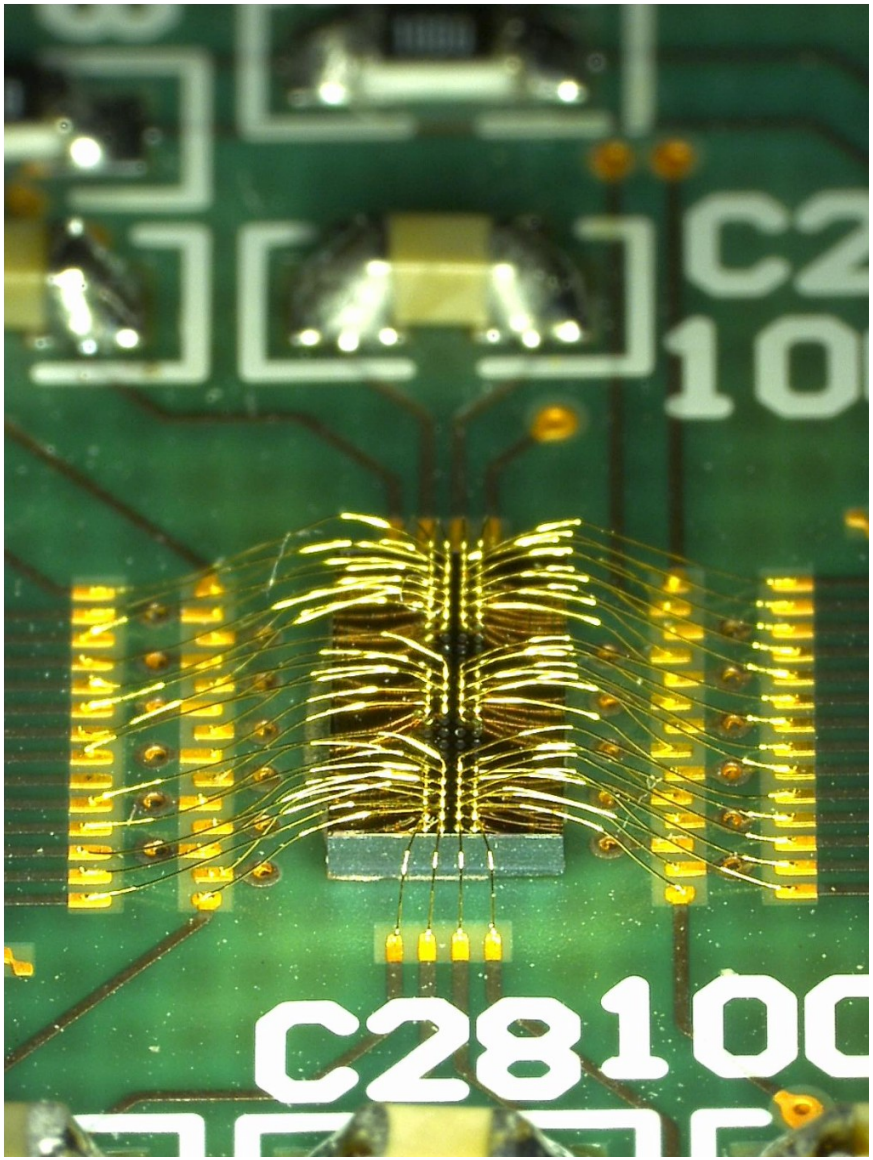
27./28.10.2014

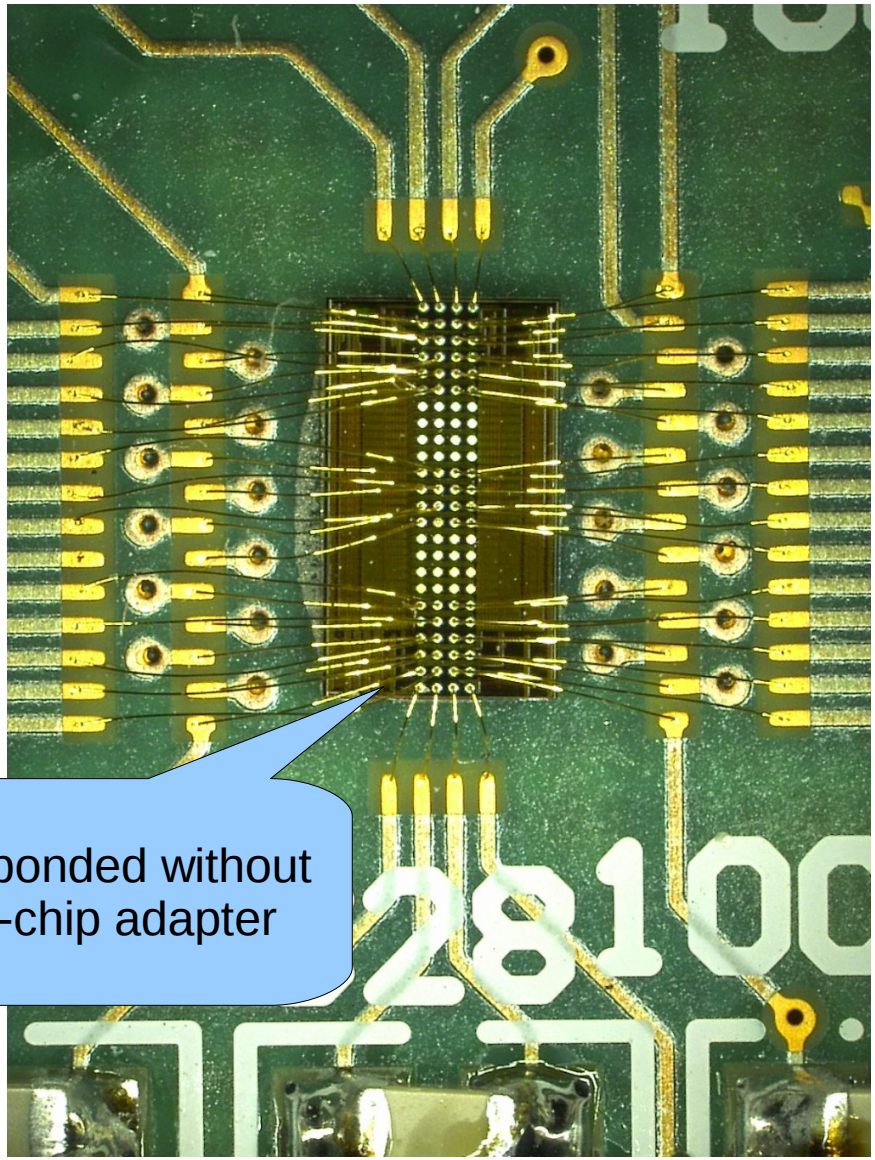
Switcher Measurements

- JTAG
  - ID Register
  - Boundary Scan Chain
  - User Register
- Control
  - Channel Shift Register
  - Gate- & Clear-Strobe
- Operating Modes
  - Non-overlapping gate pulses
  - Overlapping gate pulses
  - Row skip mode
  - Gated mode with halted read-out
  - Gated mode with read-out
- Output timing

Switcher Test PCB

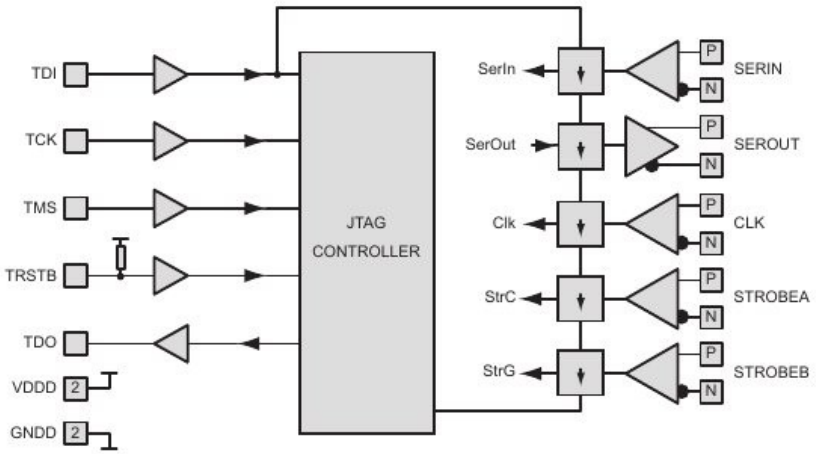
- Test PCB with output load capacitors



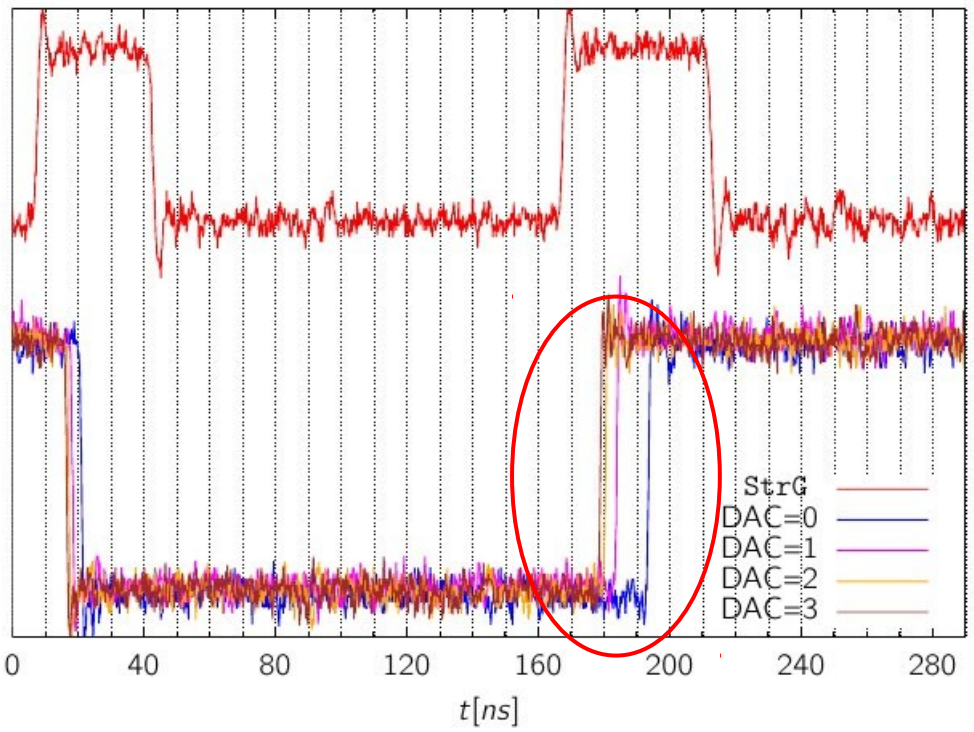


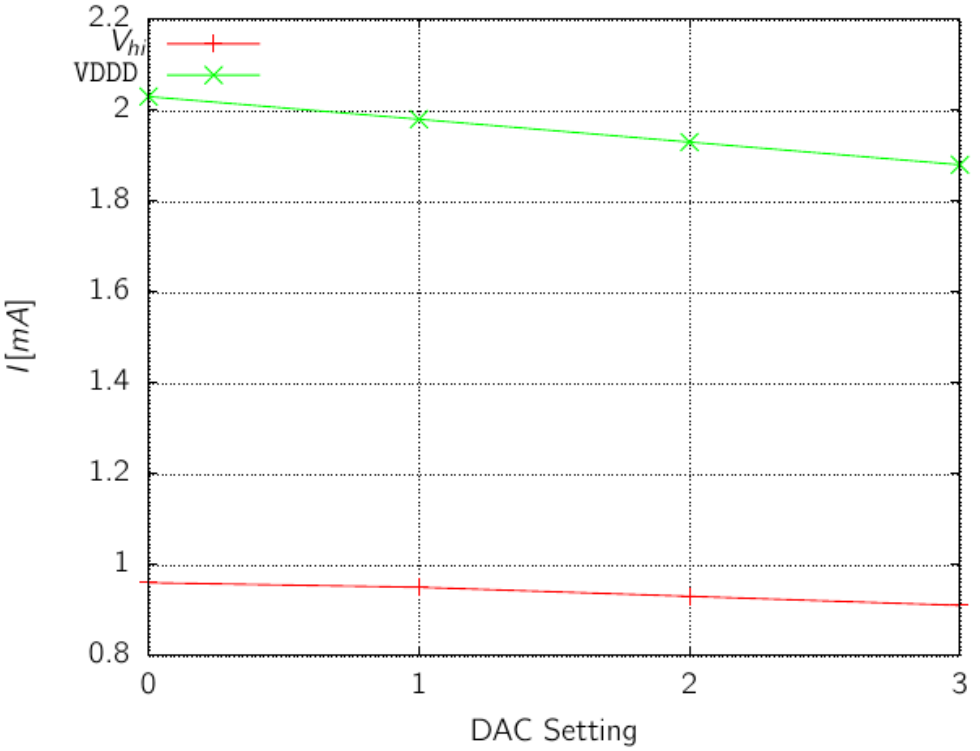
Testsoftware

- JTAG
  - ✔ ID Register
  - ✔ Boundary Scan Chain
  - ✔ User Register readback
- Control
  - ✔ Channel Shift Register
    ✔ Gate- & Clear-Strobe
    - via Boundary scan
    - via gate&clear output



User register DAC setting

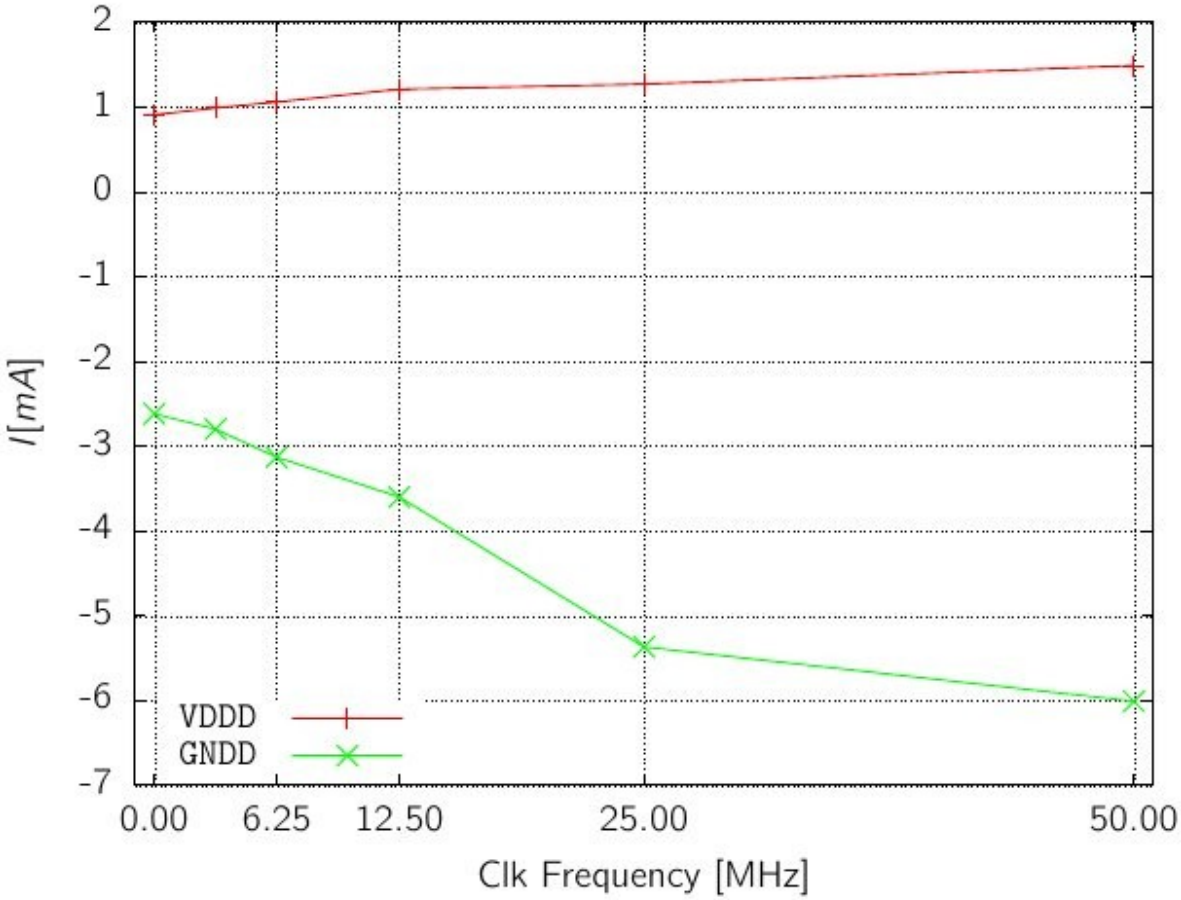




- ✔ Majority voter
- ✔ IBiasBoost setting
  - Lower current with increasing setting
  - Slower speed with increasing setting

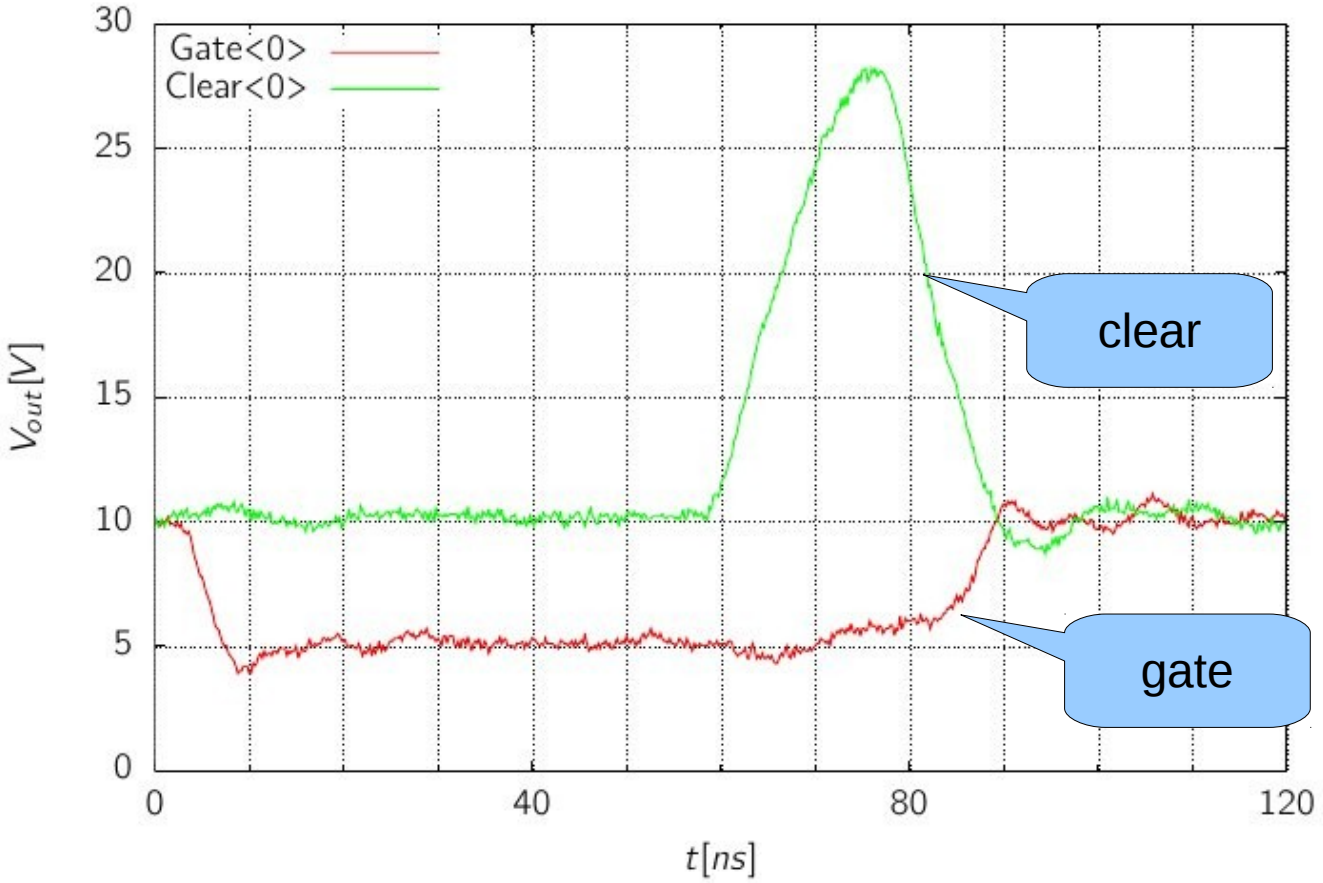
Power consumption

- 80ns matrix row read-out time => 12.5MHz clock
- ✔ linear behavior



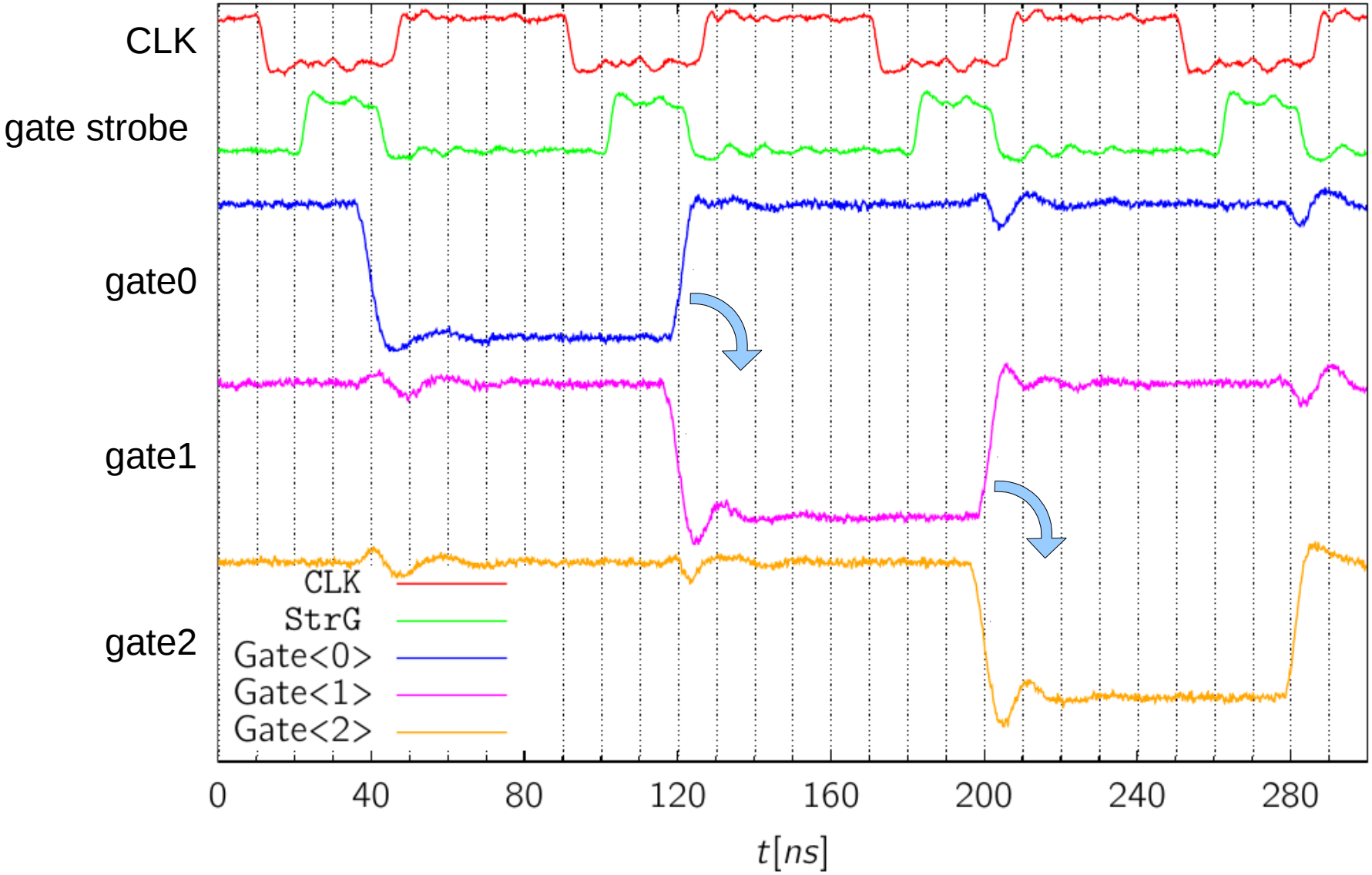
Output timing

- Typical operation of gate-on and clear pulse
- Nominal voltages
- 90pF load



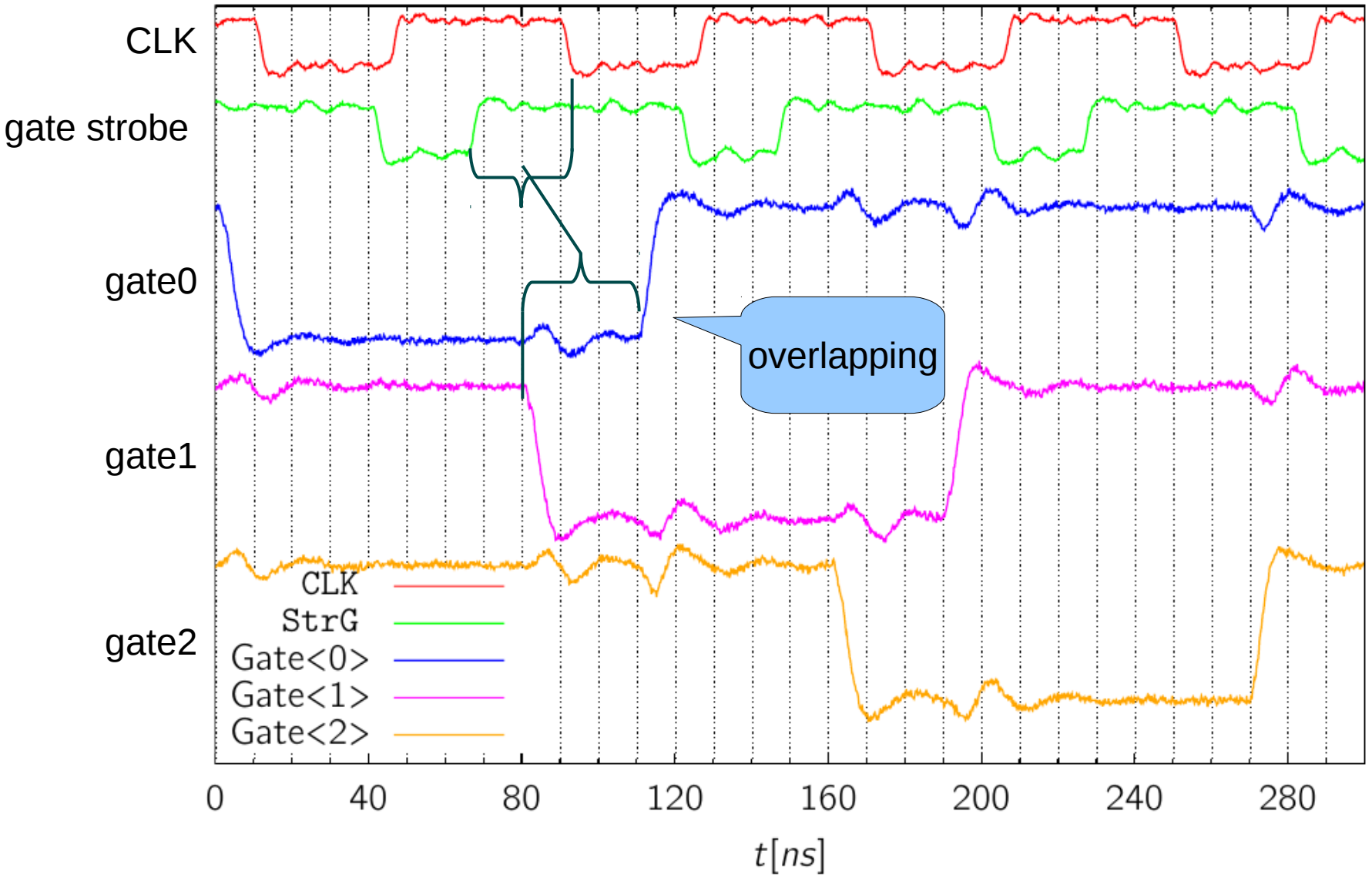
Non-Overlapping Gate Pulses

- rising edge of gate strobe after falling CLK edge



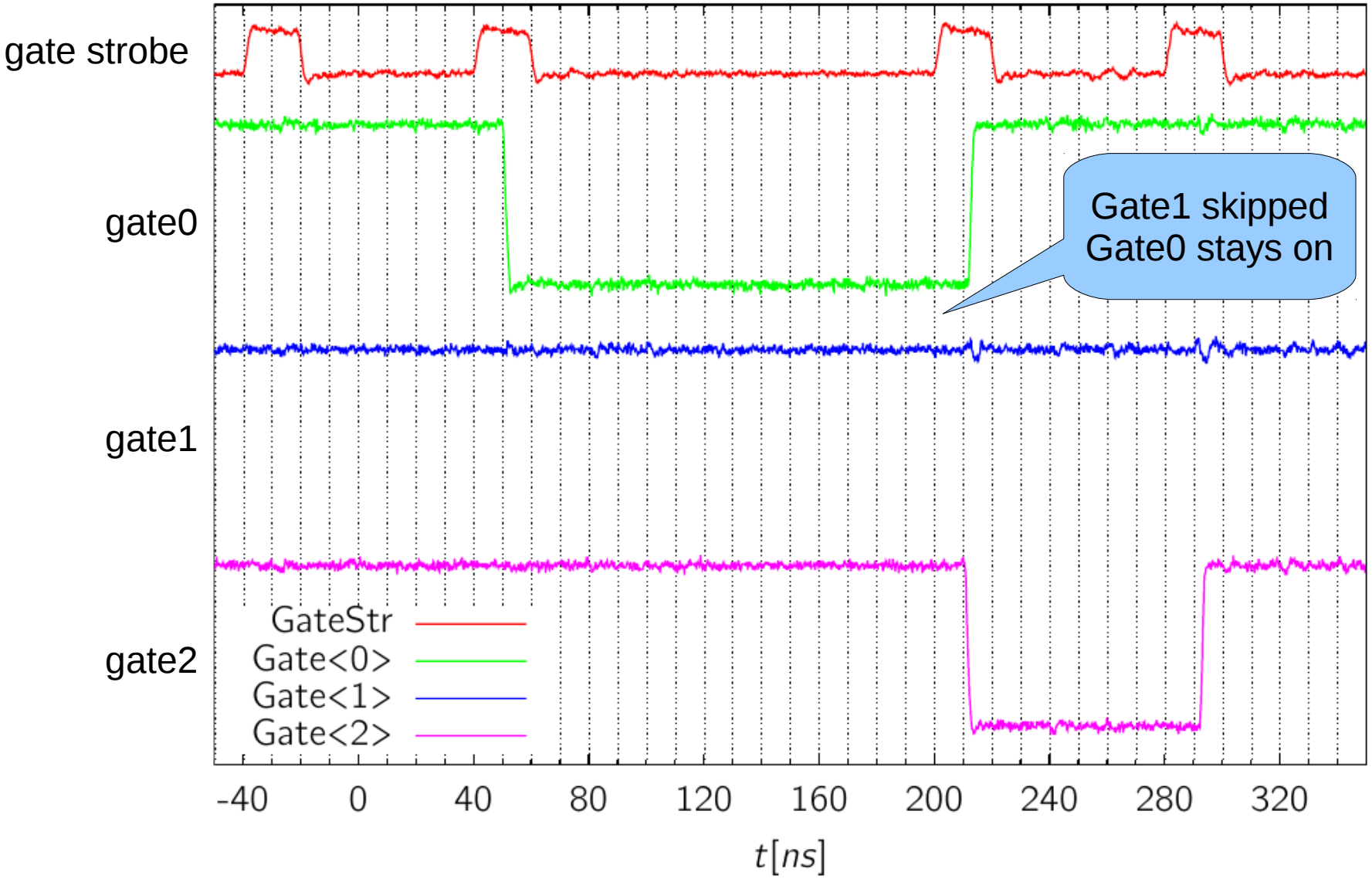
Overlapping Gate Pulses

- rising edge of gate strobe before falling CLK edge



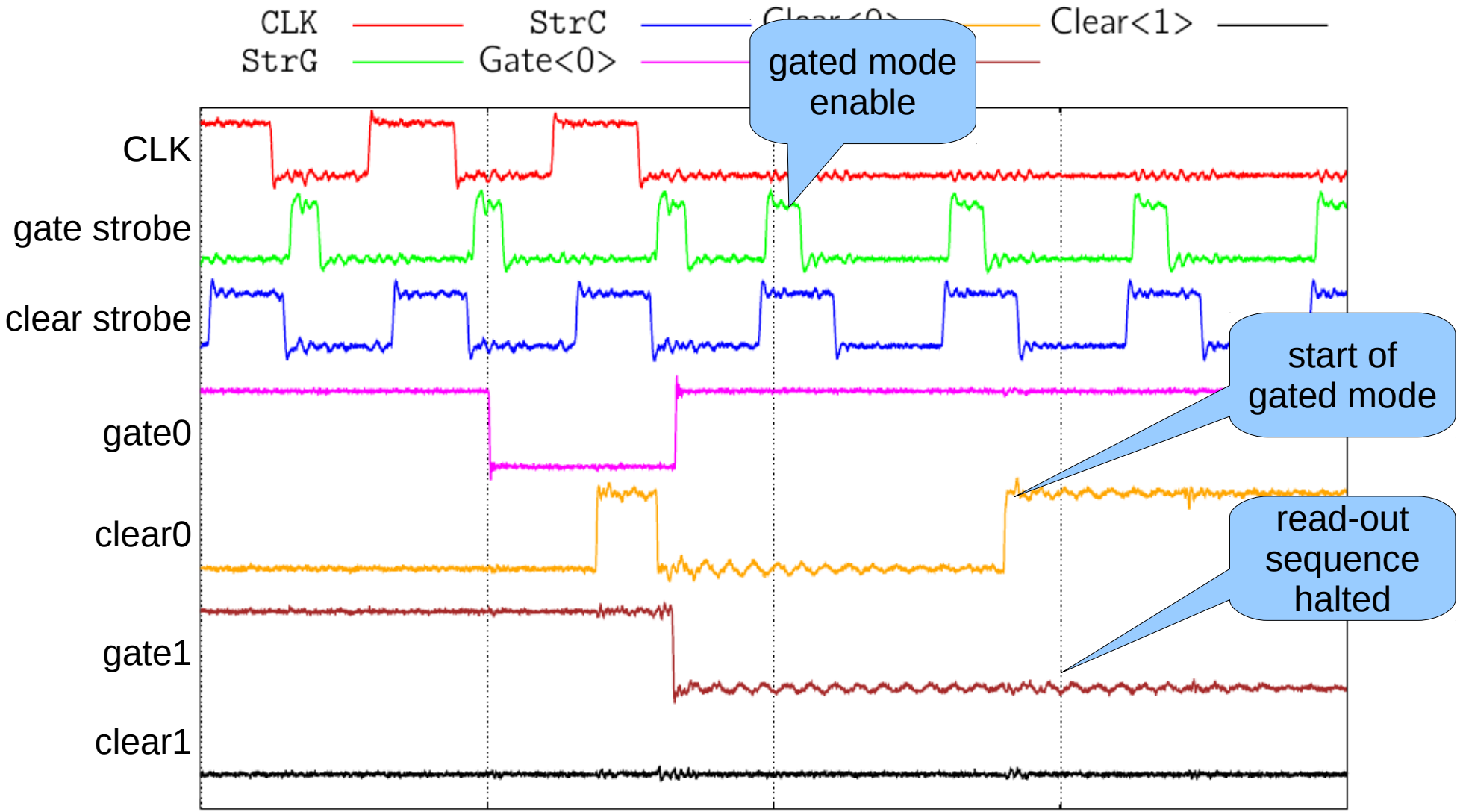
Row Skip Mode

- gate strobe omitted to skip gate1



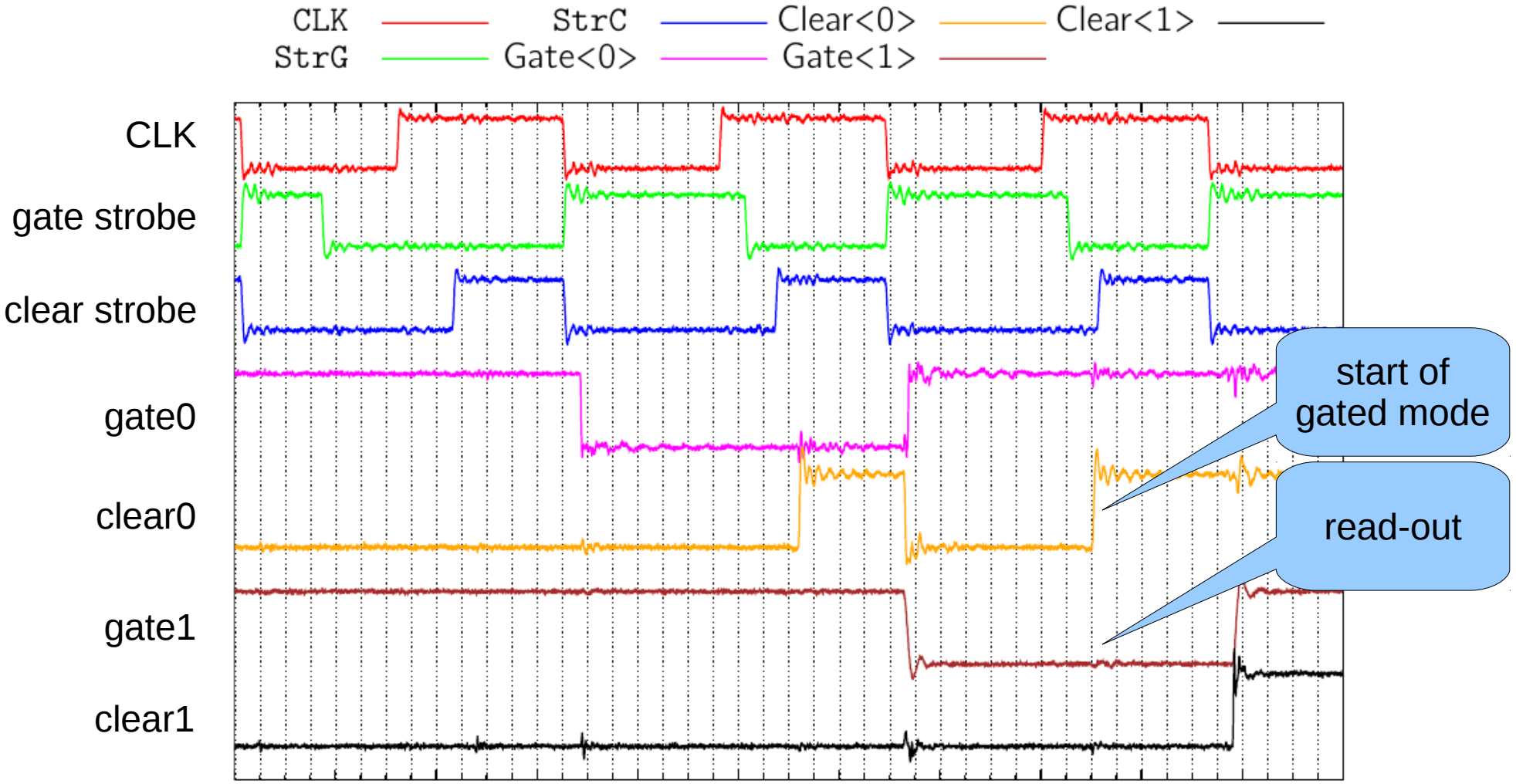
Gated Mode with halted read-out sequence

- stop CLK while clear strobe is high and gate strobe is running



Gated Mode with read-out

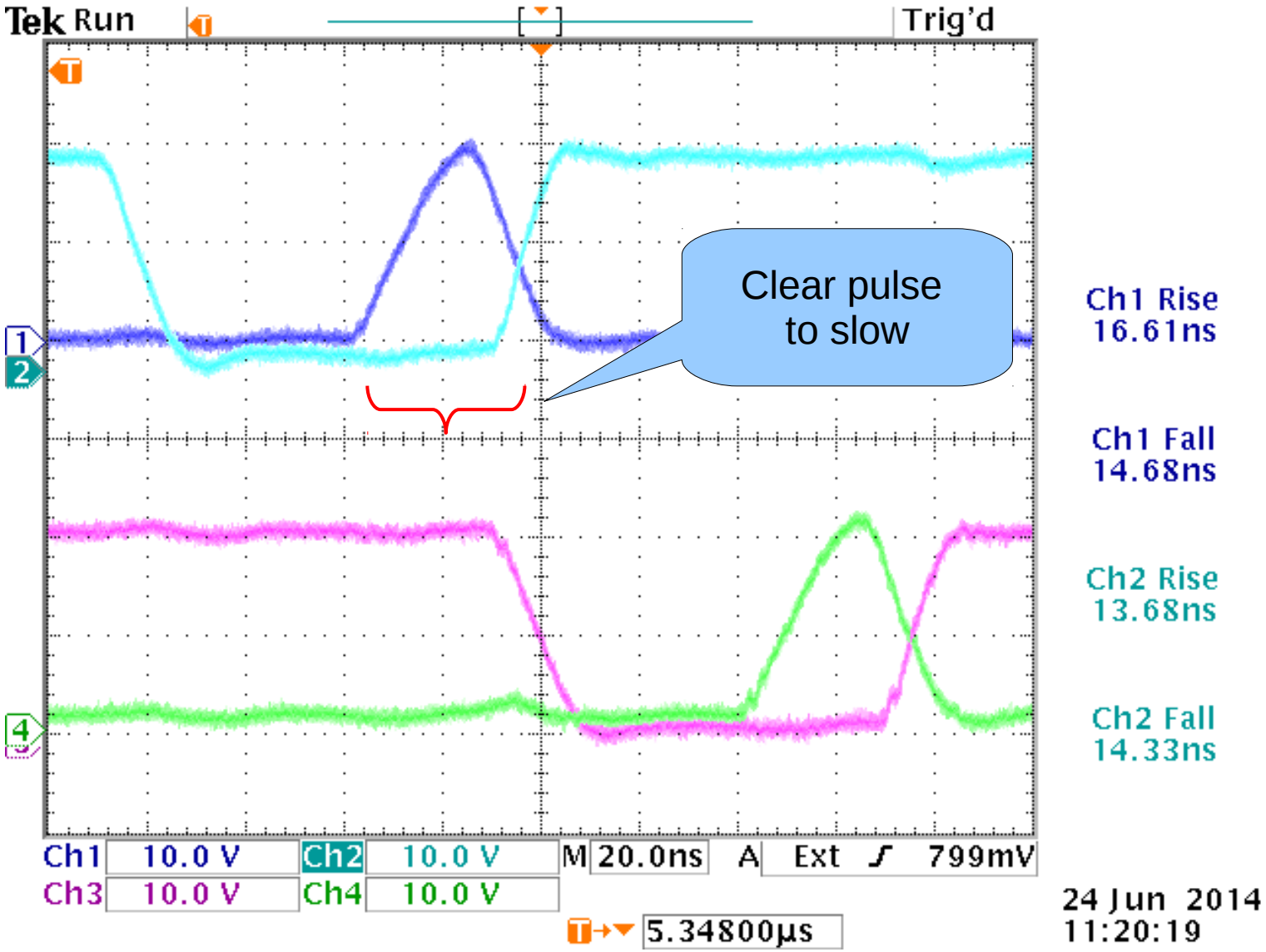
- high level CLK or clear strobe at the falling edge of gate strobe
- CLK is running



Irradiation Settings

- Xray irradiation facility Karlsruhe
  - 60kV 30mA; 100mm distance; Vanadium filter
  - 1118krad/h
  - 20Mrad
- SwitcherB settings during irradiation
  - VDDD=1.8V;
  - GateLo=ClearLo=GND
  - GateHi=ClearHi=20V
  - Running with 100ns timing
  - 150pF cap. load

20Mrad – 150pF load



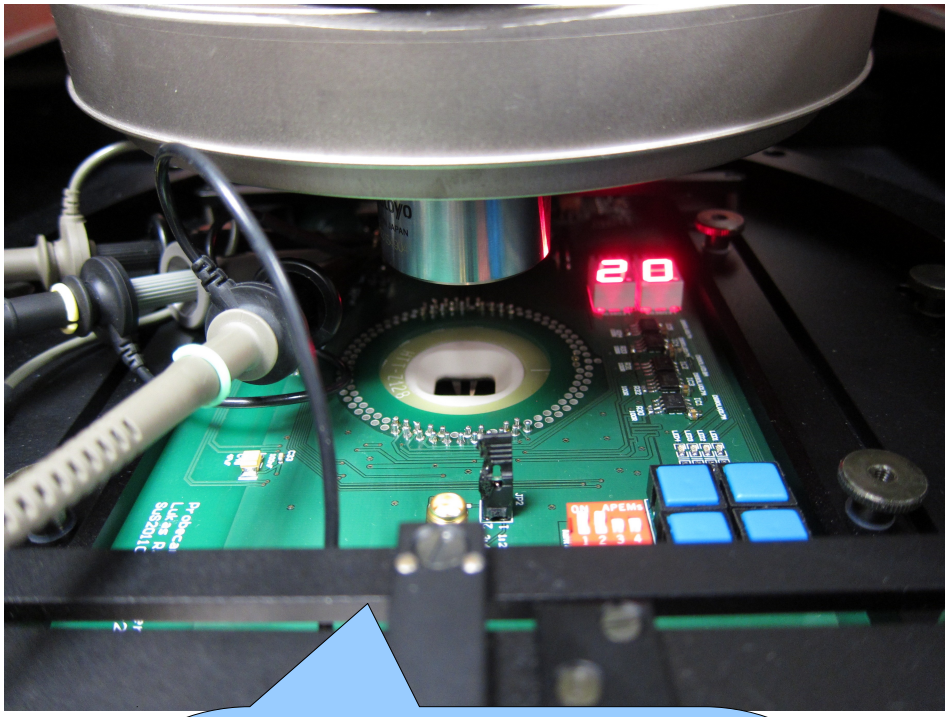
I_{VDD}=3mA I_{Vhigh}=25mA

Measurement summary

- Operating Modes
  - ✔ Non-overlapping gate pulses
  - ✔ Overlapping gate pulses
  - ✔ Row skip mode
  - ✔ Gated mode with halted read-out
  - ✔ Gated mode with read-out
- Output timing
  - ✔ Gate signal (6ns 5V@150pF)
  - ✘ Clear pulse too slow (20ns 20V@150pF)
    - 150pF est. load higher than chip design goal
    - Fix in next chip revision
- Irradiation
  - ✔ 20Mrad: chip is working

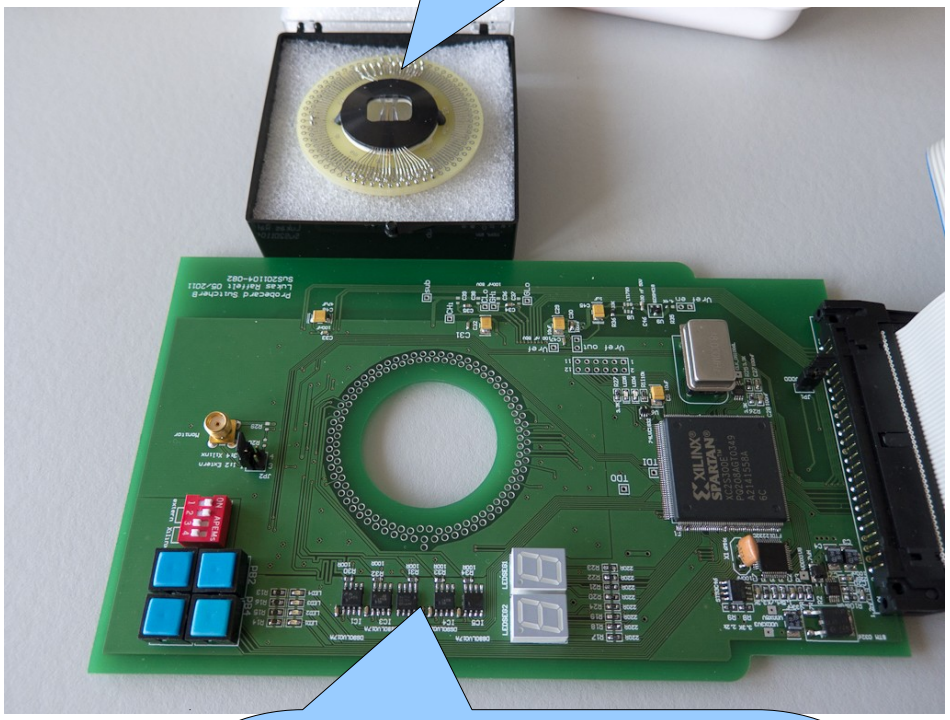
Probestation Testing

Current SwitcherB Probecard



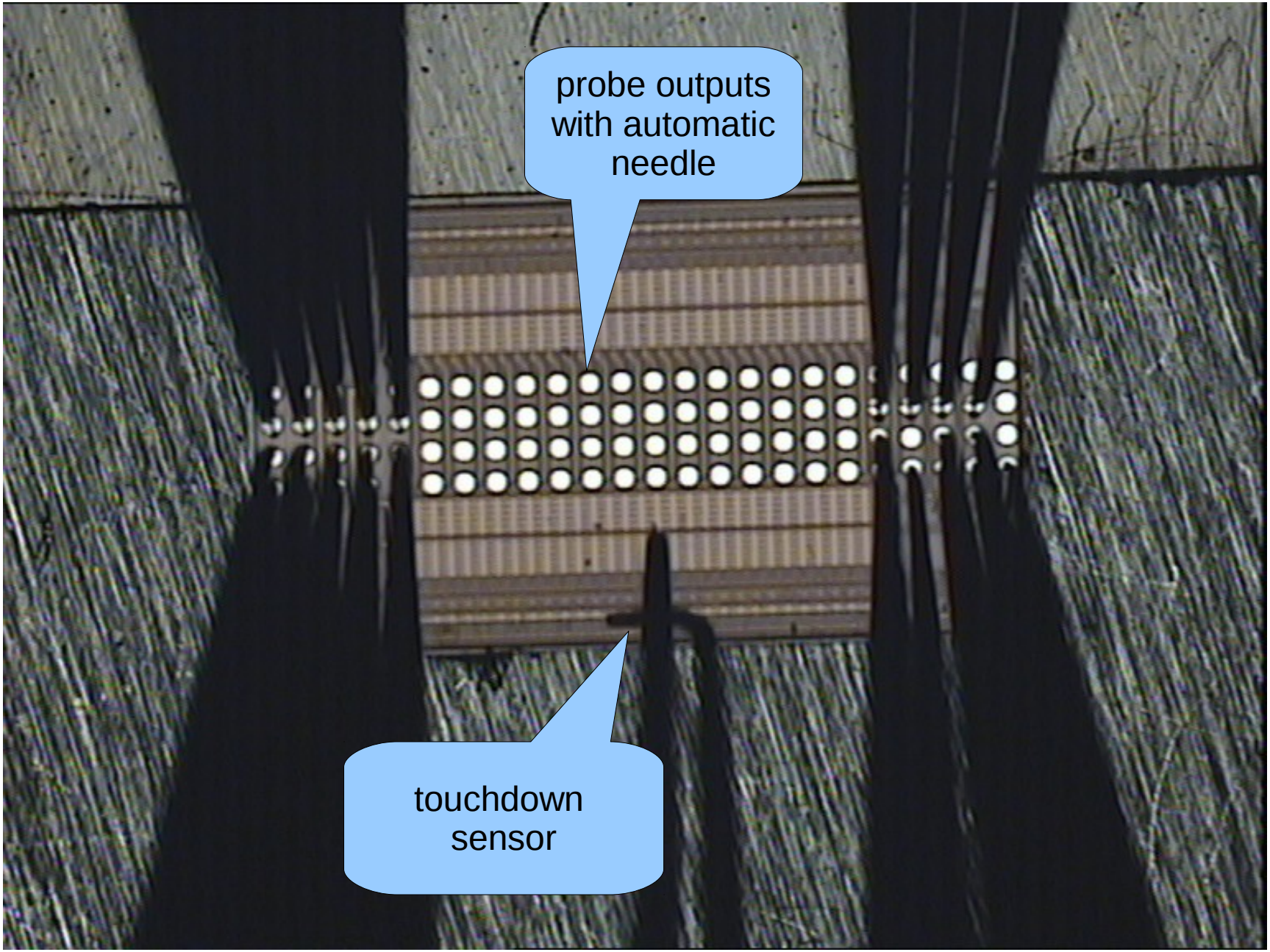
Probecard PCB mounted Probestation

Needle Ring



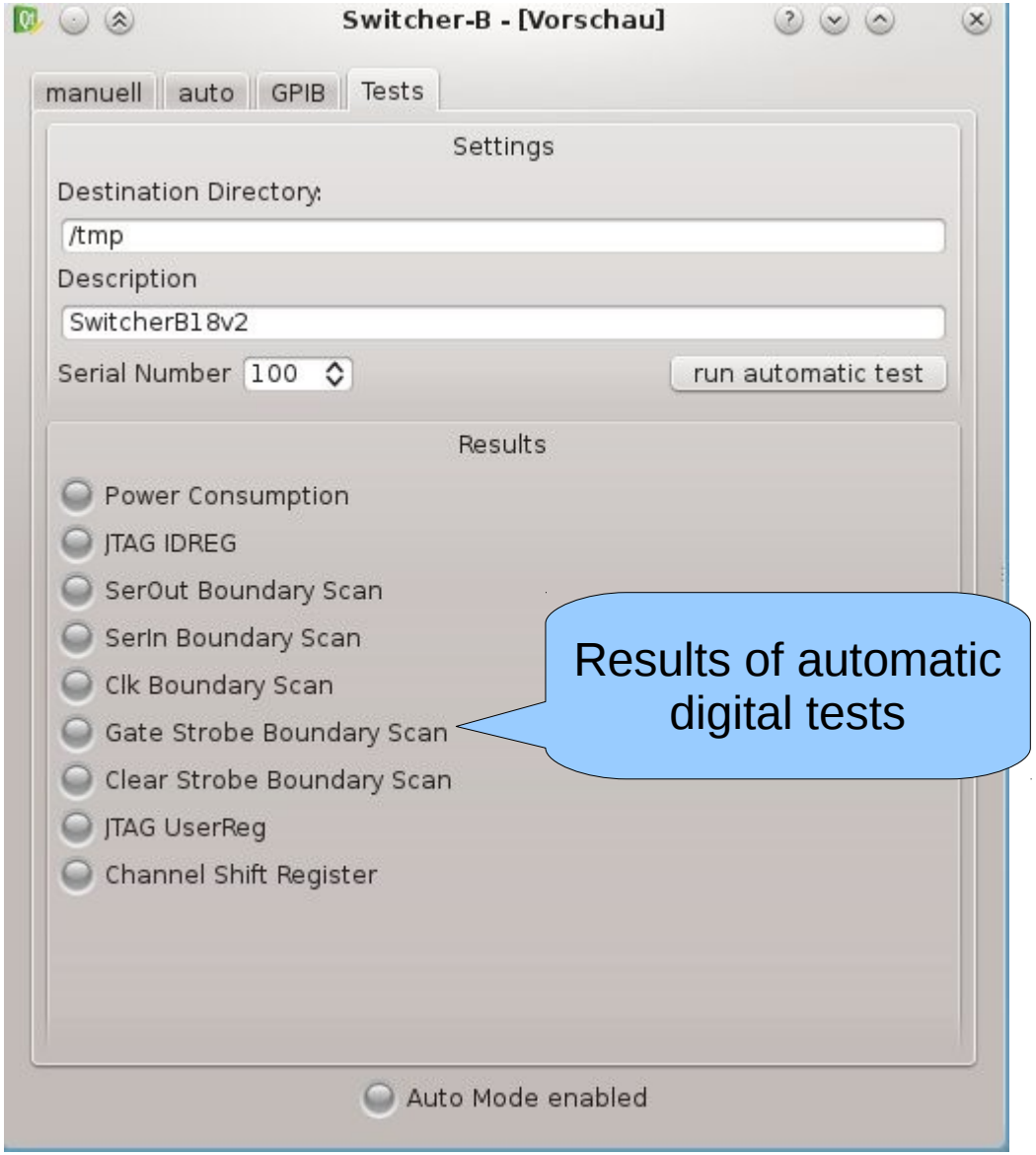
Probecard PCB with onboard FPGA

Current Probeneedles



Switcher Testsoftware

- power on, check currents
- run JTAG tests
- test shift function of channel shift register
- probe channel outputs manually and check on oscilloscope
- testreport file written



Recommendations for Mass Testing

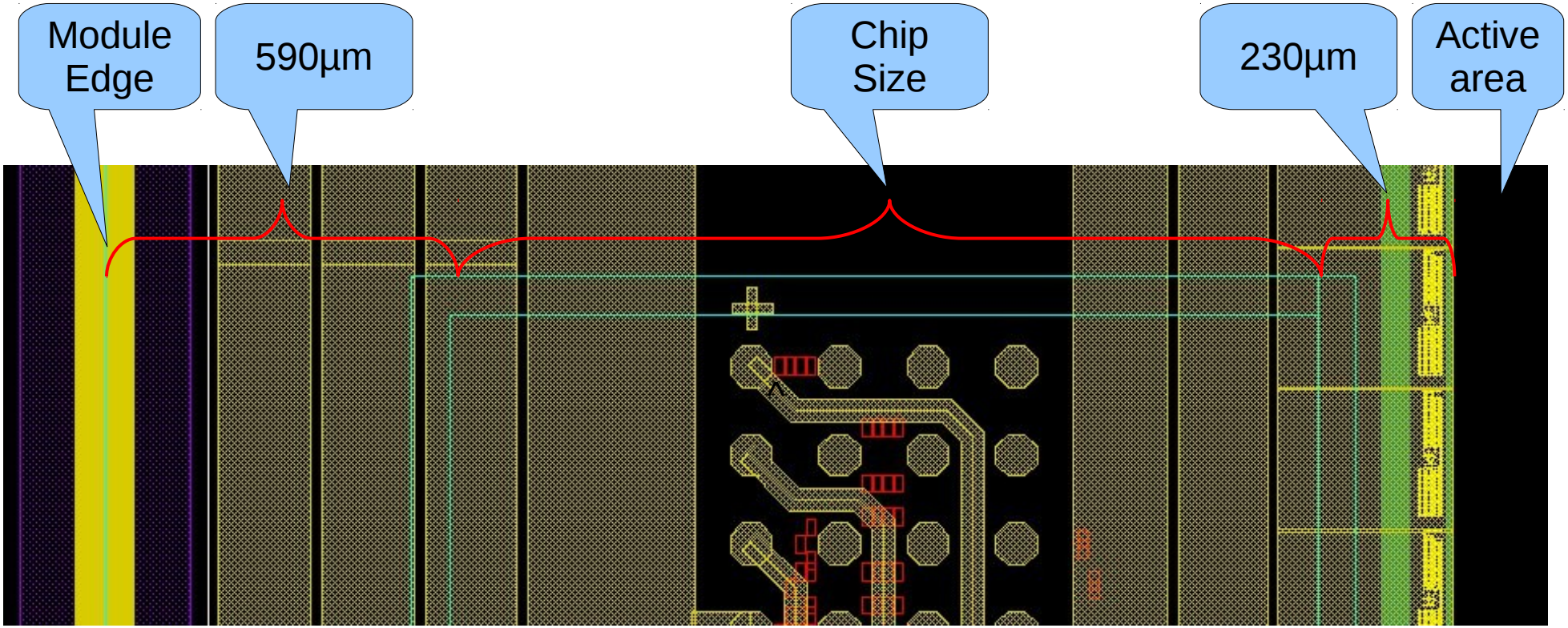
- Current setup only suitable for low volume testing
- Output testing
  - automatic probe needle slow and error prone
  - use needle ring which connects all pads simultaneously
  - multiplex outputs and measure with oscilloscope or onboard ADC
- Needle shape
  - Find optimal shape for PacTech bumped chips

Yield

- SwitcherB18v1:
  - 130 chips, 15 defect (11.5%), 4 operator damage (14.6%)
- SwitcherB18v2:
  - 60 chips, 2 defect (3,3%), 3 operator damage (8.3%)
- Defects
  - JTAG fail
  - Digital i/o fail
  - High power consumption
- Operator damage
  - Destroyed bumps with tweezers
  - Bumps damaged by needles
  - Burned chip with laser
  - Wrong chip orientation

Thank you!

Module Balcony

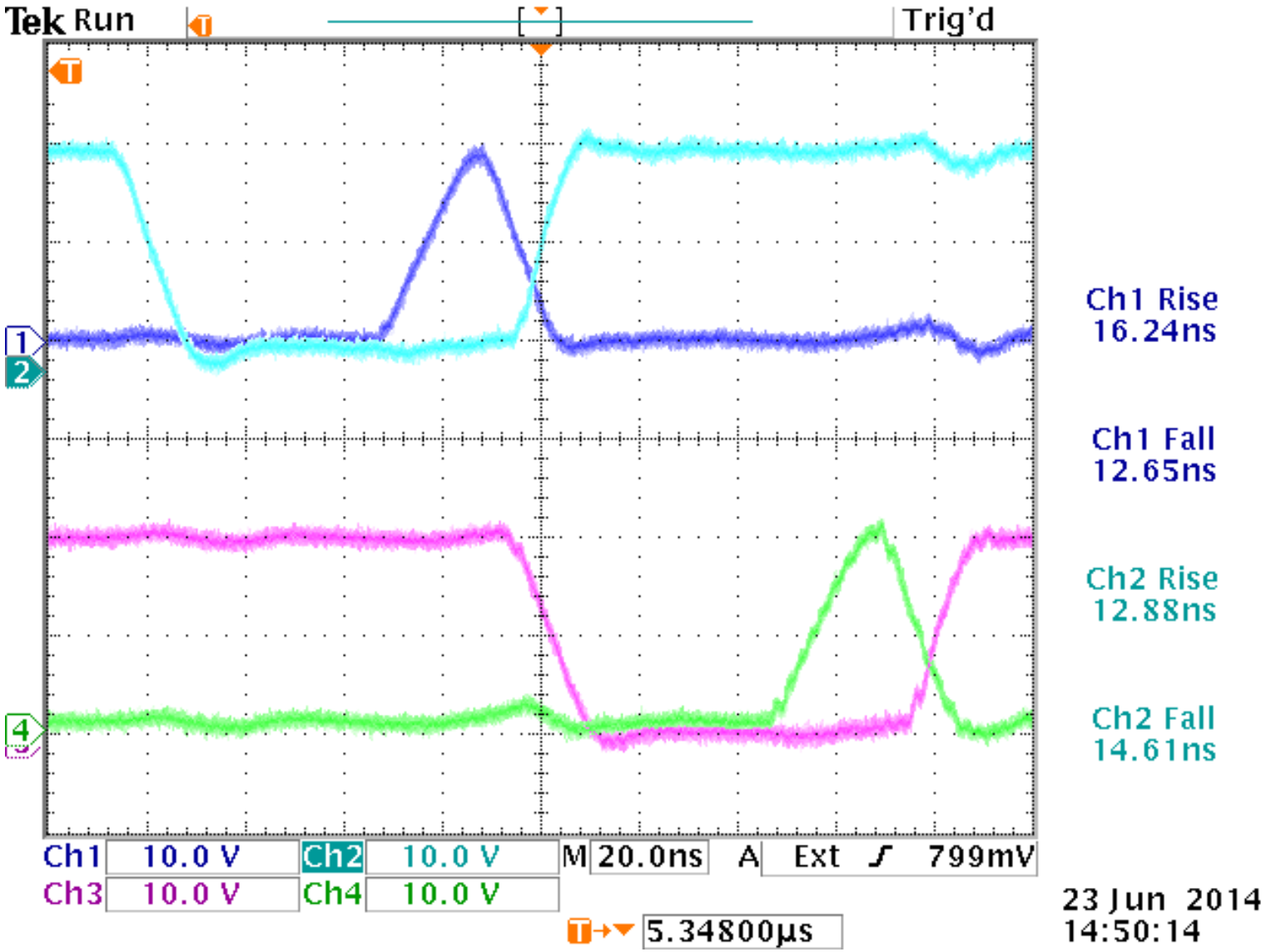


check maximum size with mechanics design!

Testreport File

```
###############
Switcher Automatic Test
###############
Chip Serial Number: 1
Description: SwitcherB18v2
Date: 2013_07_24-09:01:47
###############
initializing chip
###############
clearing shift register
setting JTAG bypass
setting UserReg: EnableTermination=on, Ibias=3,
IbiasBoost=3
###############
Power Consumption
###############
A+Bhigh:   10.009V 0.003A
VDDD+Vref: 1.802V  0.005A
###############
reading JTAG IDREG
###############
IDREG is 0x23456789 should be 0x23456789
IDREG is 0x23456789 should be 0x23456789
IDREG is 0x23456789 should be 0x23456789
JTAG IDREG read successfull in 3 of 3 cases
###############
SerOut boundary scan test
###############
serout is 0 should be 0
serout is 1 should be 1
serout is 0 should be 0
SerOut test successfull in 3 of 3 cases
###############
SerIn boundary scan test
###############
data out is 0x0 expected 0x00
data out is 0x10 expected 0x10
data out is 0x0 expected 0x00
SerIn test successfull in 3 of 3 cases
###############
Clk boundary scan test
###############
data out is 0x0 expected 0x00
data out is 0x4 expected 0x04
data out is 0x0 expected 0x00
clk test successfull in 3 of 3 cases
###############
GStr boundary scan test
###############
data out is 0x0 expected 0x00
data out is 0x1 expected 0x01
data out is 0x0 expected 0x00
gstr test successfull in 3 of 3 cases
###############
CStr boundary scan test
###############
data out is 0x0 expected 0x00
data out is 0x2 expected 0x02
data out is 0x0 expected 0x00
cstr test successfull in 3 of 3 cases
###############
JTAG UserReg test
###############
writebuffer 0x000000000fff  readbuffer 0x000000000fff
...
```

500krad - 150pF load



I_{VDD}=3mA I_{Vhigh}=18mA