

# Bit Error Rate Test of DHPT 1.0 Gigabit Serial Link

**Leonard Germic**, Carlos Marinas, Hans  
Krüger and Norbert Wermes  
germic@physik.uni-bonn.de

University of Bonn

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- 1 Gigabit Serial Link
- 2 Test Setup
- 3 Results

## Facts:

- 1.6 GHz differential output
- programmable preemphasis
- off-chip  $100\ \Omega$  matching resistors
- 1.2 V domain (VDD\_CML, core voltage)

- Compensation of the attenuation of high frequency regime in the signals spectrum due to long distance transmission
  - Increasing bandwidth
  - Preventing single bit error

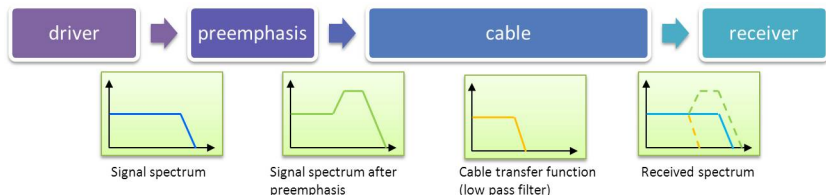
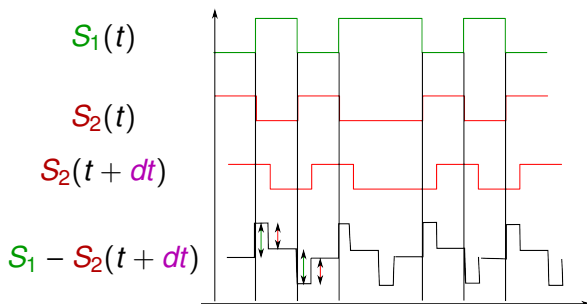
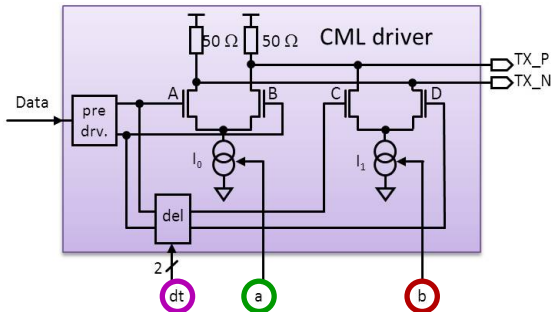


Figure: Signal spectrum with preemphasis.

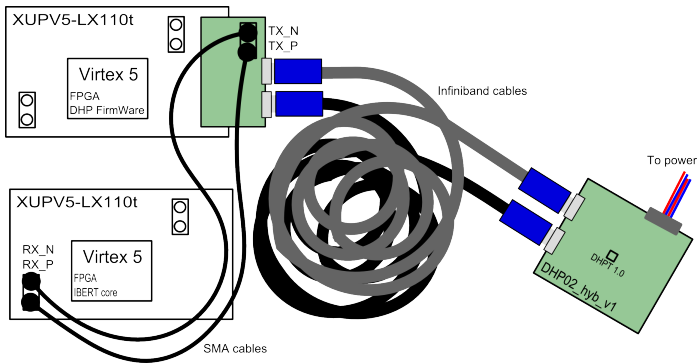
- Preemphasis realization: Subtraction of signal  $S_1$  with delayed signal  $S_2$ .
- Two 8 bit DACs  $IDAC\_CML\_TX\_BIAS$  and  $IDAC\_CML\_TX\_BIASD$
- One 2 bit DAC  $pll\_cml\_dly\_sel$



- Current Mode Logic Driver with programmable preemphasis
- Three parameters:
  - **IDAC\_CML\_TX\_BIAS**, **IDAC\_CML\_TX\_BIASD**, **pll\_cml\_dly\_sel**
  - Same values of **IDAC\_CML\_TX\_BIAS** and **IDAC\_CML\_TX\_BIASD** do not correspond to same currents/differential voltage swing (differently sized current mirrors)



- 1x Evaluation board XUPV5 – LX110t as DHH emulator
- 1x Evaluation board XUPV5 – LX110t as Bit Error Rate Tester (IBERT, Xilinx)
- 2x 15 m Infini band cables
- ... and a crazy 'handmade' script



**Figure:** BERT Test system. Top board = DHH emulator, Bottom board = IBERT (Xilinx).



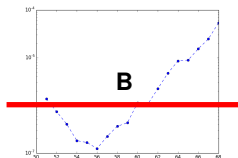
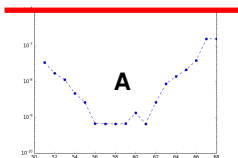
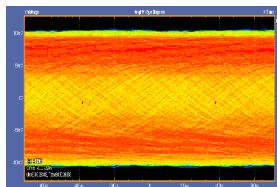
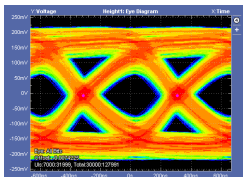


Figure: Red line indicates the  $BER_{thr}$  of  $10^{-6}$

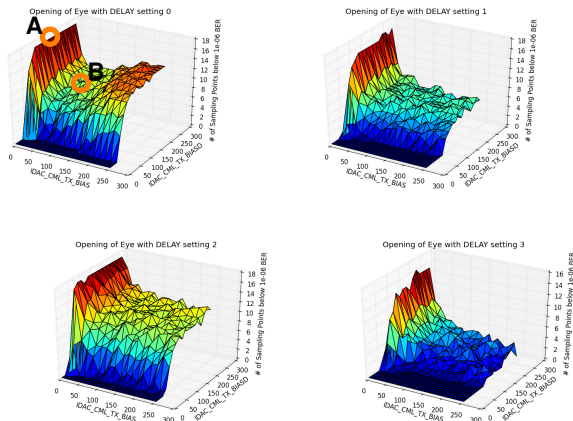
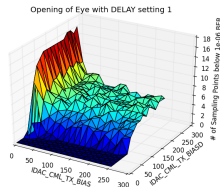
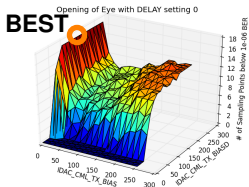
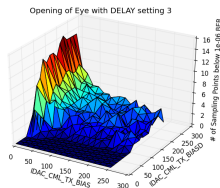
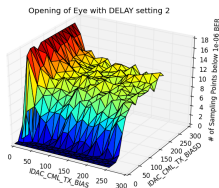


Figure: Sweep results at a threshold of  $BER_{thr} = 10^{-6}$ . Higher is better - wider opening at  $BER_{thr}$



Optimal working point **BIAS** = 15, **BIASD** = 150, **dly** = 0.



**Thank you for your attention!**

- These are NOT absolute BER values.
- NMOS of current mirrors saturate above DAC values  $\sim 150$  (Design bug)

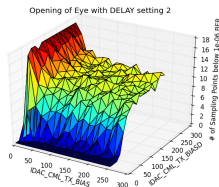


Figure: Plateau due to saturation of the current mirrors.