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Data Handling Processor
Performance Test Results

Tetsuichi Kishishita, Bonn University

DEPFET PXD ASIC Design Review, October 27-28, 2014

Outline

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- Verification results from prototype blocks (DHPT 0.1)
  - PLL & high speed serial link driver
  - Analog blocks (bias generator, temp. sensor)

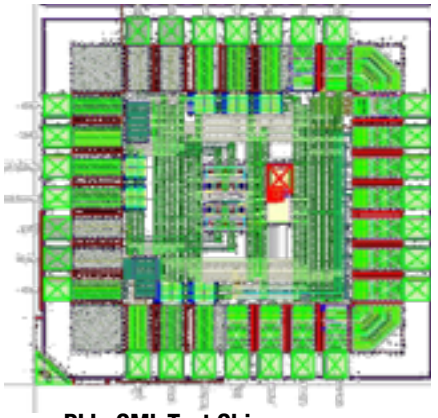
- DHPT 1.0 performance
  - Verification results
  - Known issues & mitigation strategies

DHPT 0.1 Prototype Chip

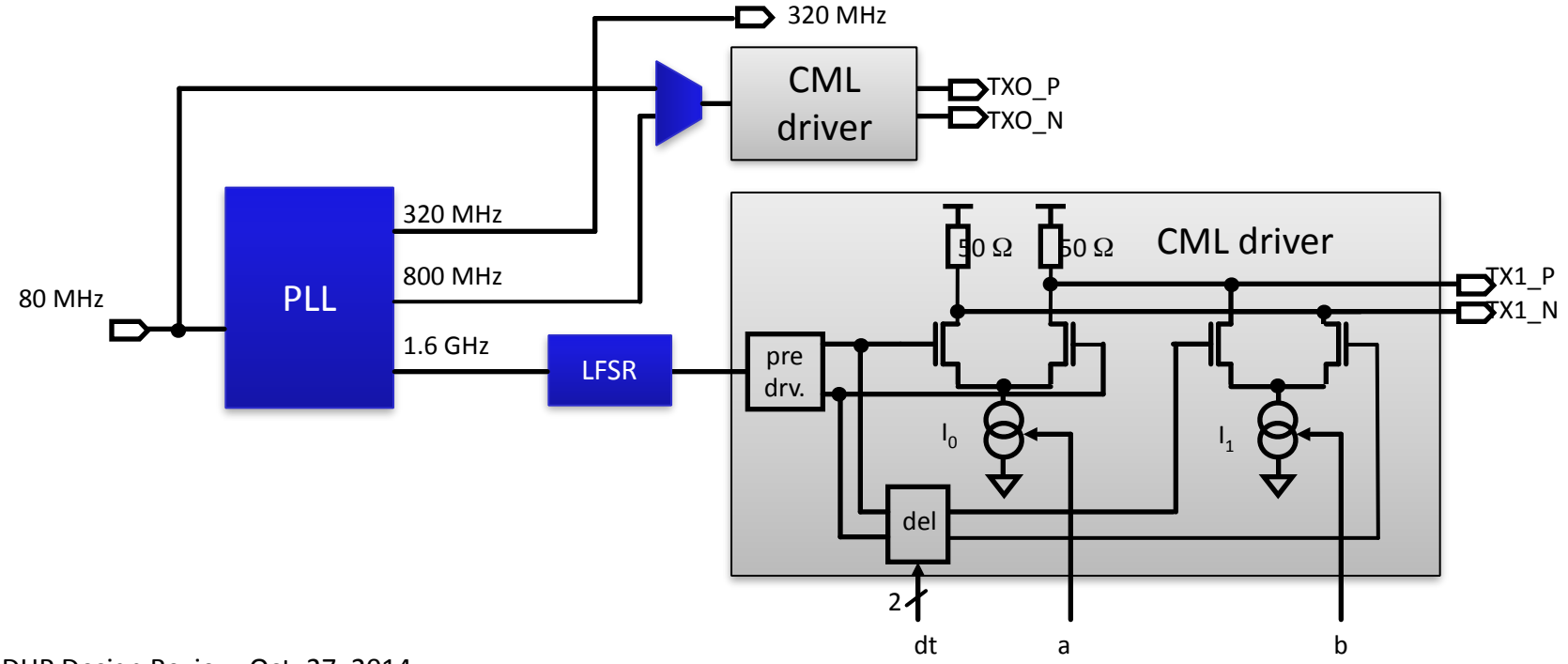
PLL & GBIT DRIVER

DHPT 0.1 - PLL & Gbit Driver

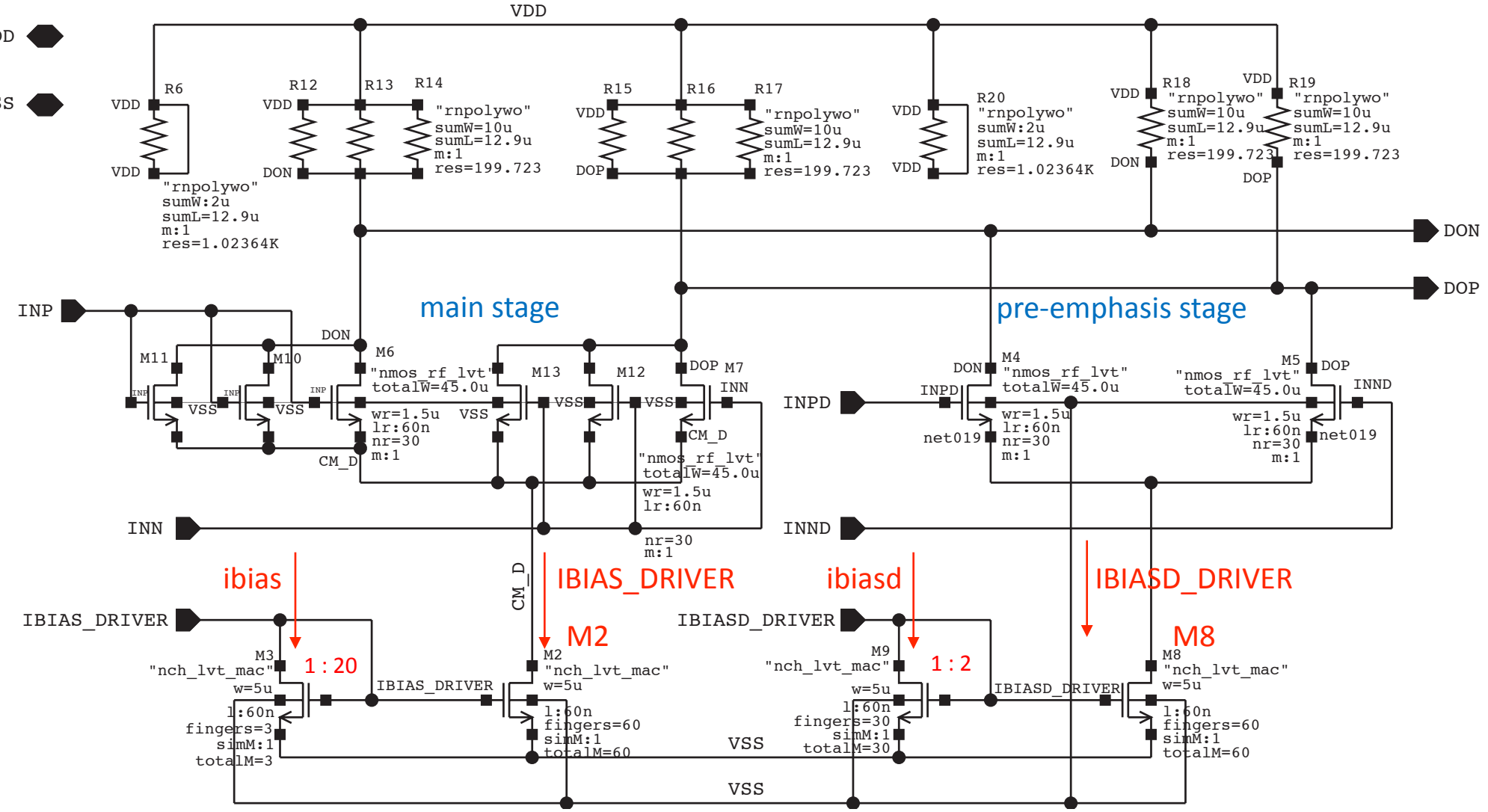
- PLL
  - 80 MHz reference clock
  - 1.6 GHz, 800MHz & 320 MHz outputs
- Pseudo random bit sequence generator
  - 8 bit LFSR
- CML link driver with programmable pre-emphasis
  - Two differential pairs with adj. bias currents (tap weights *a*, *b*)
  - Programmable delay *dt*



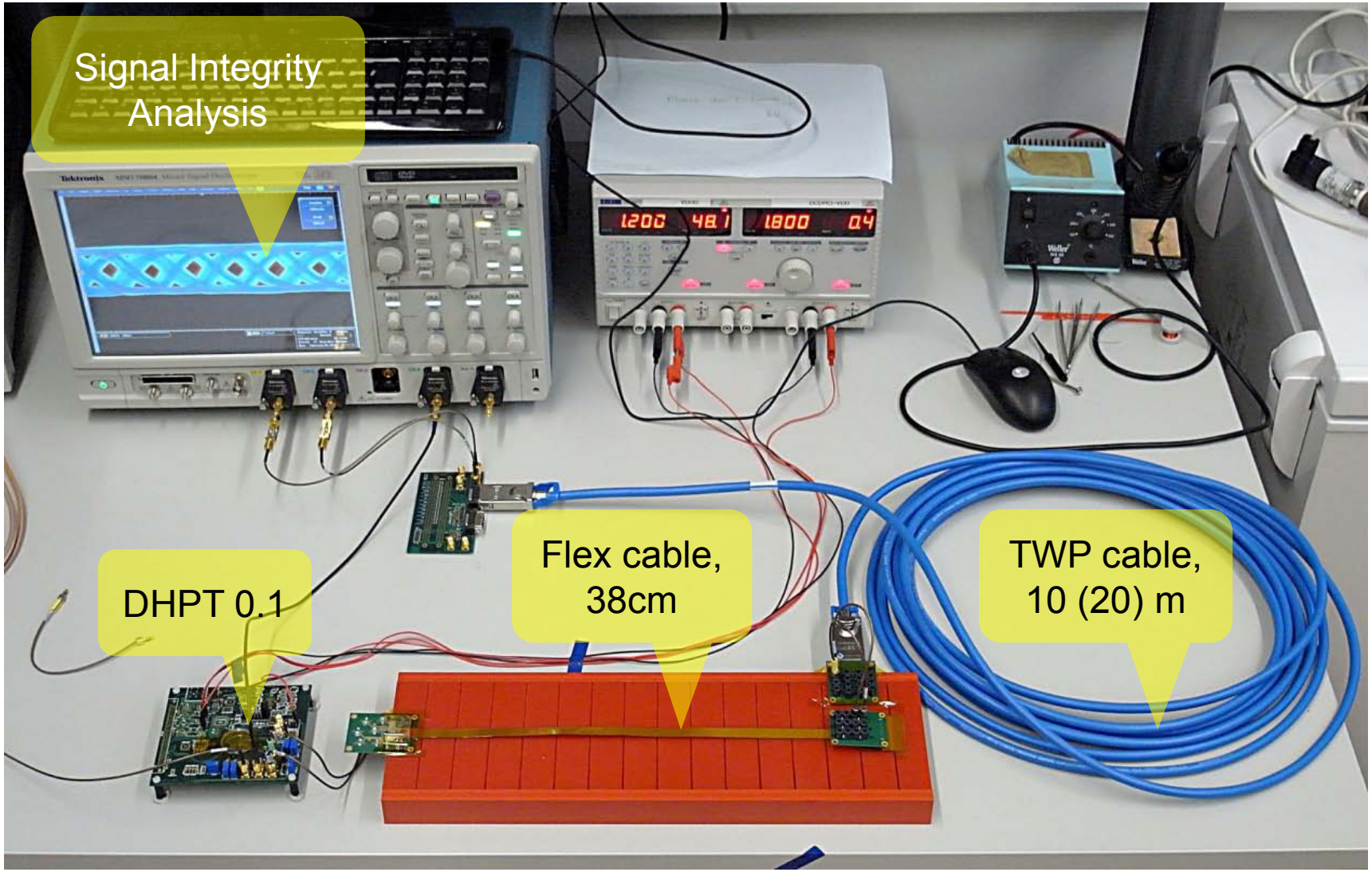
PLL_CML Test Chip,
T. Kishishita



Driver Schematic

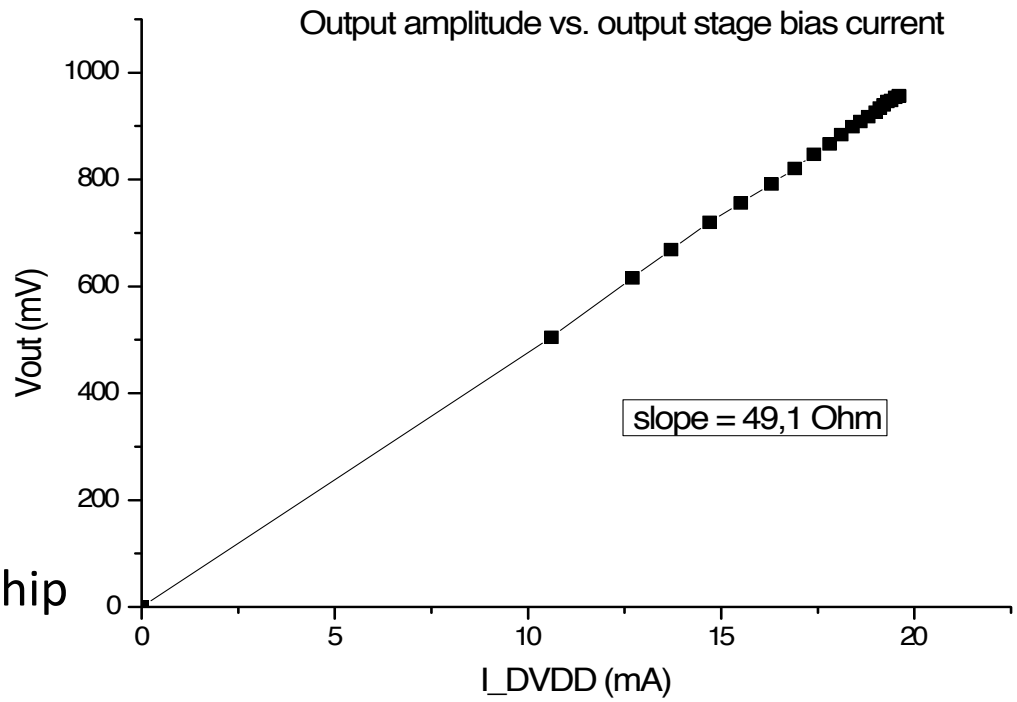


DHPT 0.1 – Test setup



Differential Output Amplitude

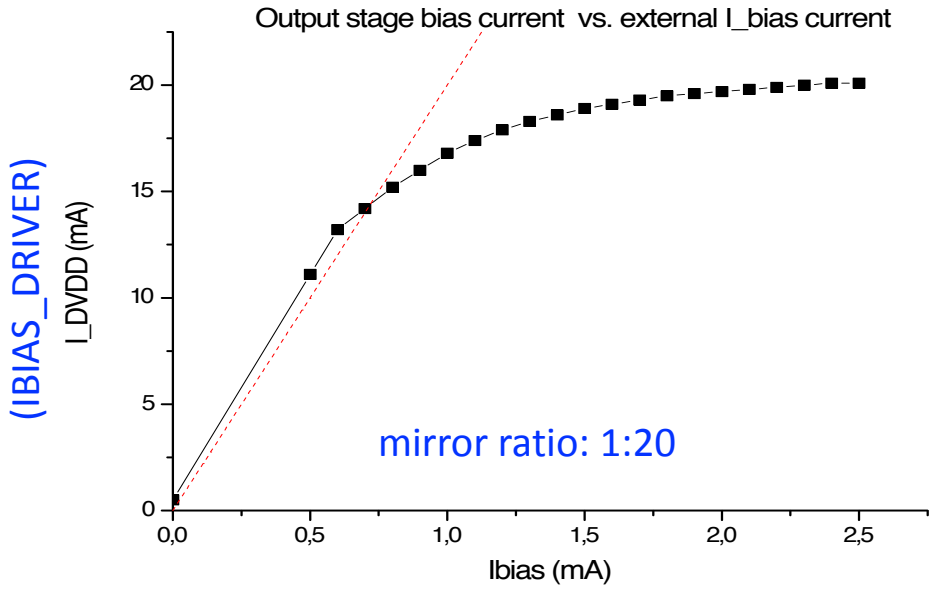
- Linear function of bias current (IBIAS_DRIVER)
- IBIAS_DRIVER ≈ I_DVDD
- Pre-emphasis off (IBIASD_Driver = 0)
- Effective output resistance: 49.1 Ohm
- DC output resistance: 55 Ohm
- ➔ ~3.5 Ohm Series resistance (chip wiring, bond wire, PCB trace)



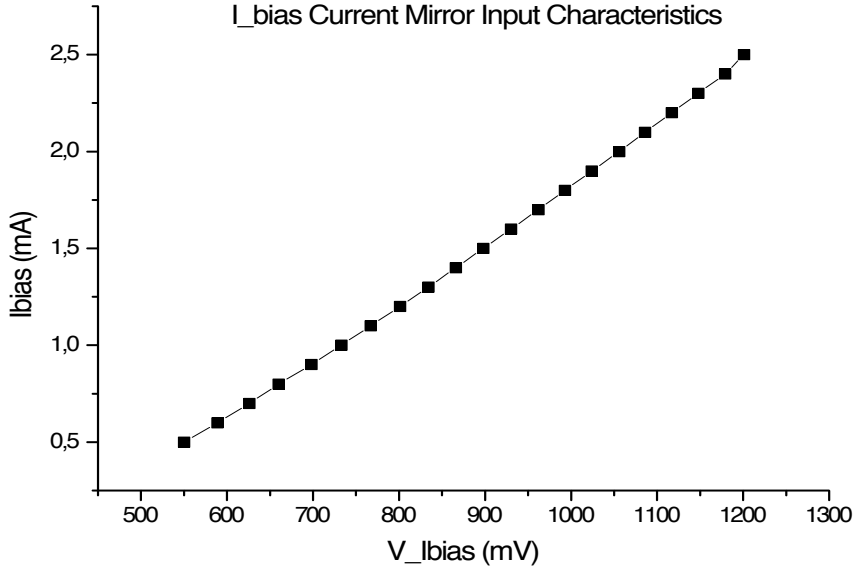
➔ Output resistance Ok

Main Output Current Mirror

- IBIAS_DRIVER current mirror
- Design value
  IBIAS_DRIVER/Ibias = 20
- Non-linear for Ibias > 0.7mA
  ➔ M2 not saturated?
- Drive current limited to 20 mA
  ➔ $Vout_{max}$ = 957 mV

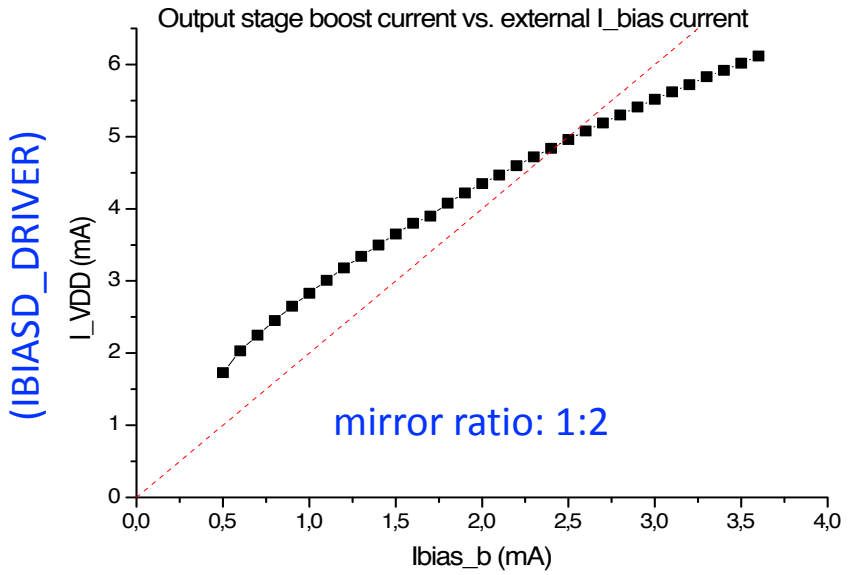


➔ Limited by current sink (M2) or switches M0/M1 (too high on resistance)?

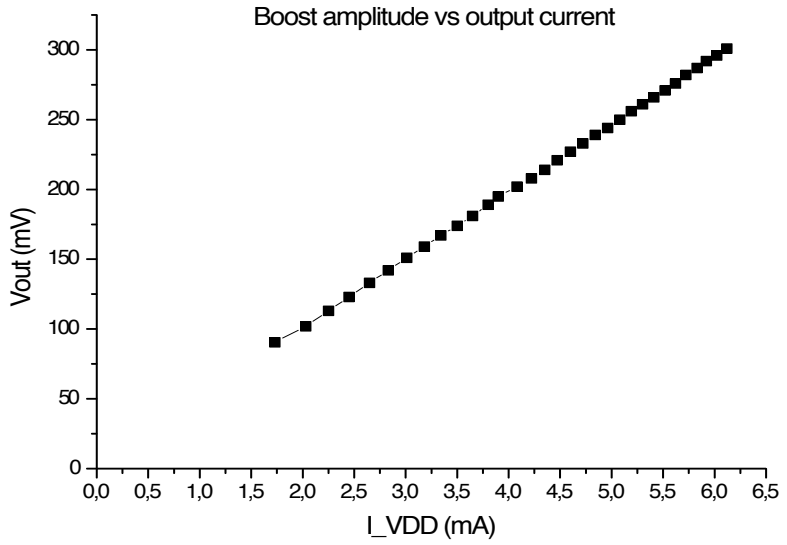


Boost Output Current Mirror

- IBIASD_DRIVER current mirror
- Design value
  IBIASD_DRIVER/Ibiasd = 2
- Fair linearity
- Drive current limited to 6.12 mA
  → $Vboost_{max}$ ~300mV



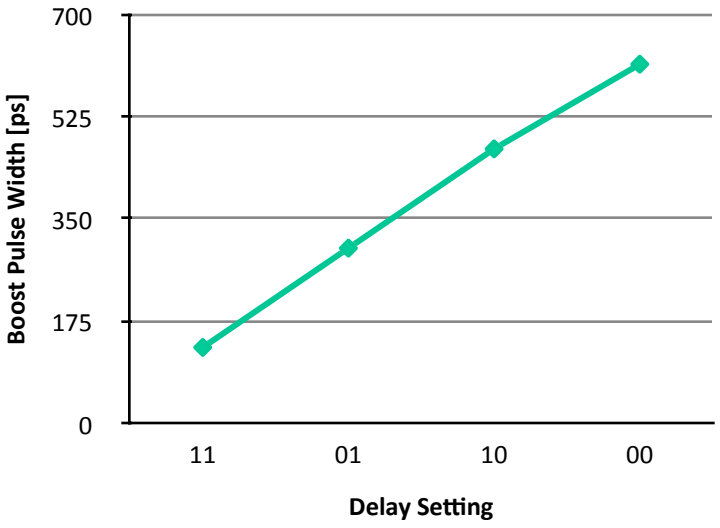
➔ Make boost current sink M8 stronger

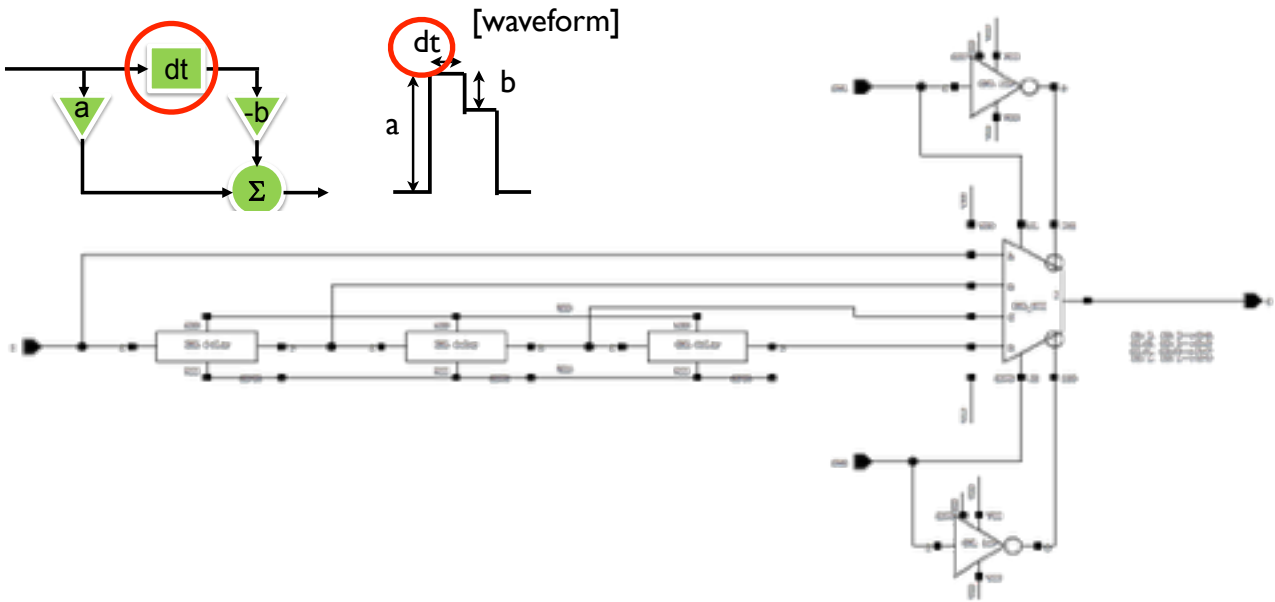


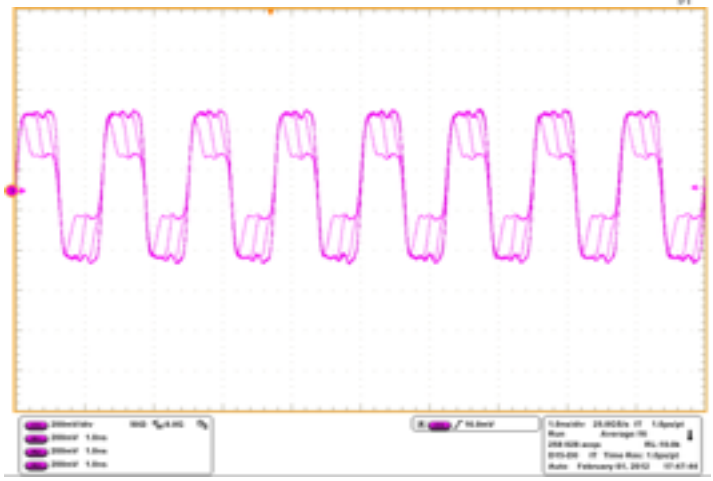
Delay Settings

Setting SW[1:0]	Pulse Width [ps]
11	*130*
01	*300*
10	*470*
00	*615*

➔ ~170 ps per delay buffer



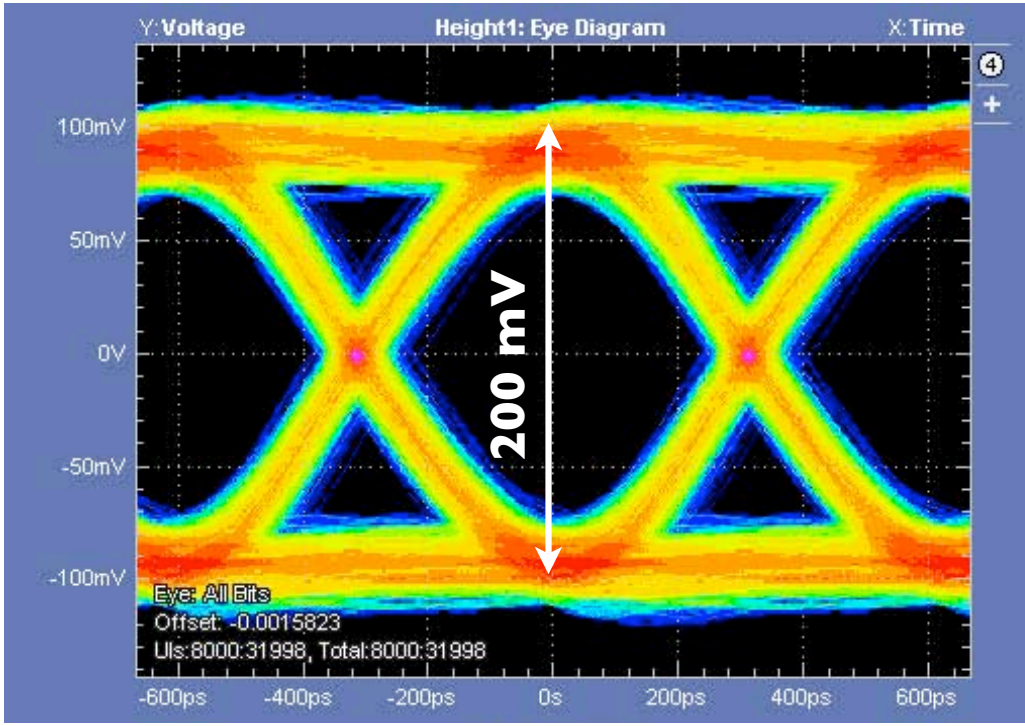


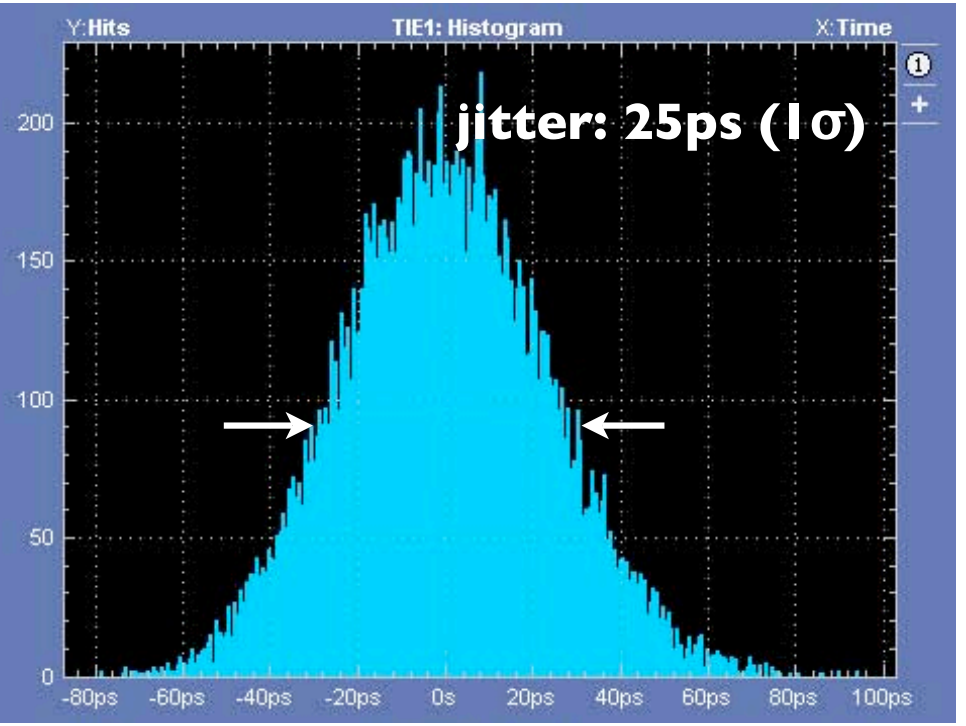


800 MHz clock, different delay settings

Signal Integrity Characterization

- 1.6 Gbps LFSR-8
- 30 cm kapton cable
  + **10m** AWG26
  twisted pair cable





Signal Integrity Characterization

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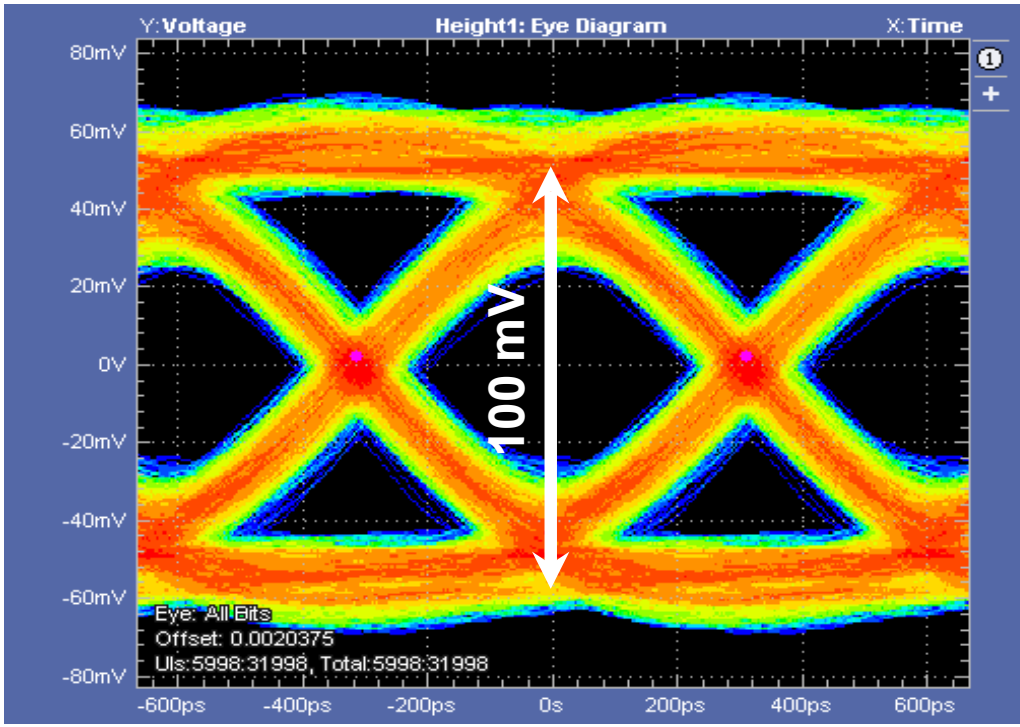
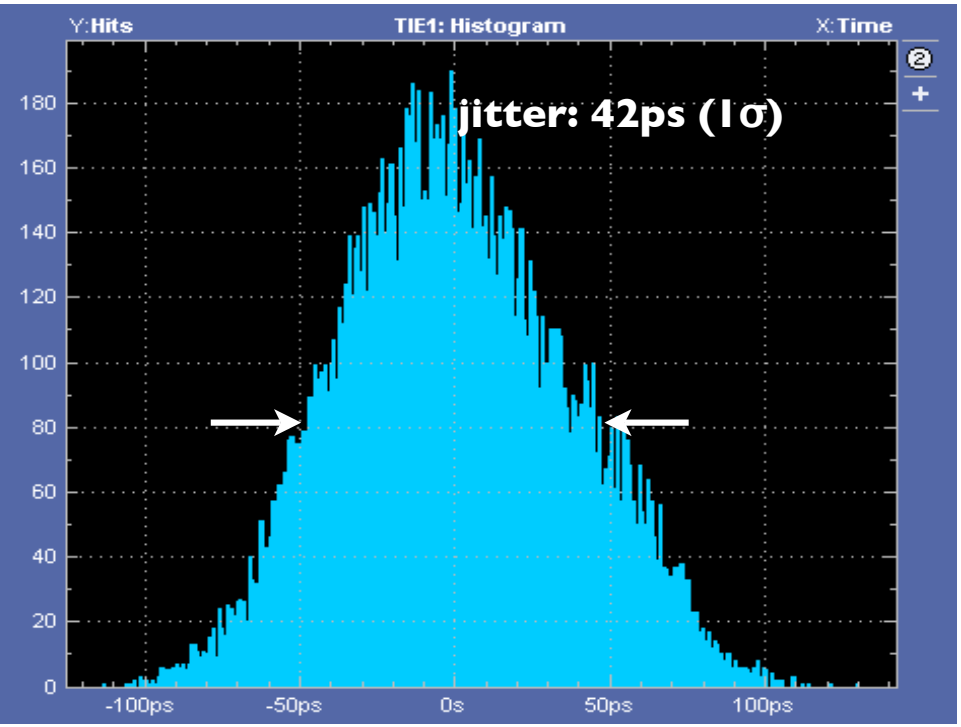


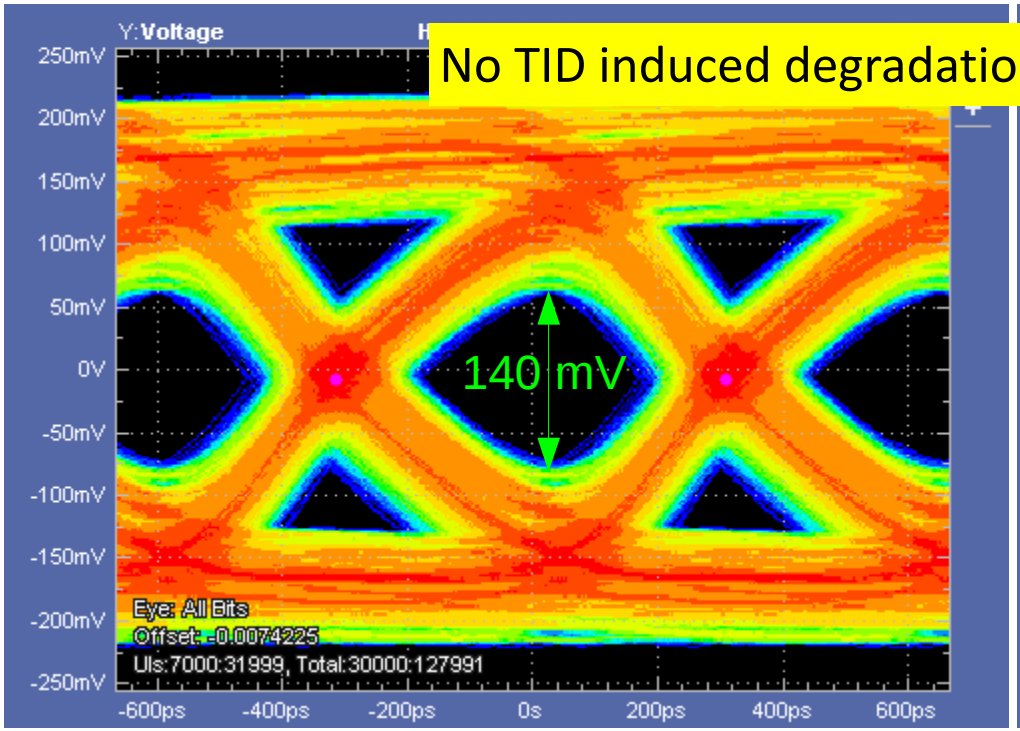


DHPT 0.1 X-ray Irradiation

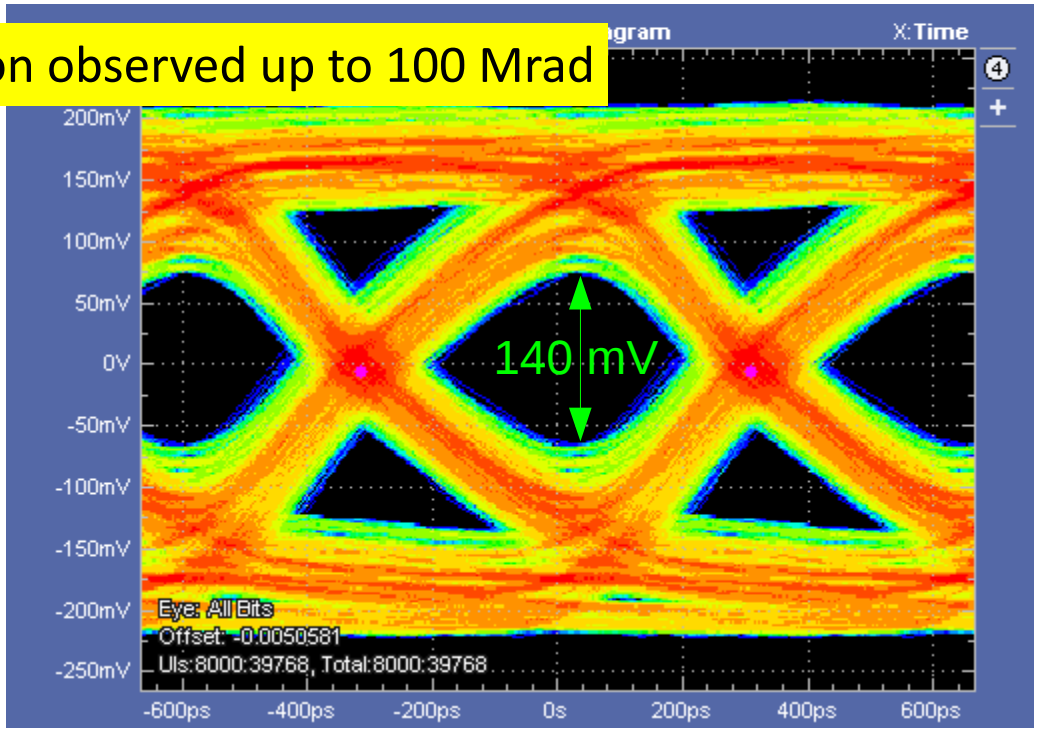
- TSMC 65nm TID tolerance:
  - V_{THR} shift (wide pMOS and nMOS only)
  - PLL + Gbit link performance (with 15 m cable)
- Up to 100 Mrad (60keV X-ray tube, Karlsruhe)
- Dose rates: ~300 kRad/h (initial) → ~2Mrad/h (end)
- Annealing after each step: 80°C for 100 min

Belle II: 10 Mrad for 5 yr operation

No TID induced degradation observed up to 100 Mrad

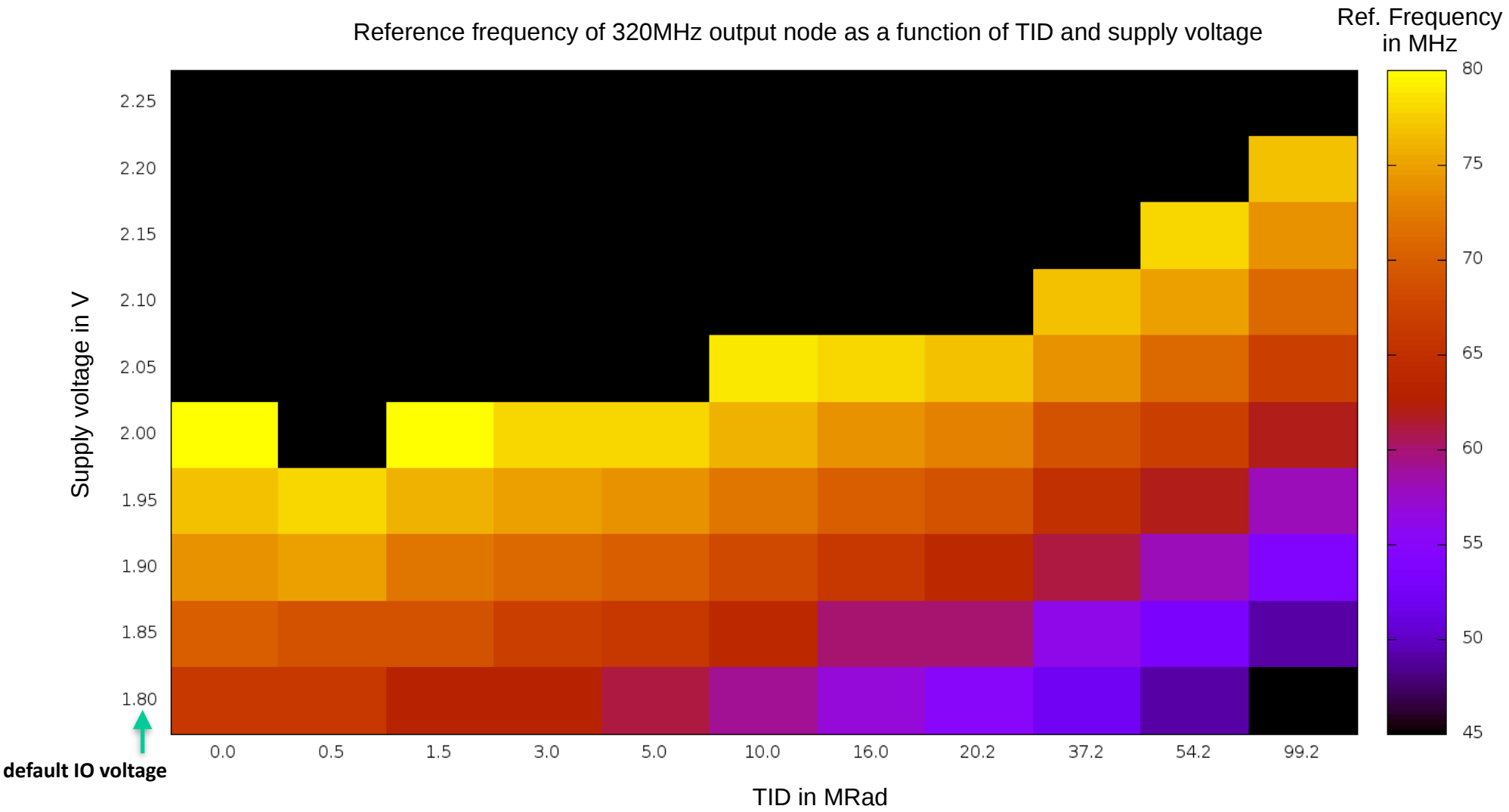


Dose = 0 MRad Jitter ~51 ps



Dose = 100 MRad Jitter ~54 ps

PLL output



PLL works even after 100 Mrad, slow outputs mainly come from CMOS driver (thick gate oxide).

Summary DHPT 0.1 – CML Driver Characterization

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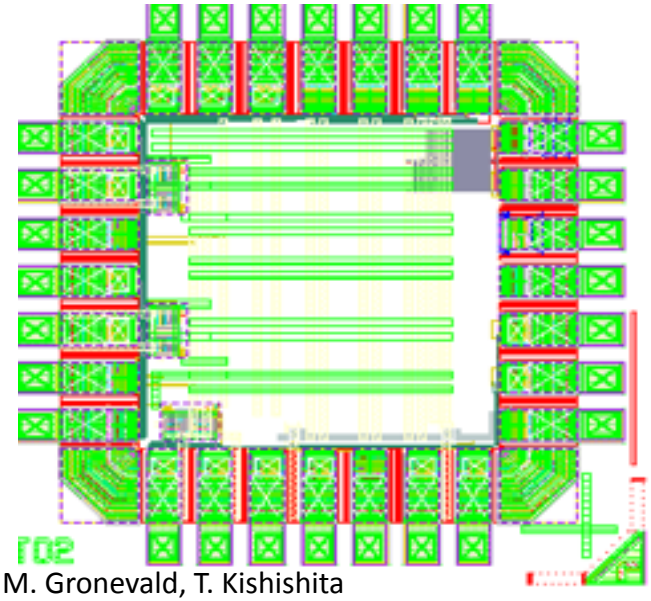
- Delay settings Ok
  - minimum delay setting (SW[1:0]=11 → 130 ps) shows best eye diagram for long cables
  - Possible optimization: make delay steps a bit smaller (170 ps → 120 ps, 7 → 5 inverter per delay)
- Bias current settings can be optimized
  - Recommended adjustments:
    - Increase main current (+ 5-10mA) → higher signal amplitude
    - Increase boost current (+ 4mA) → higher pre-emphasis level, better damping compensation
  - Current configuration
    - Current sinks: M2 (main bias) same size as M8 (boost bias), but M2 sinks 20 mA and M8 6 mA.
    - Ratio of main and boost switches is 3:1 (Ok)
- Good signal integrity driving 38cm kapton + 20m TWP cable @ 1.6Gbps
- No sensitivity for TID of 100 Mrad

DHPT 0.2

LVDS RX / TX

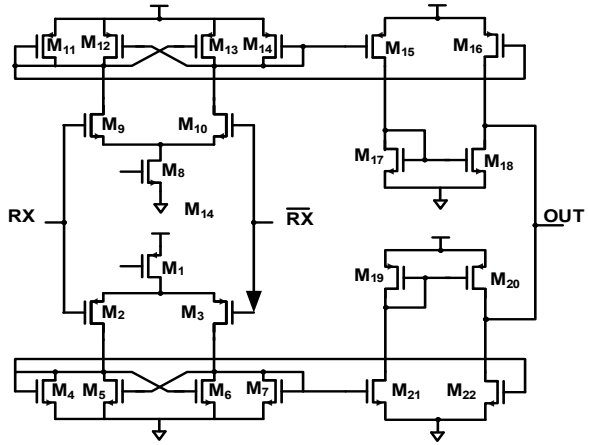
LVDS RX / TX



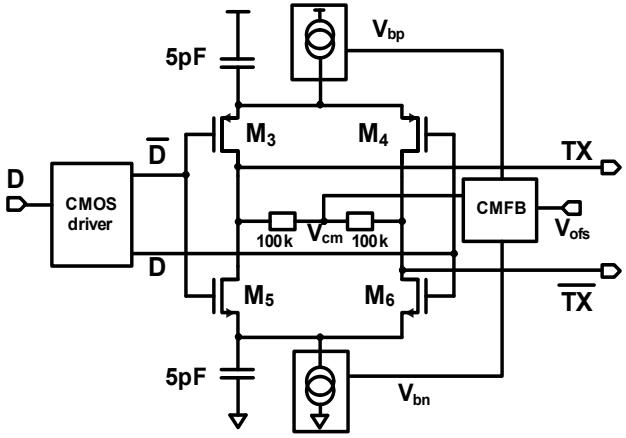
M. Gronevald, T. Kishishita

- **LVDS Reciver (1.8/2.5V)**
- **LVDS Transmitter (1.8/2.5V)**
- **Level Shifters 1.2V<->1.8/2.5V**
- **Custom IO (ARM compatible)**

LVDS Receiver



LVDS Driver



DHPT 0.2 – LVDS TX/RX Results

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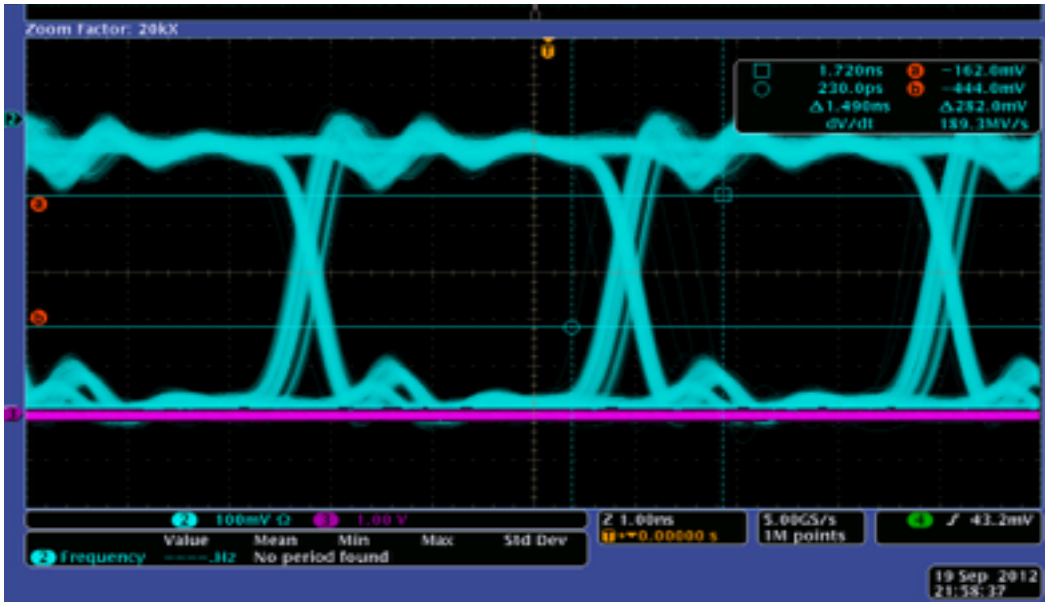
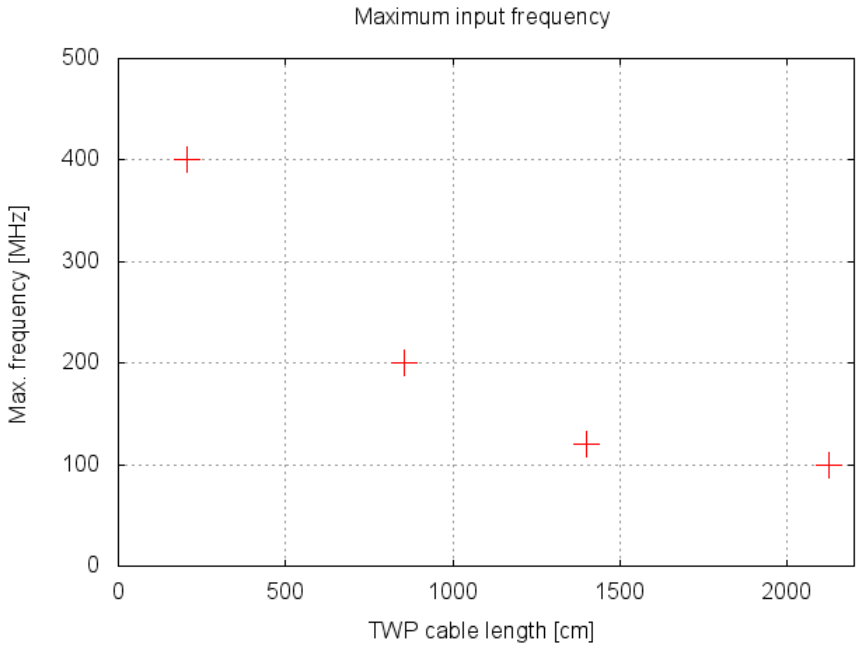
PRBS (2^7-1) @ 320MHz - VDD 1.2V/1.8V



Both receiver and transmitter work as expected.

DHPT 0.2 – LVDS TX/RX Results



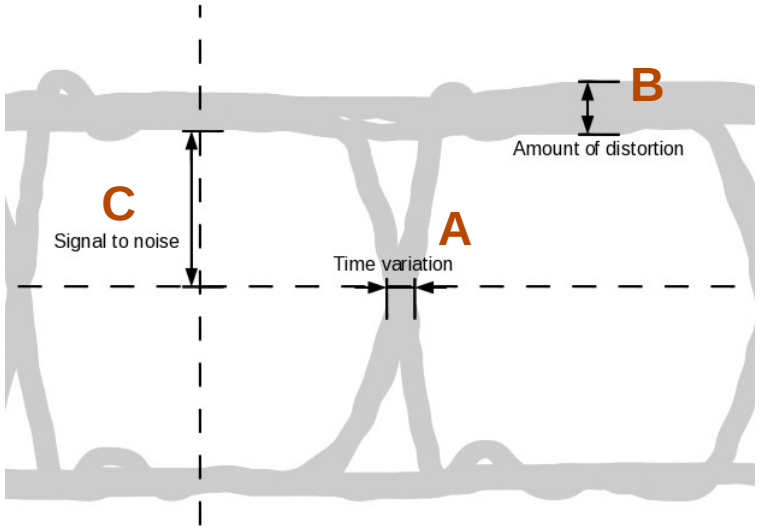


Figure: Measurement for Iref=150uA with V_{DD} = 1.33V

These values are lower thresholds for the max. frequency!!!

length [cm]	Max. frequency [MHz]	A [ps]	B [mV]	C [mV]
205	400	1010	212	128
856	200	2260	94	166
1401	120	2940	114	154
2125	100	2920	128	114

DHPT 1.0

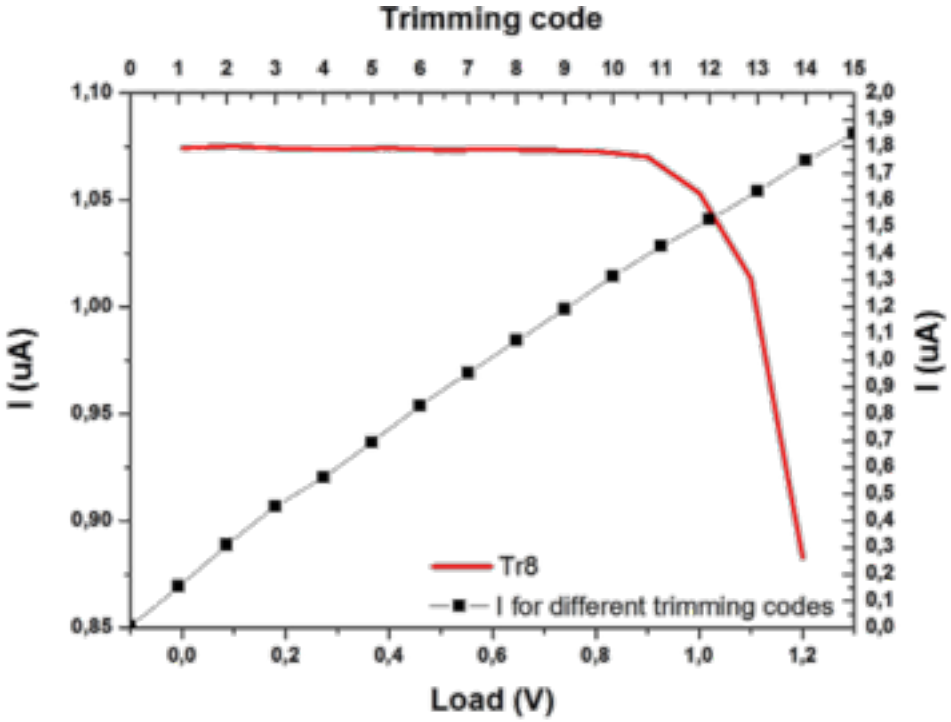
ANALOG BLOCKS

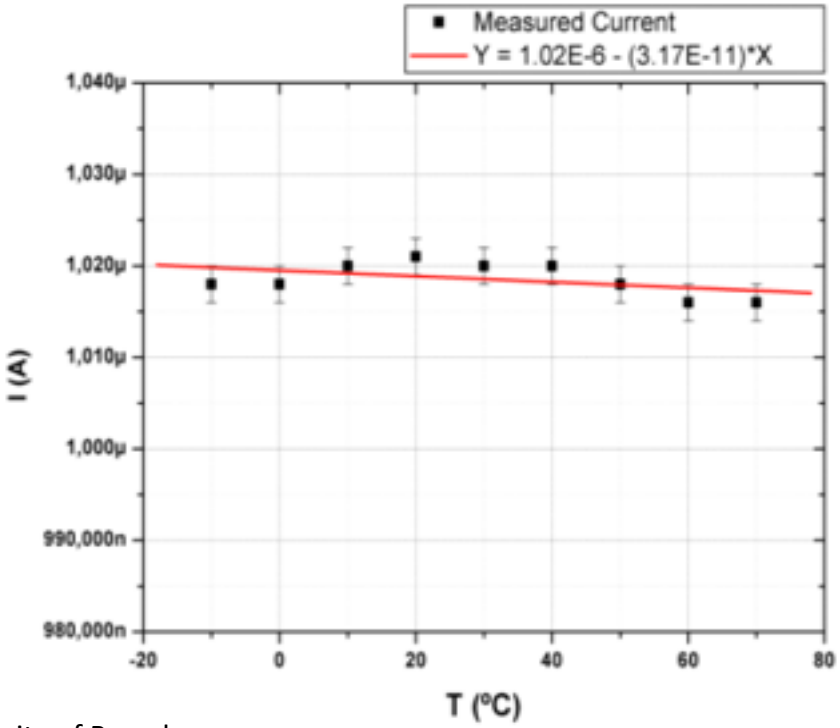
Analog Blocks – Current Reference (1uA)

Bias module provides 8 bias current to PLL, CML, and LDVS (each 1-255 uA with 8-bit DAC).

The core is Temperature Independent Current Reference (1uA)

- Compliance ✓
- Trim functionality ✓
- Temperature sensitivity ✓





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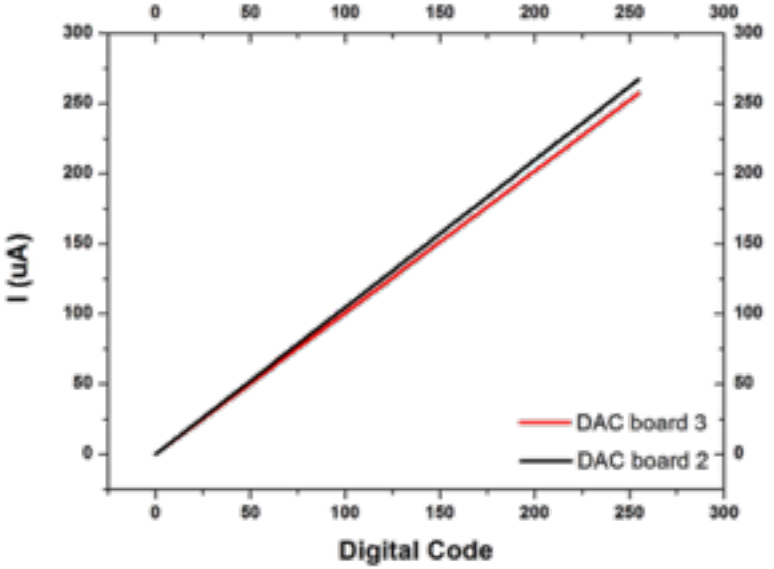
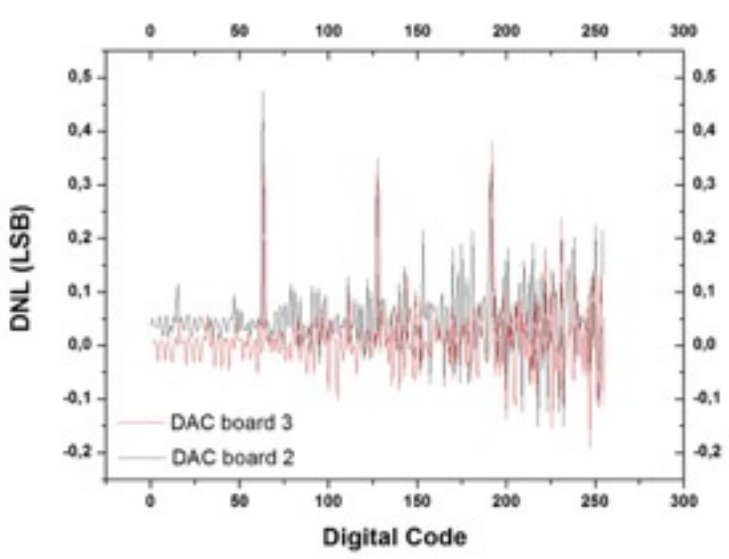
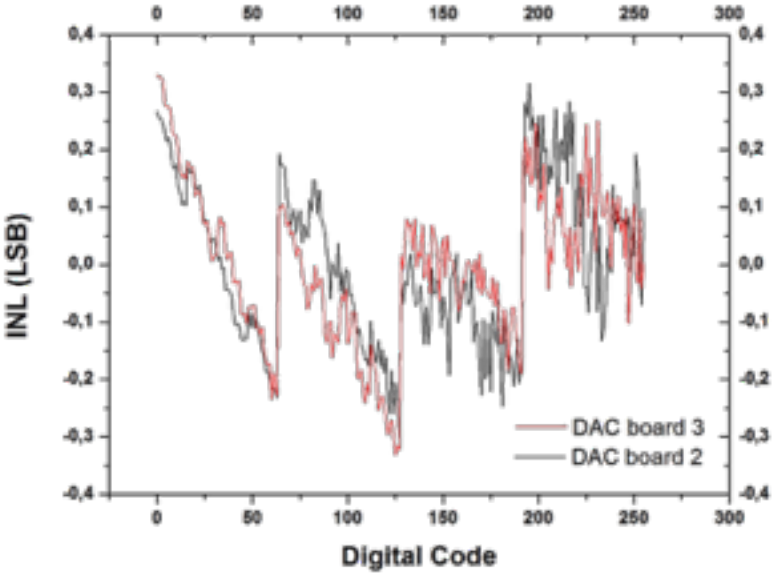
Analog Blocks – 8-bit DAC

8-bit DAC for bias current control (1-255 uA)

- Dynamic range ✓
- Linearity ✓



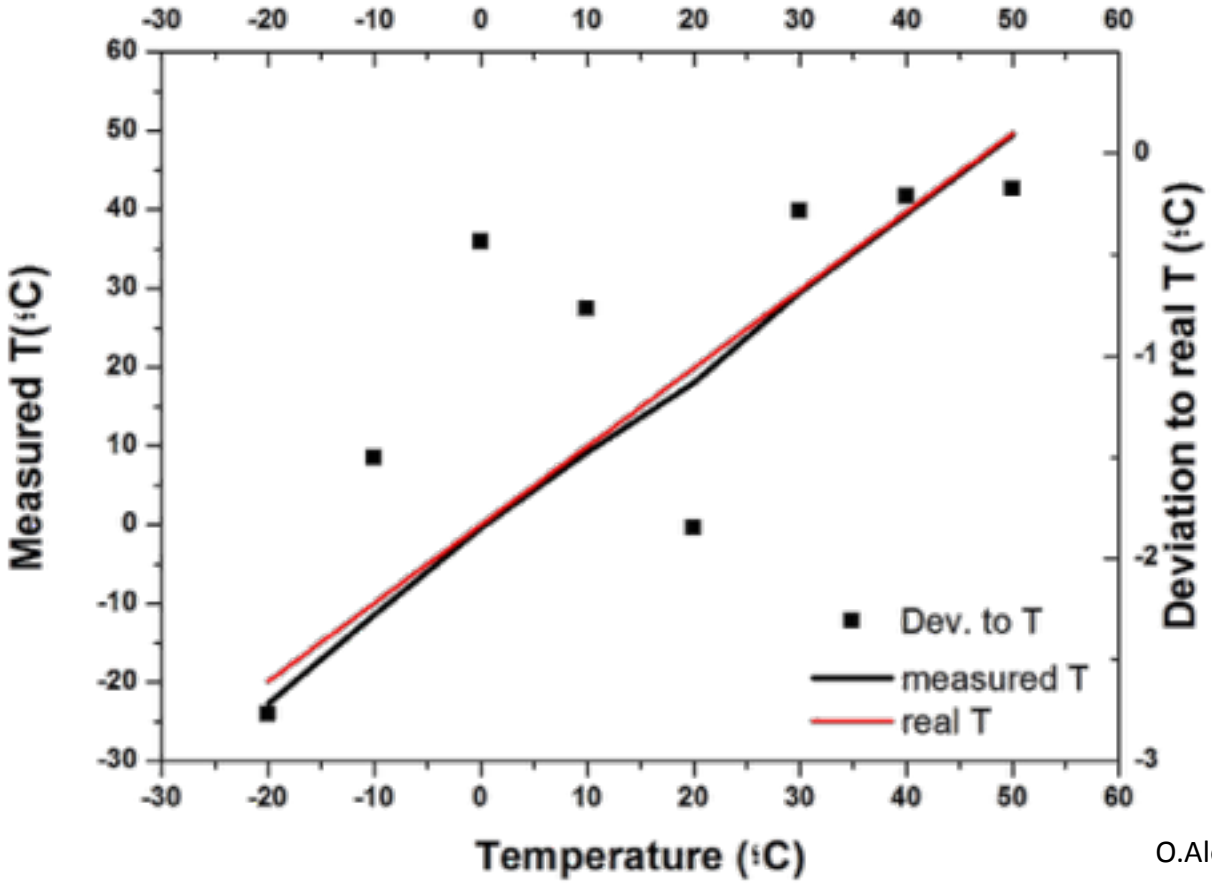




Analog Blocks – Temperature Sensor

Internal or external sensing diode + 16 bit Sigma-Delta ADC

- Measurement range -20°C ... +60°C ✓
- Accuracy ±1°C ✓



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DHPT 1.0

KNOWN ISSUES & LAYOUT IMPROVEMENT

✓ Serializer behaviors

✓ CML output swing

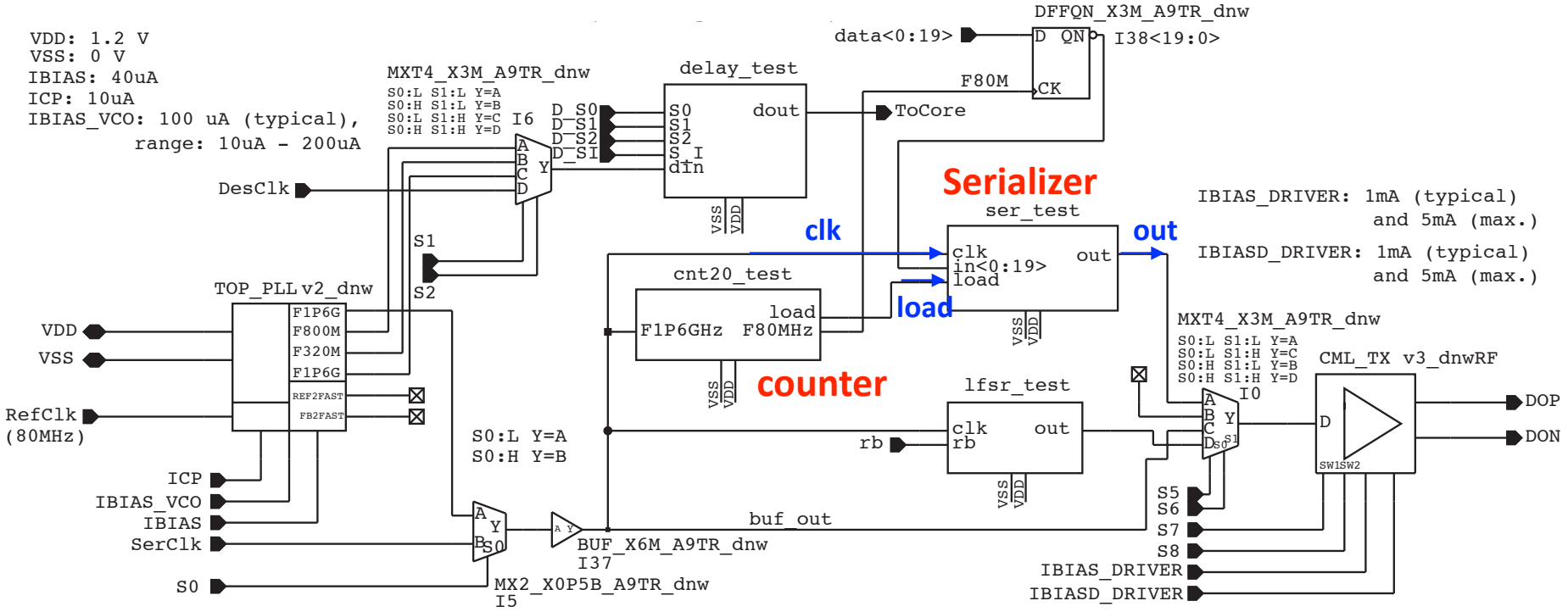
Serializer

- Serializer works, but VDD and/or GCK have to be adjusted:
  - GCK= 80 MHz → VDD= 1.6V (works but should not be applied for a long time)
  - GCK= 60 MHz → VDD = 1.4V (ok)
- Manufacturer test data ➔ wafer batch has „slow NMOS“ (too high threshold)

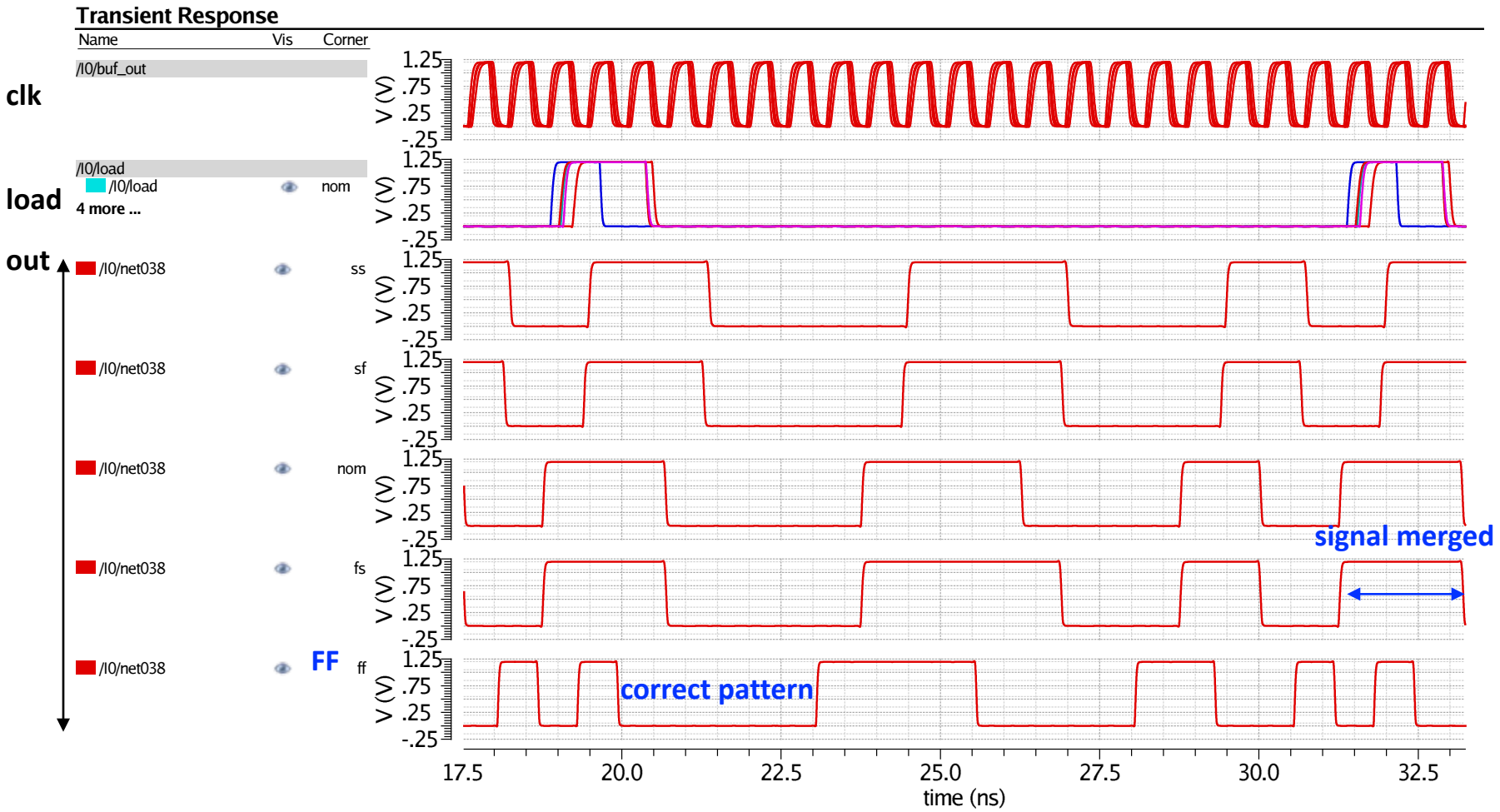
PARAMETER BY LOT:		SPEC LO	SPEC HI	MIN	MAX	MEAN	STD DEV
VTl_N4	(N/.3/.06/1)	0.300	0.490	0.368	0.490	0.423	0.029
Isof_N4	(N/.3/.06/1)	-1.400E-07	0.000	-8.958E-10	-3.833E-11	-2.339E-10	2.063E-10
Isat_N4	(N/.3/.06/1)	0.491	0.735	0.547	0.673	0.593	0.031

- Issue within the Serializer localized → can be fixed with a small design change

Schematic of the serializer

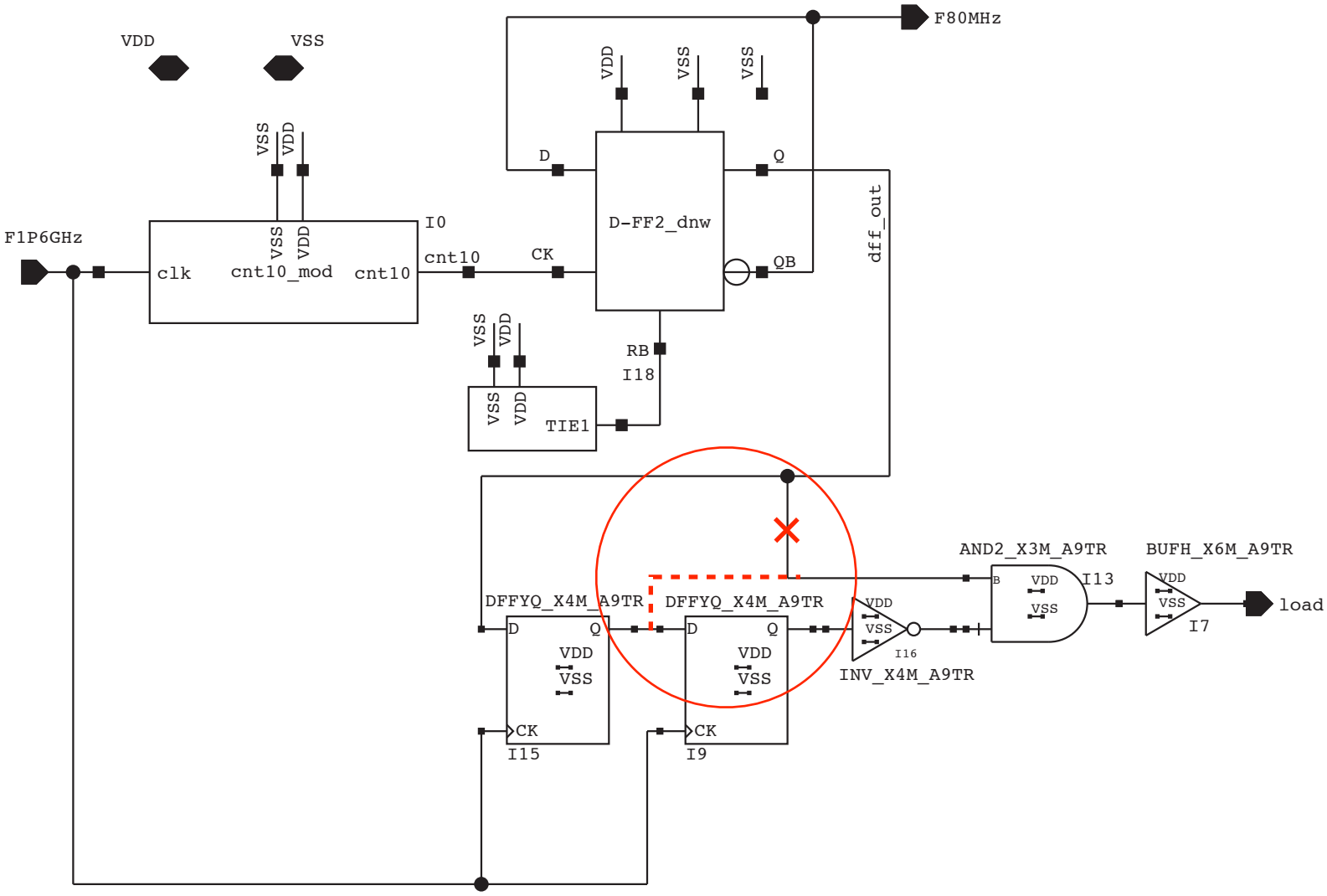


Simulation result

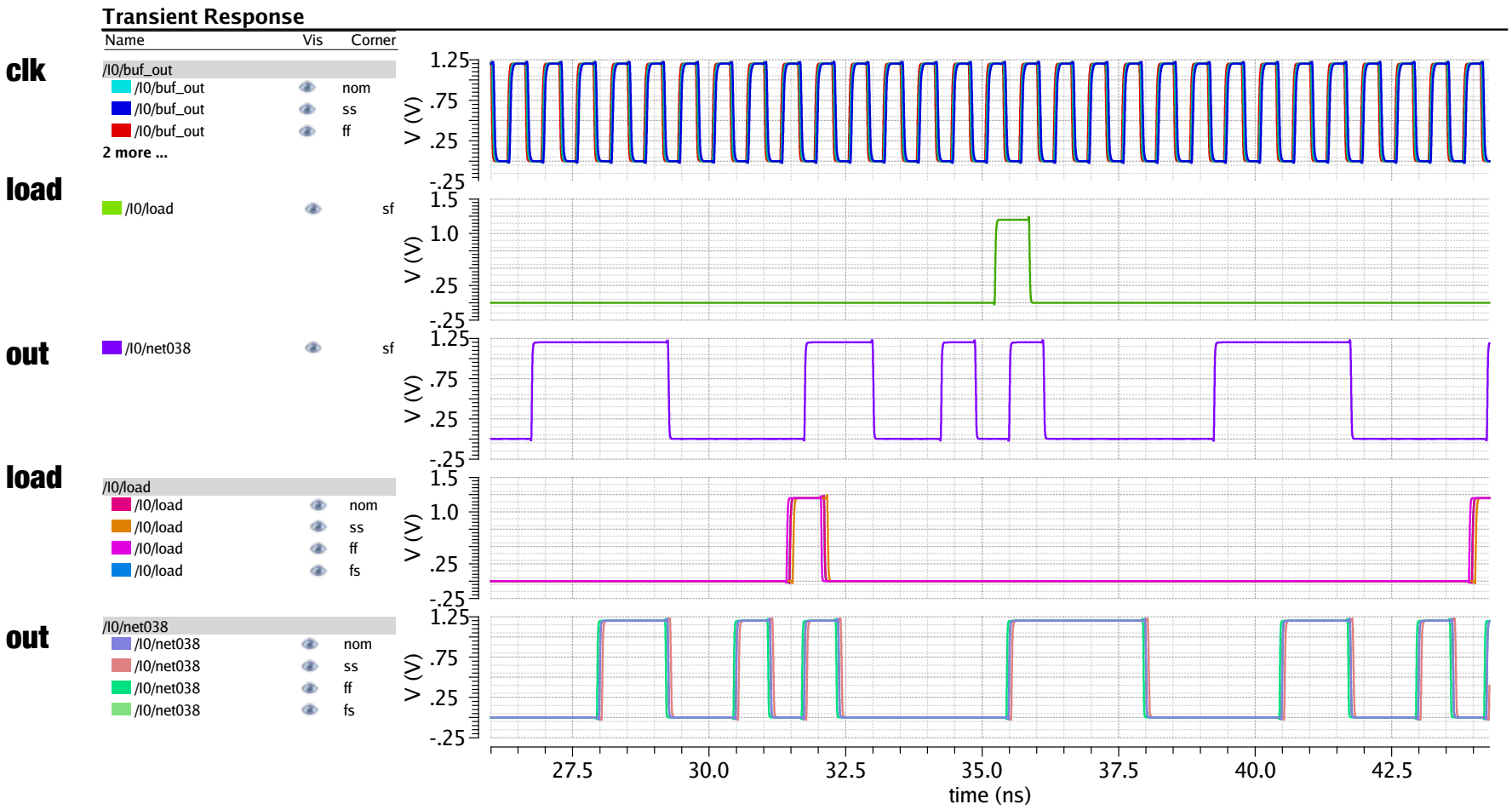


Timing of "load" is not provided correctly, except fast-fast corner.

counter circuit



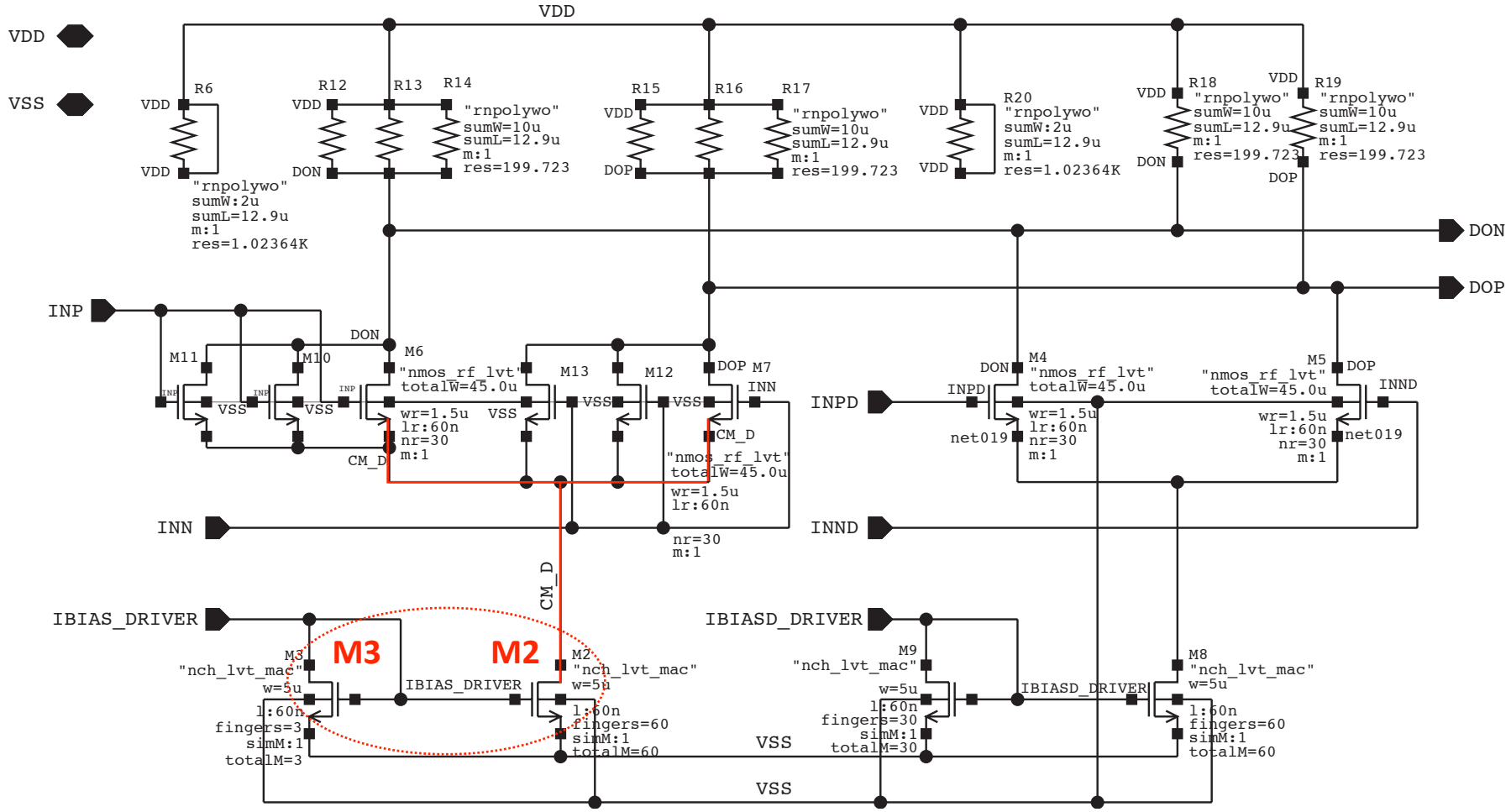
Simulation result (after modification)



Correct pattern can be obtained in all corners.

Schematic of the CML driver

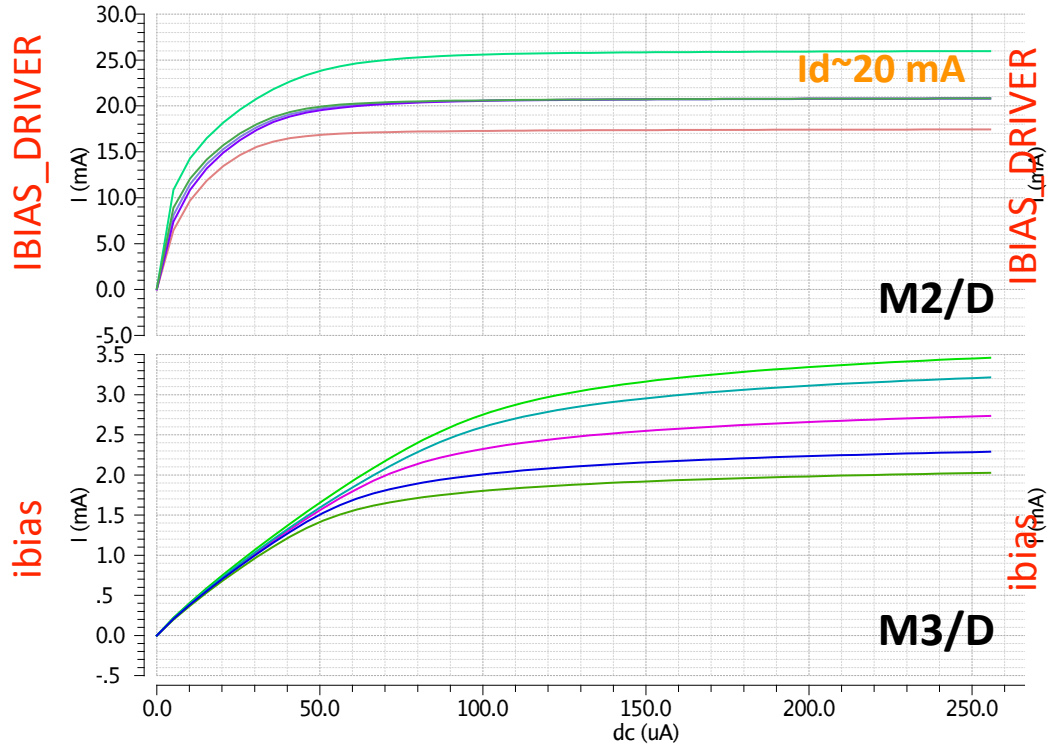
M2 is out of saturation with smaller bias current than expected.



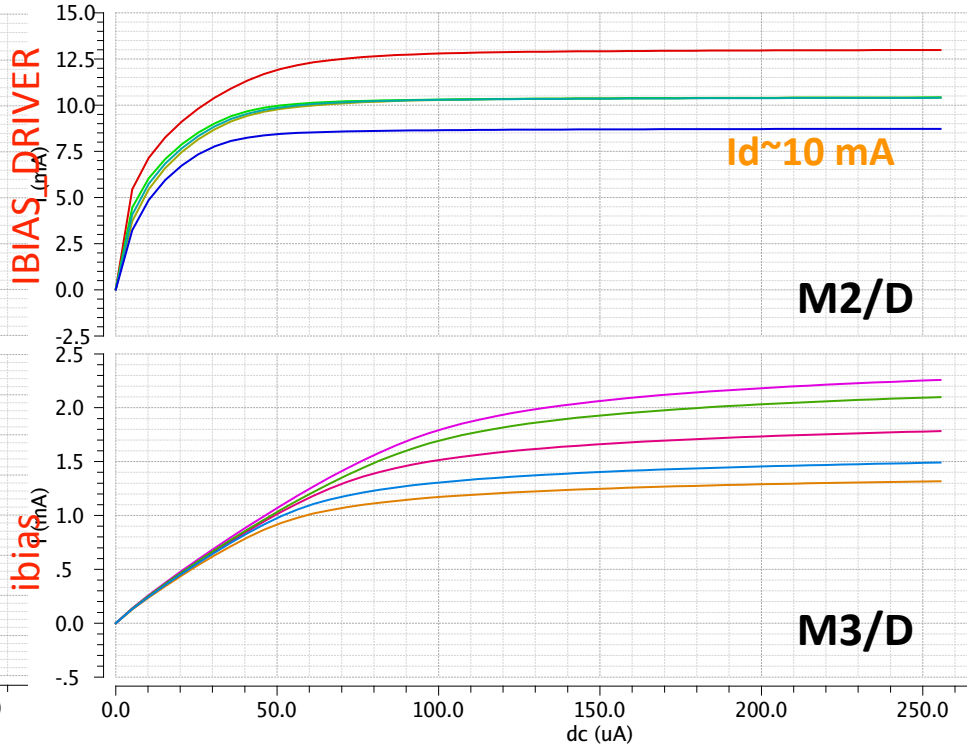
Simulation results

without any output connection

Schematic simulation (ideal)



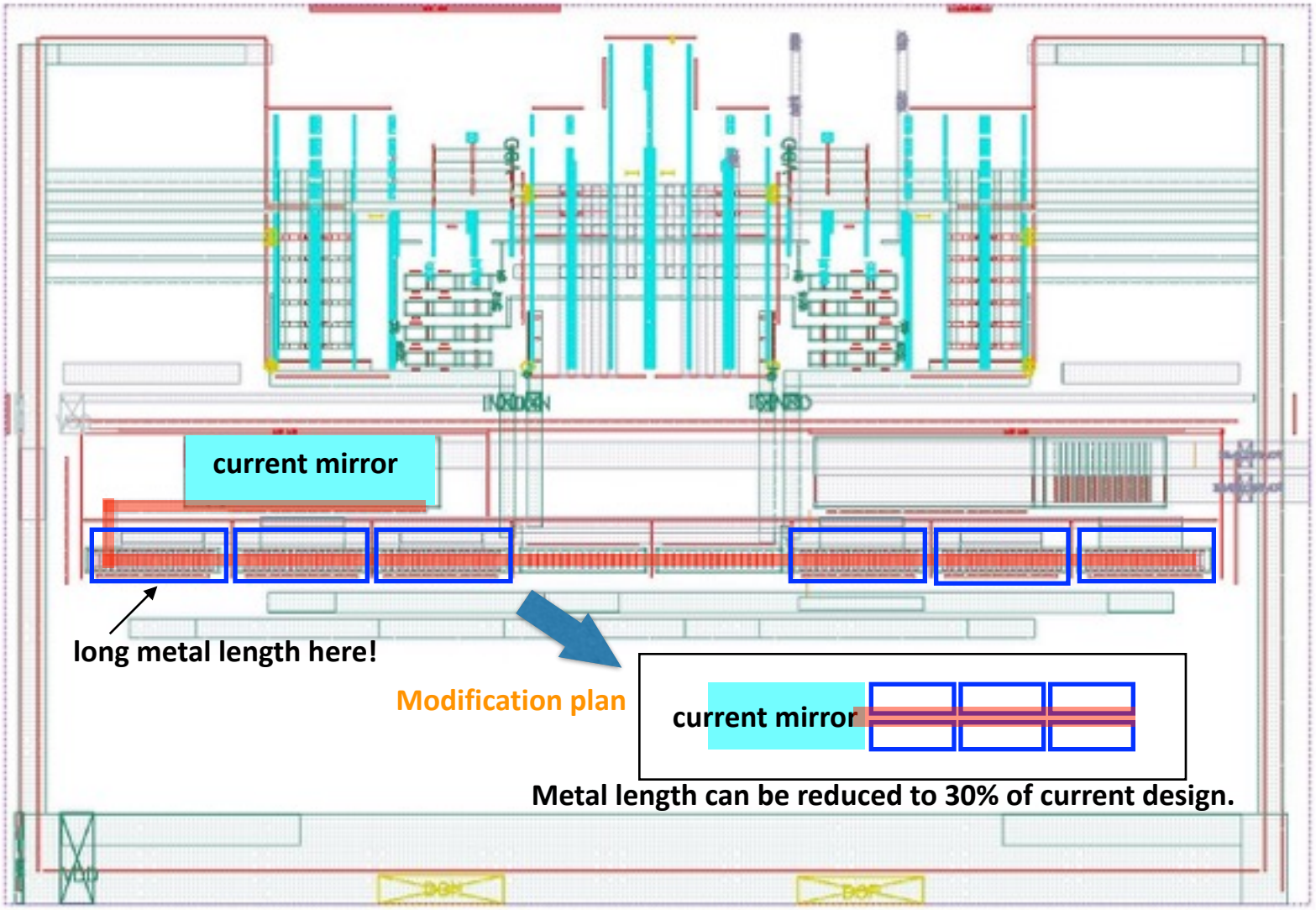
After parasitic extraction (realistic)



The difference comes from "voltage drop due to large serial resistance" between current source and switching transistor.

Layout can be improved in the next submission. The ideal output swing is two times larger.

Modification plan



Output swing will be improved at least 50%.

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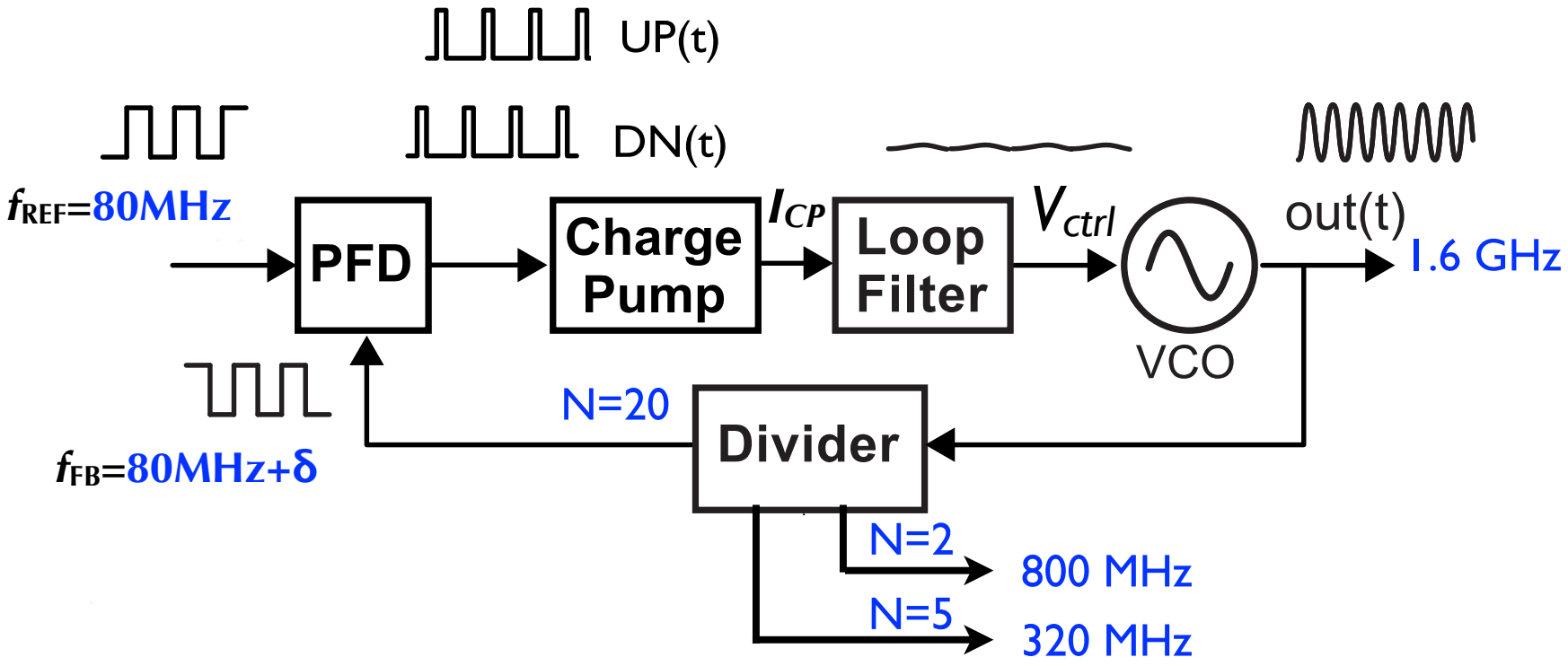
Thank you very much.

SCHEMATIC DETAILS (BACKUP)

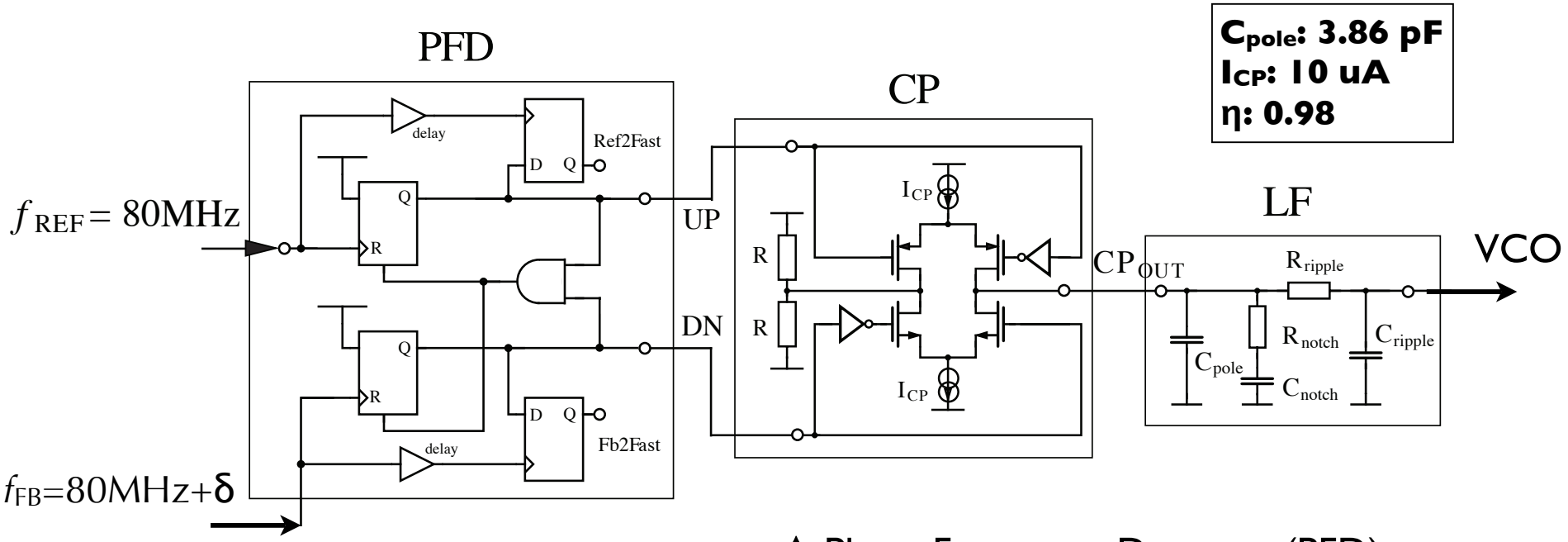
Overview of PLL architecture

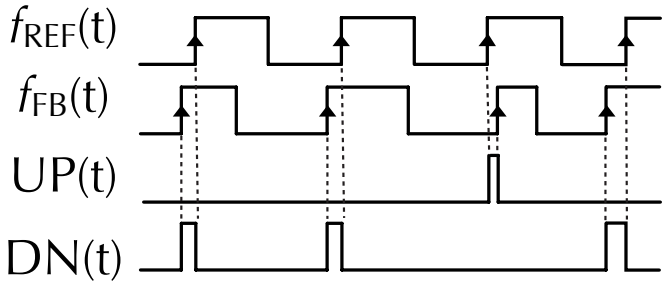
PLL generates 1.6 GHz from 80 MHz reference clock.

- ✦ Voltage Controlled Oscillator (VCO) provides oscillating waveform with variable frequency
- ✦ PLL synchronizes VCO frequency to input reference freq. through feedback
- ✦ Use digital counter structure to divide VCO frequency



PFD, Charge pump, and Loop filter

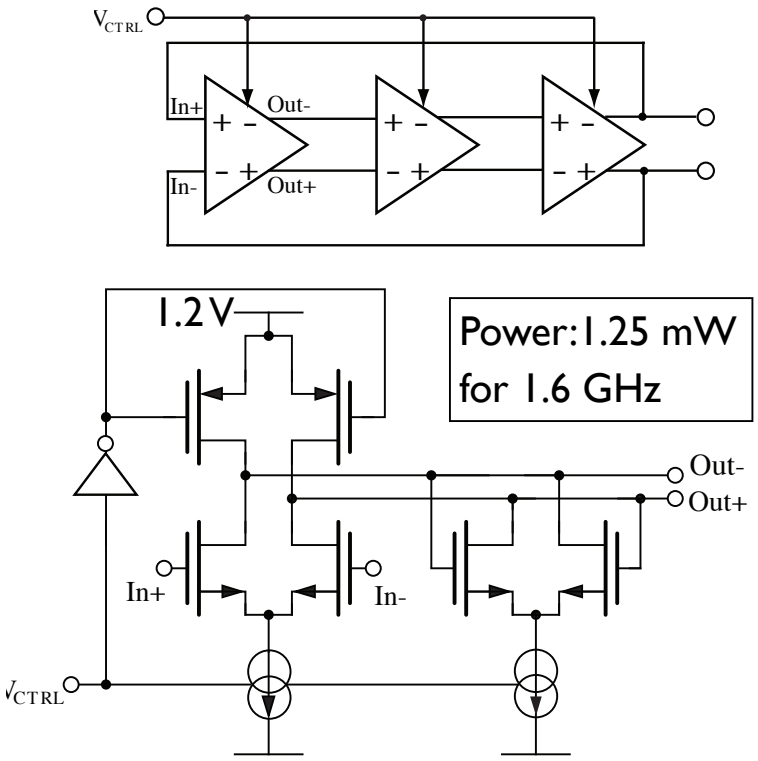




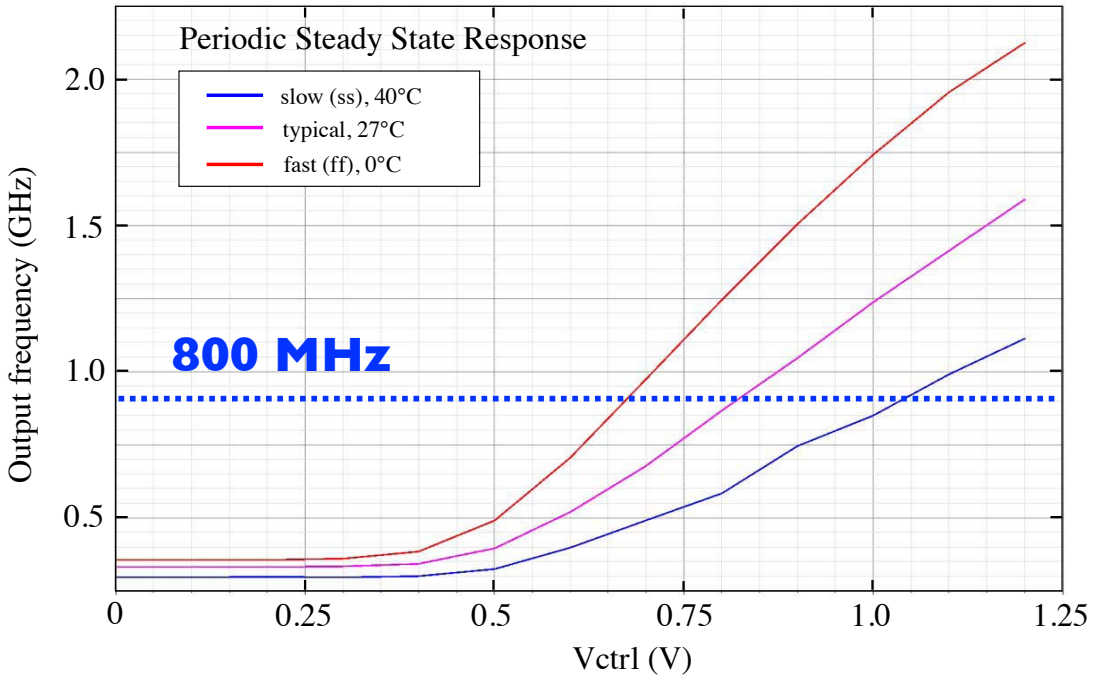
- ✦ Phase-Frequency Detector (PFD): classical two flipflops structure, additional error detection circuit
- ✦ Charge-pump (CP): differential structure with dummy branch
- ✦ Loop-filter (LPF): MIM structures, well-tuned parameters for PLL stability

Voltage-Controlled Oscillator (VCO)

- three inverters connected as a ring oscillator
- differential pairs with PMOS loads with cross-coupled stages for rail-to-rail switching



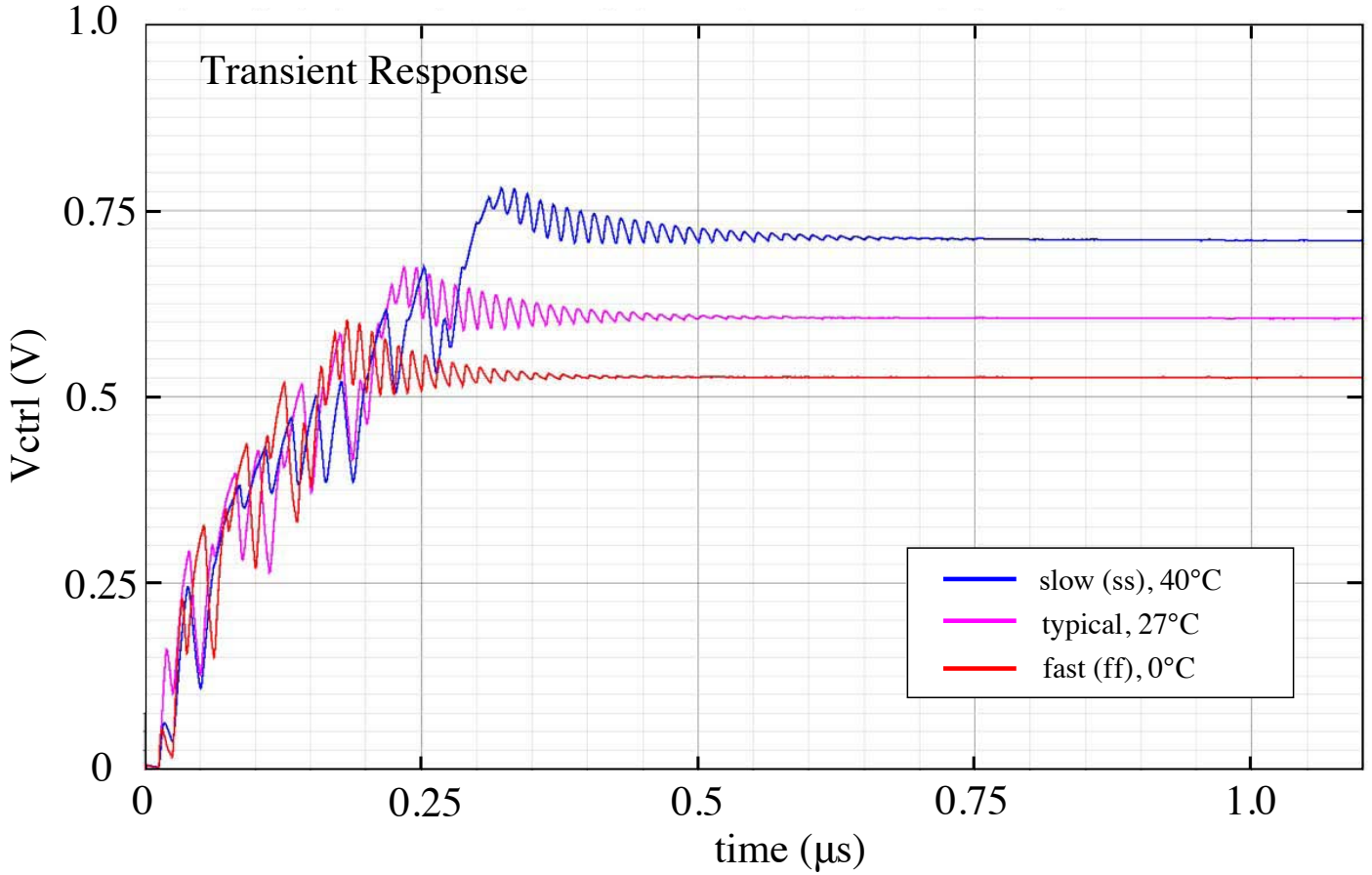
[800 MHz vs. Vctrl]



- wide tuning range of the output frequency
- oscillation freq. of 1.6 GHz is secured under 3σ process variations.

PLL Settling Behavior

- The V_{ctrl} settles to the final value in t_{settle}~750 ns within accuracy of 2%.
- Stable behavior for all process corners.
- Layout parasitics are included in the simulation.



CML driver with pre-emphasis

- Differential current mode logic (CML):

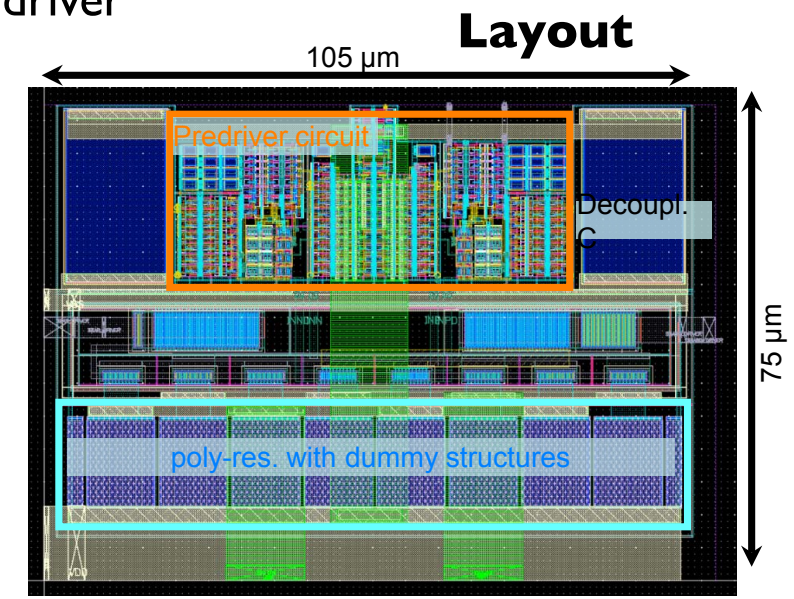
  driver (phase control) + differential pair post driver

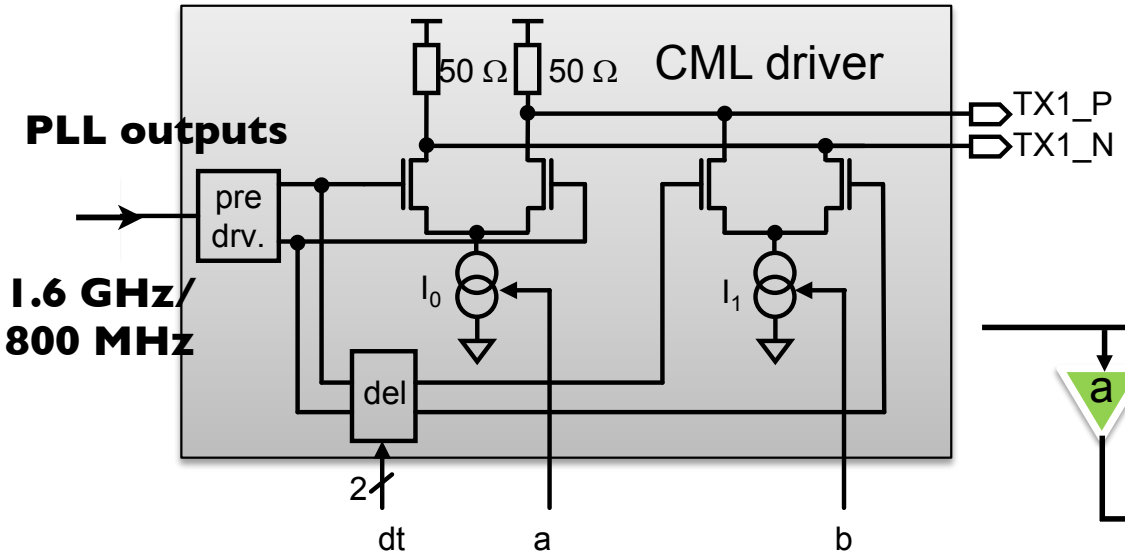
- Two differential pairs: adj. bias currents:

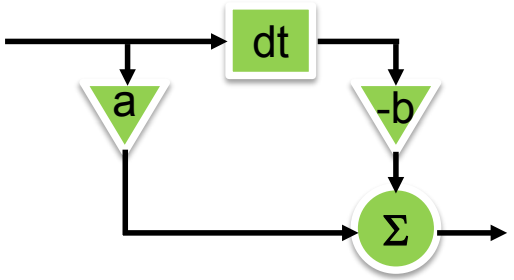
  - tap weights (a & b),

  - delay (dt) upto 600ps with 4 fixed steps

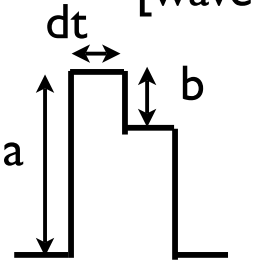
- Dummy poly layout for impedance matching



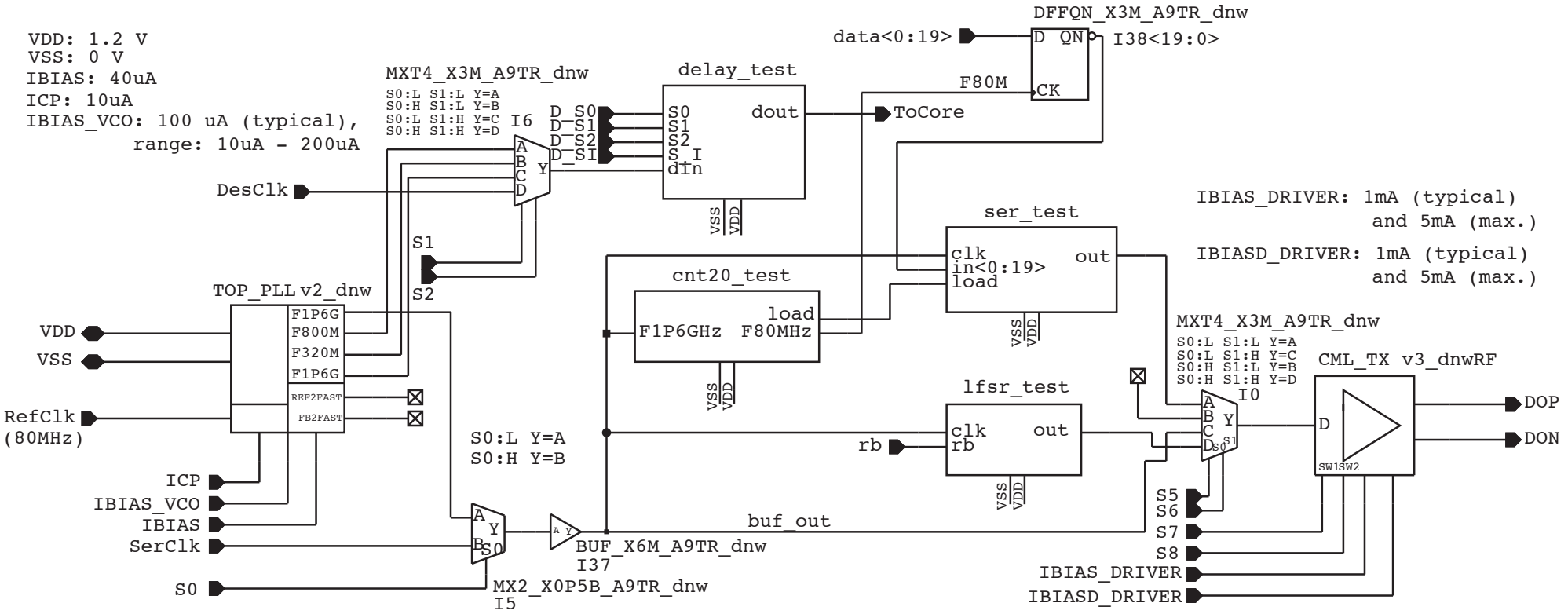




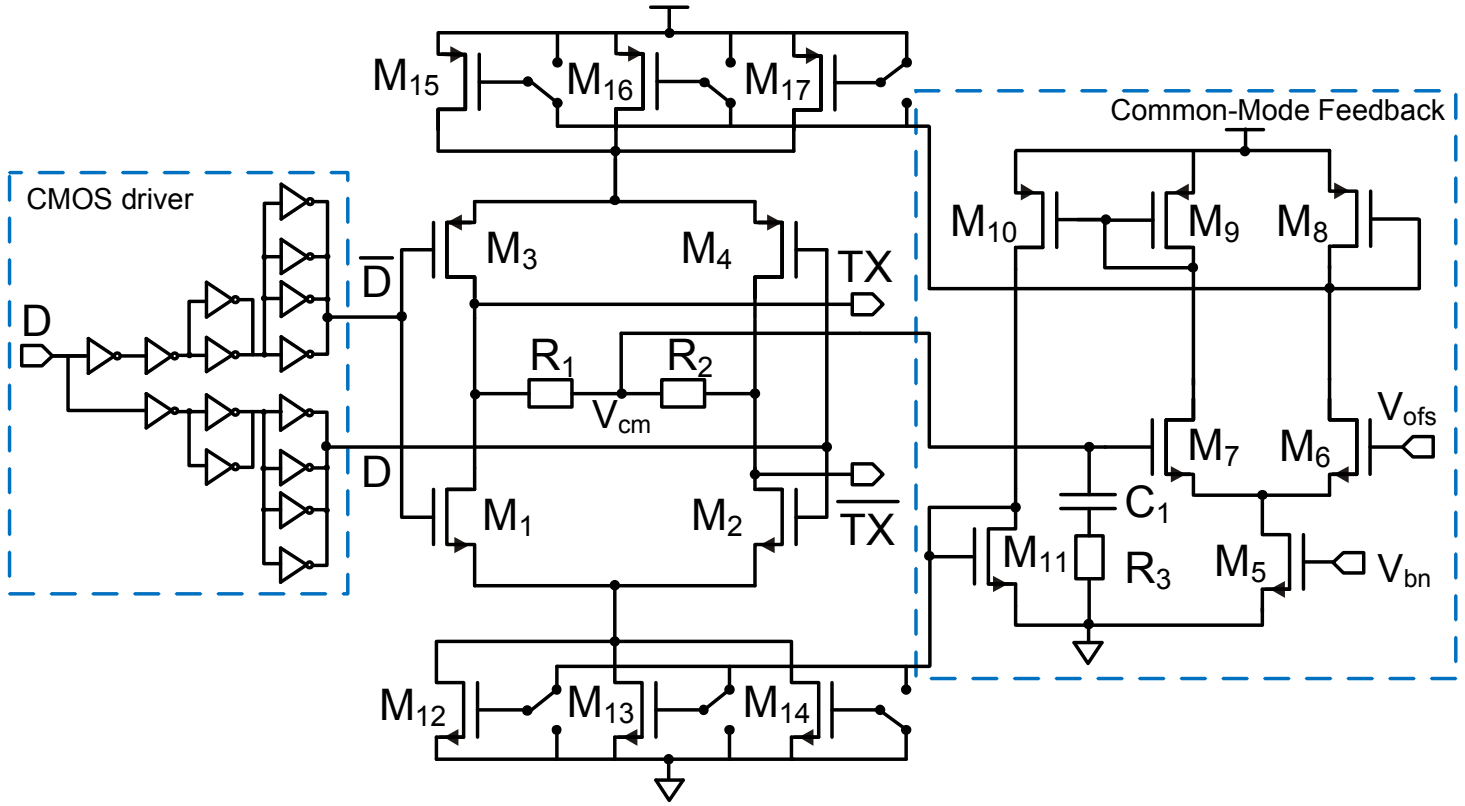
[waveform]



PLL+Serializer+CML

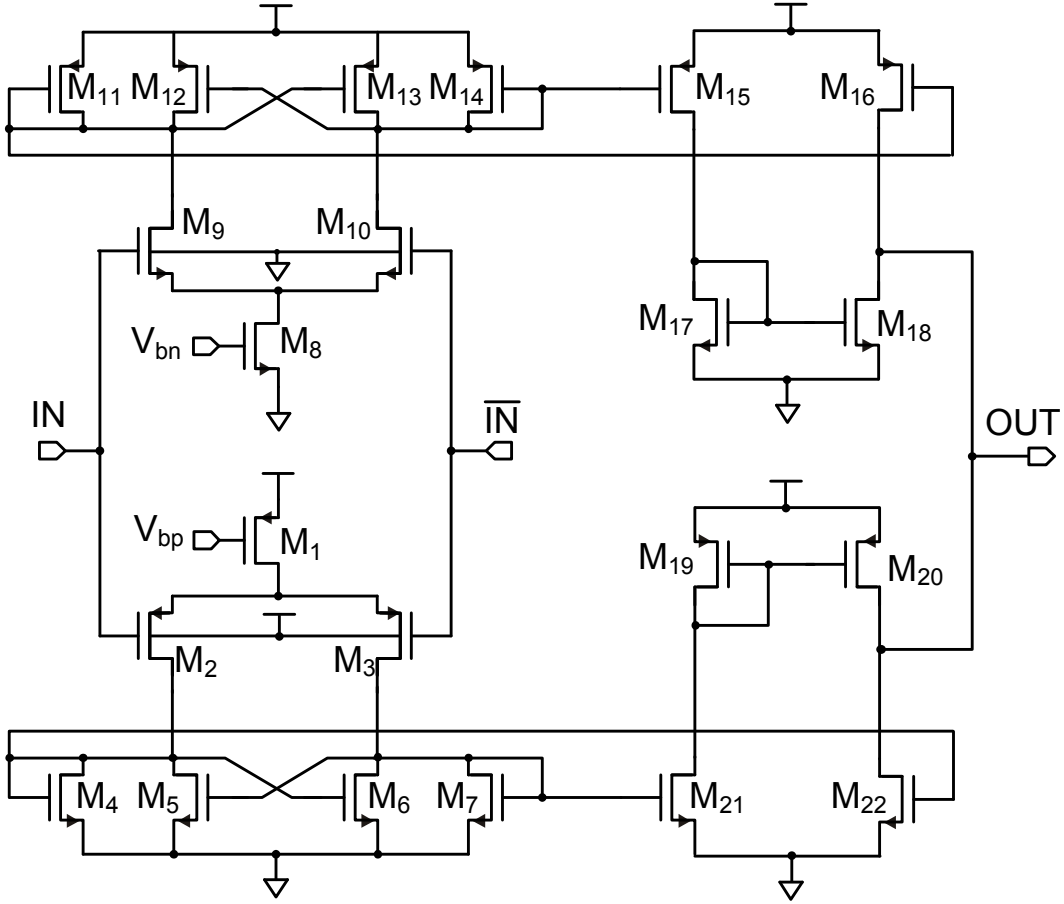


LVDS TX



- ✓four switching transistors with common-mode feedback circuit.
- ✓adjustable signal current from 0.6—3 uA.
- ✓100 Ohm termination resistors are implemented with poly-resistors.

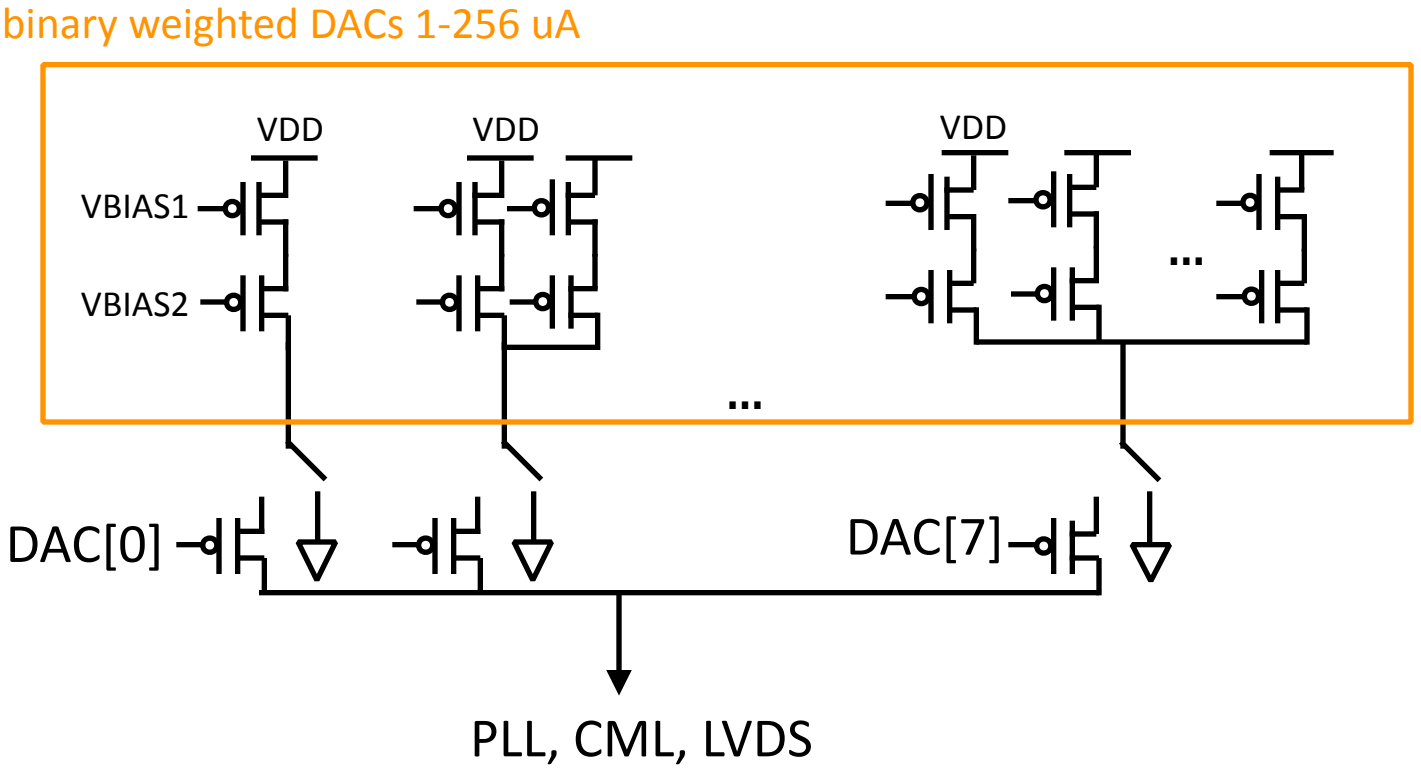
LVDS RX



- ✓NMOS & PMOS diff. pair for wide common-mode input range
- ✓positive feedback circuit M4~M7, M11~M14 for higher speed and hysteresis.
- ✓high-gain 2nd-stage amp. for full CMOS output

BIAS_MODULE

It provides 8 bias currents to PLL, CML, and LVDS.
An 8-bit current-steering DAC provides a programmable current (1 to 255 uA).



Temperature sensor (designed by UB)

universitätbonn

✓ Operating temperature of -20℃~70℃, with ΔT=0.2℃ accuracy.

✓ based on Voltage Proportional To Absolute Temperature (VPTAT) method.

✓ drop voltage of the diode is digitalized by ΣΔ-ADC and temperature.