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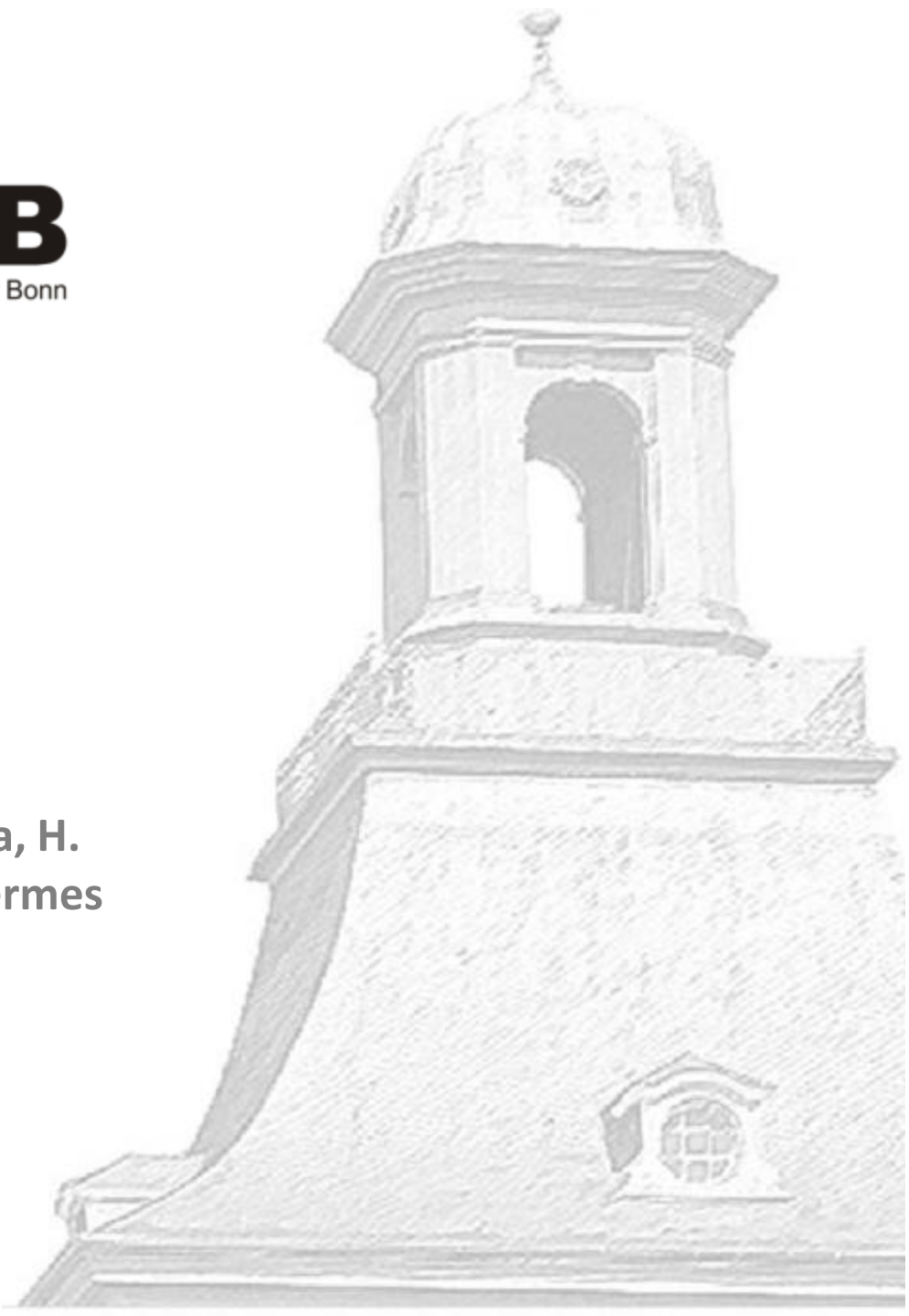
Silizium Labor Bonn

DHP

L. Germic, T. Hemperek, T. Kishishita, H. Krüger, F. Lütticke, C. Marinas, N. Wermes
University of Bonn



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The DEPFET Ladder

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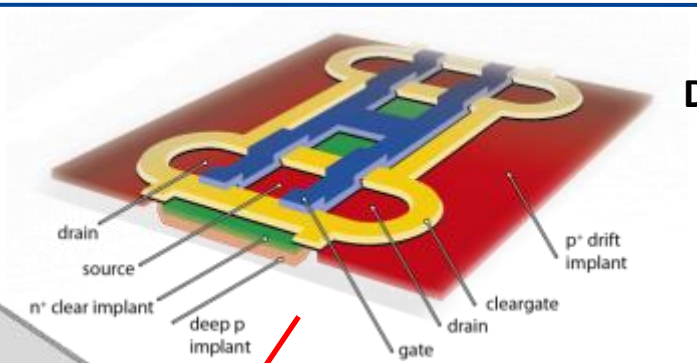
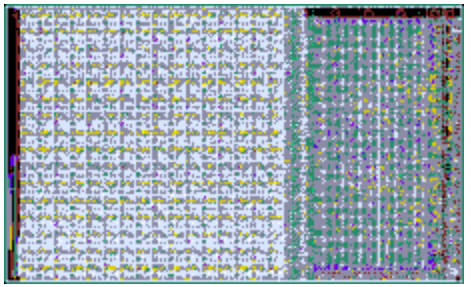
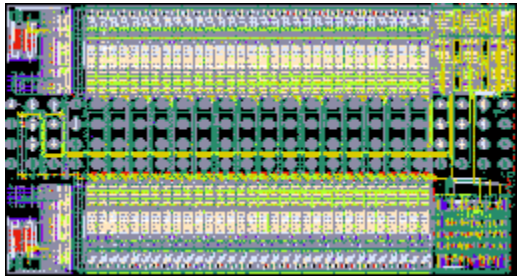


DCDB (Drain Current Digitizer)
Analog frontend



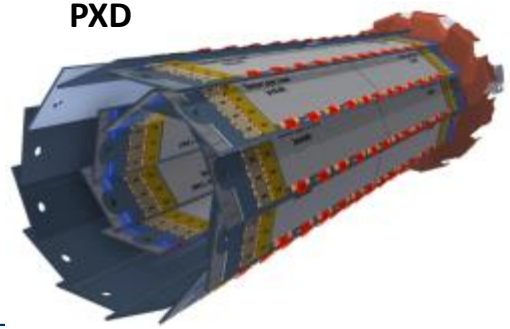
UMC 180 nm
Size 5.0×3.2 mm^2
TIA and ADC
Pedestal compensation
Rad. Hard proved (20 Mrad)

SwitcherB
Row control

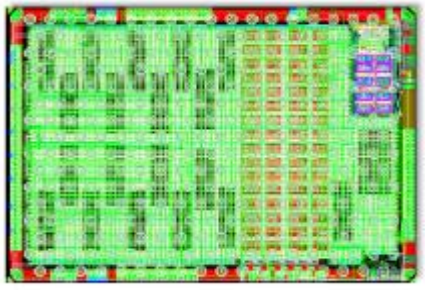


AMS/IBM HVCMOS 180 nm
Size 3.6×1.5 mm^2
Gate and Clear signal
Fast HV ramp for Clear
Rad. Hard proved (36 Mrad)

PXD



DHP (Data Handling Processor)
First data compression



TSMC 65 nm
Size 4.0×3.2 mm^2
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation
Rad. Hard proved (100 Mrad)

DHP

The DHP is a digital chip used to reduce data rates produced by the DCD

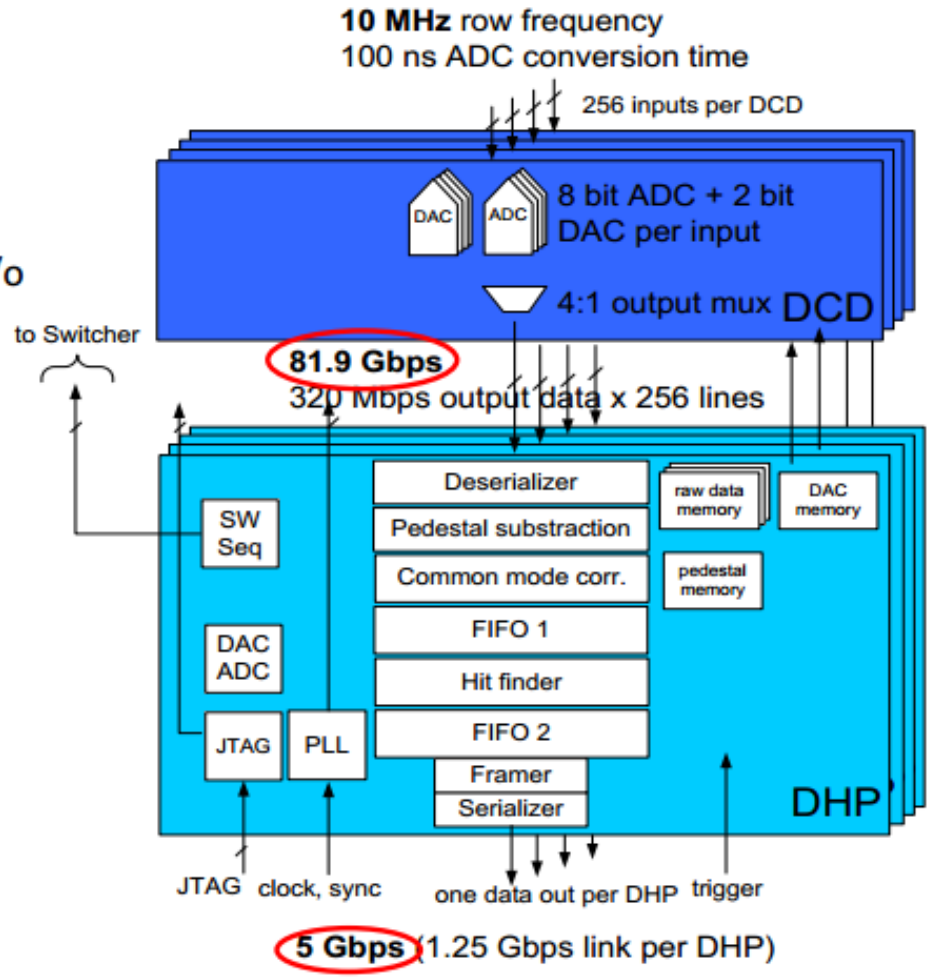
To do the data reduction, the DHP does:

- Data pre-processing: triggered frame selection, pedestal subtraction, common mode correction and zero suppression.
- Serial formatting to send the data to the DHH through a specially designed current mode logic serial link.
- Correct for pedestal spread sending the offset sequence.
- The DHP is responsible for the control sequence generation for the Switcher-B chips chain, thus steering the matrix.

DHP Functional Overview

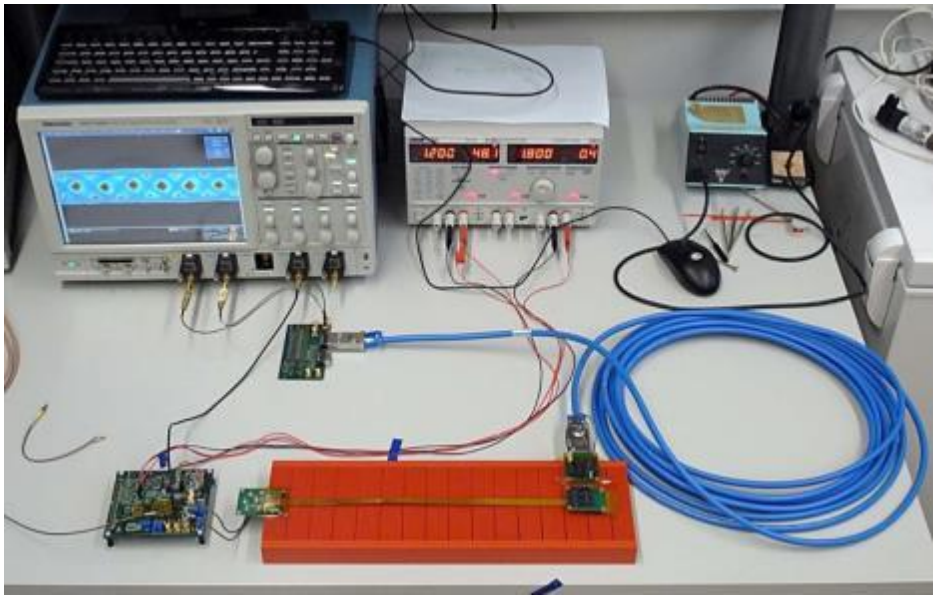
- Functionality
  - Module controller
    - JTAG bus to DCDB and SWITCHER chips
    - Clock & timing generation & distribution
  - Data reduction (1/20): 0-suppression, triggered r/o

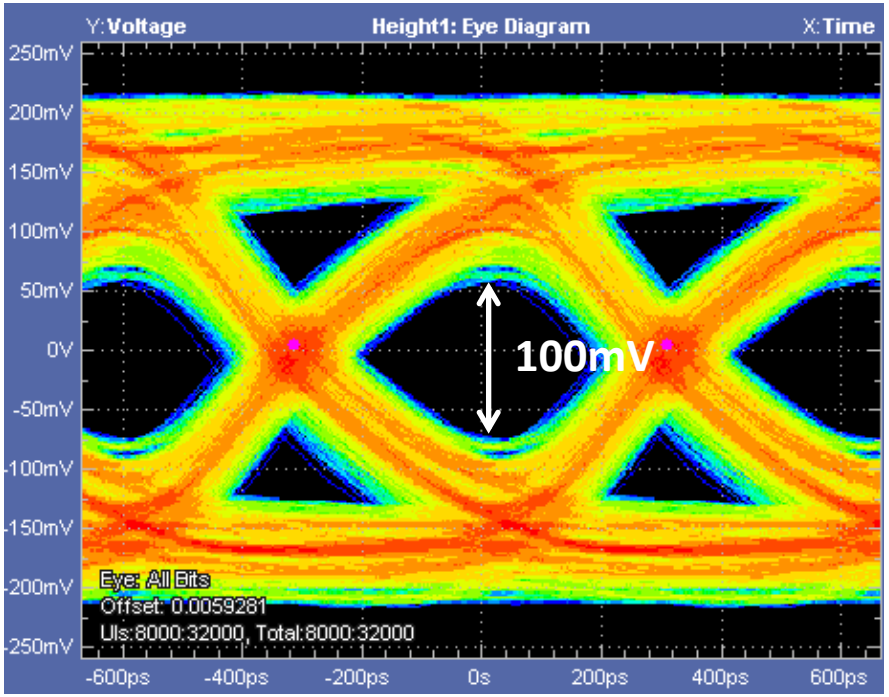
- Data processing details
  - Raw data buffer
  - Common mode (two pass)
  - Fixed pattern noise correction (static pedestals)
  - Hit finder (FIFO1 + FIFO2)
  - Framing (AURORA)
  - Serializer + Gbit link driver



DHP Functionality

- Data processing
- SWITCHER sequencing
- Inter-chip communication
- Serial link

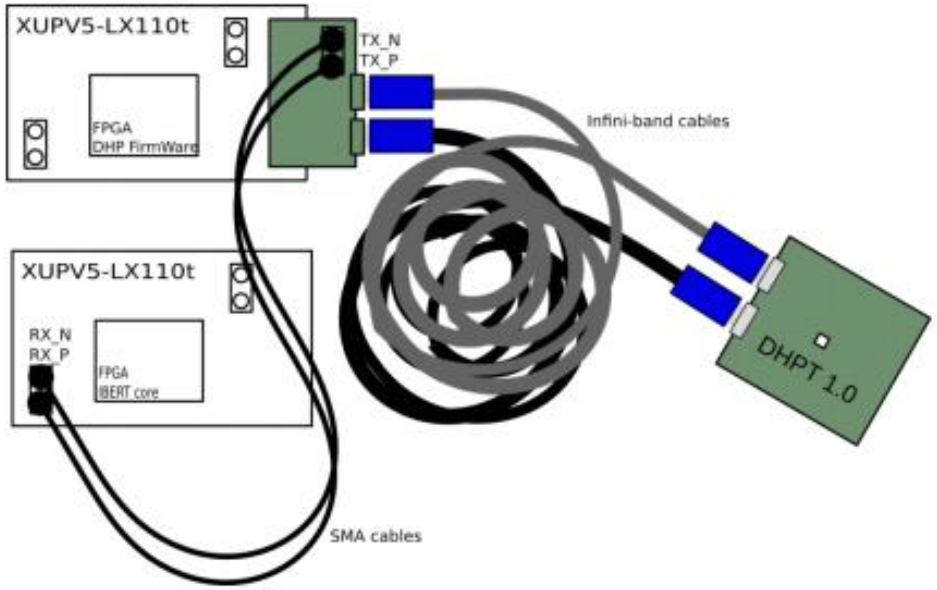


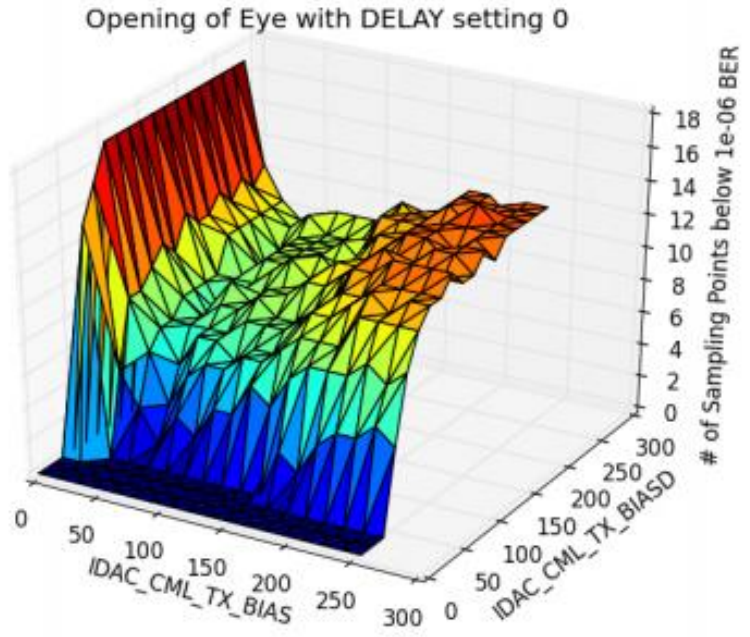


Irradiated (100 Mrad) DHPT 0.1, can drive 20 m of Infiniband cable

BER Tests

- Error rate tests and parameters optimization for designed 15m cables





Parameter optimization for 15m data cable

Optimal Working Point

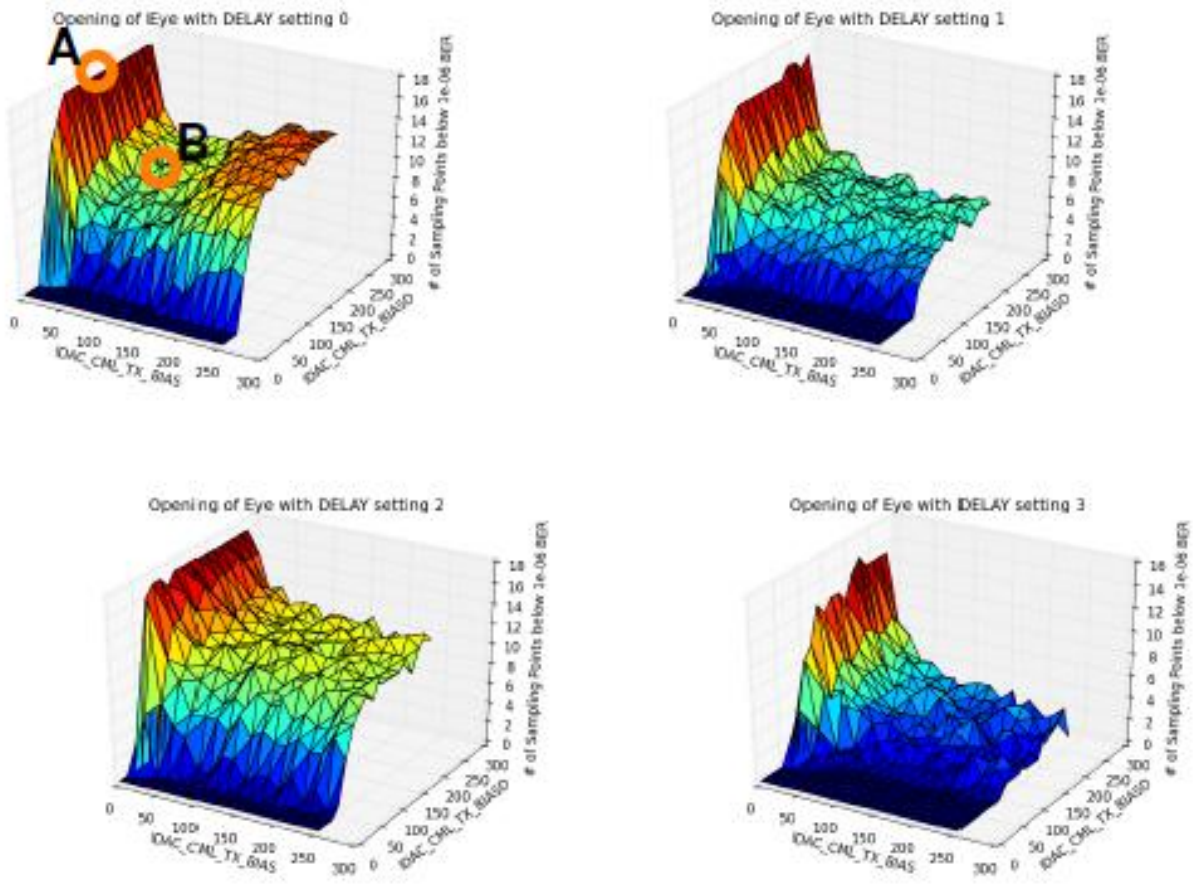


Figure: Sweep results at a threshold of $BER_{thr} = 10^{-6}$. Higher is better - wider opening at BER_{thr}

Status of the Funcional Verification

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	IP Block / Task	Status	Comment
Custom IP	Gbit Link Driver	✓	
	PLL / Serializer	(✓)	Works with adjusted VCC / CLK freq.
	Temperature Sensor	✓	
	LVDS IO	✓	
	Interface DHP-DCD	TBD	Need new WB adapter (LVDS DCDCLK)
	Interface DHP-Switcher	(✓)	Gated mode operation not verified yet
	Bias DAC, Current reference	✓	
Data Processing	Command Interface (Manchester encoded)	✓	
	Memory Access (via JTAG)	✓	
	Data Processing: Channel Masking	TBD	
	Double Precision Common Mode Processing	✓	
	Overflow Handling	TBD	

- **Fix serializer (small change in the schematic/layout)**
- **Improve CML AMPLITUDE**

Plans

- Hybrid 5.0:
  - Tests communication DCD ↔ DHP
    Irradiation, temperature, 2b DAC, timing and phase alignment

  - Assembly planned within the next 4 weeks
  - Tests to be finished by March

- EMCM:
  - System related aspects
    Link stability and parameter optimization

Motivation

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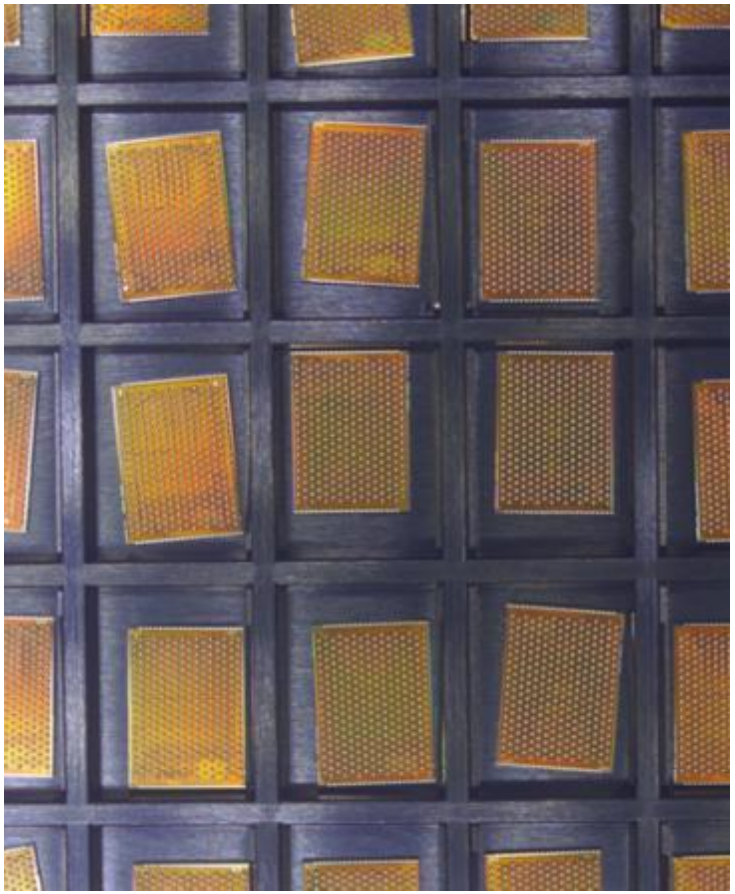
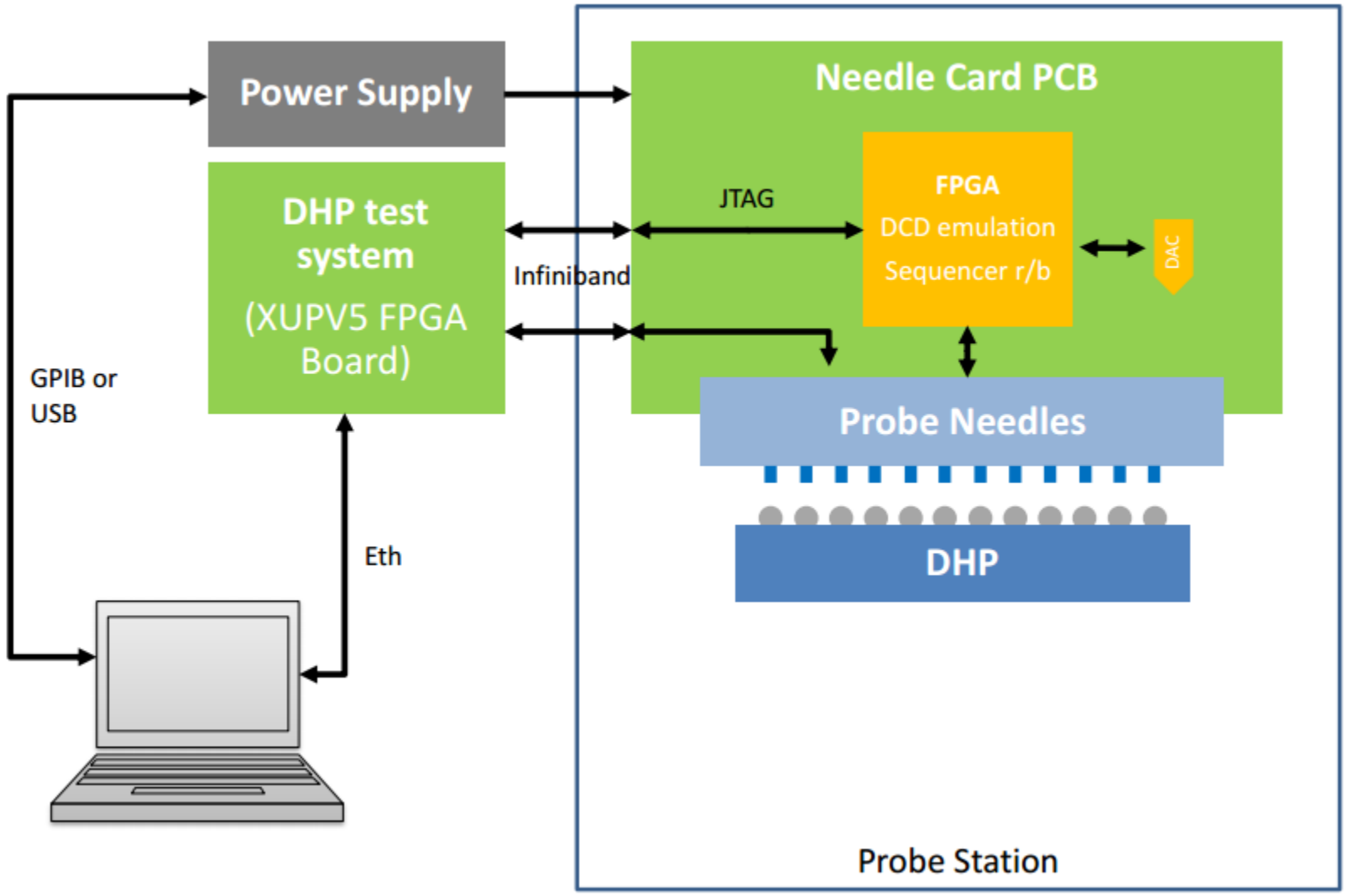
- PXD modules a sensitive to single-point-of-failure of the DHP
- We had very little statistics of the DHP yield (limited to wire bond adaptors)
- Need to qualify the chips before flip-chip mounting
- What do we do in terms of QC on the DHPs?
- How do we make sure the chips delivered are OK for mounting on the PXD?



DHP Chip Probe Test System



Probe Station Setup

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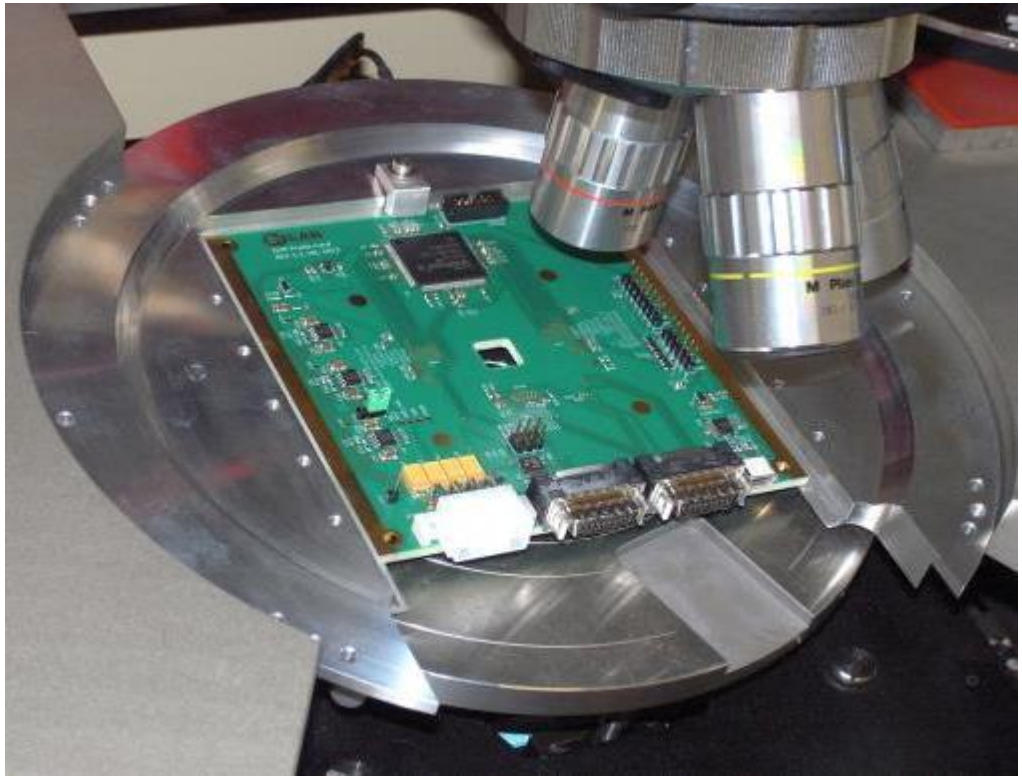
- Needle card fixture
- We have diced chips only
  - Put single chips on chuck (Ok for now)
- External components:
  - Power supply

  VDD = 1.2 V, VDD_CML = 1.2 V and DVDD = 1.8 V
  - Xilinx XUPV5 Evaluation Platform (DHHemulator)
  - 1 GHz Oscilloscope



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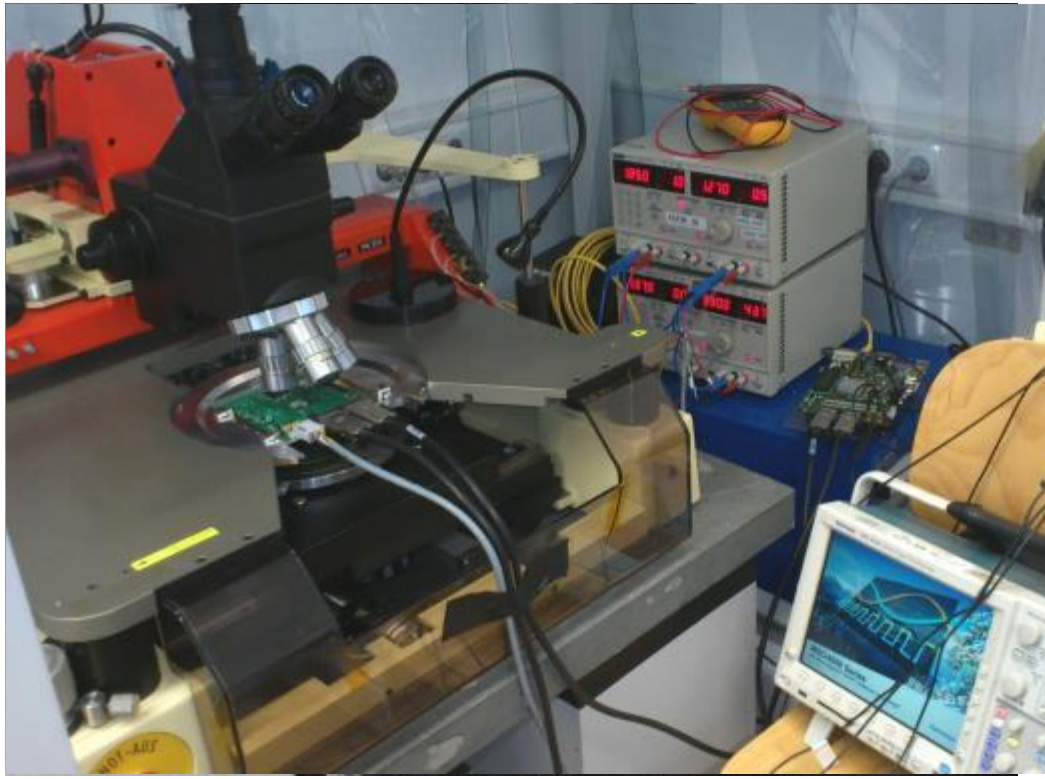
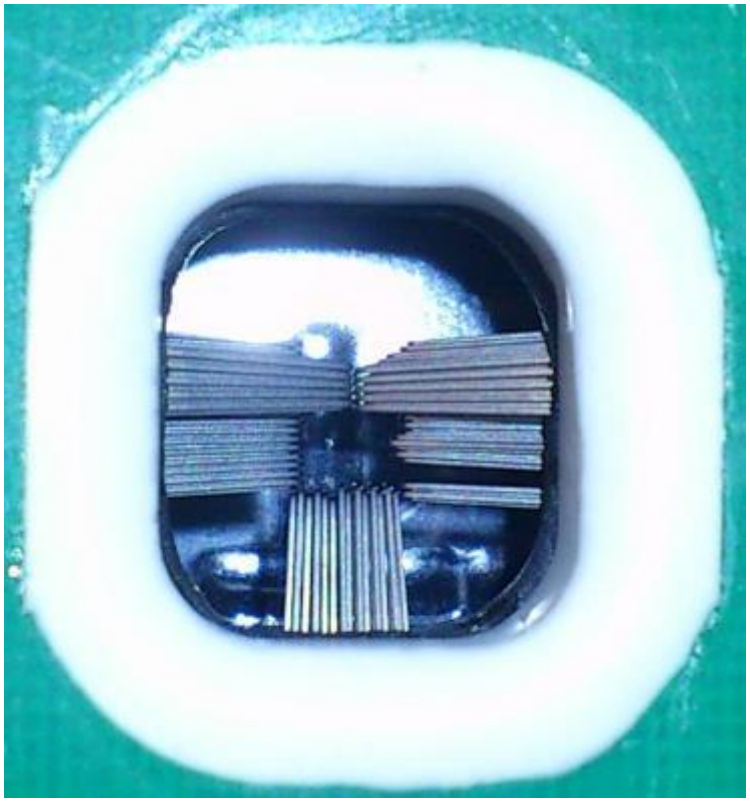
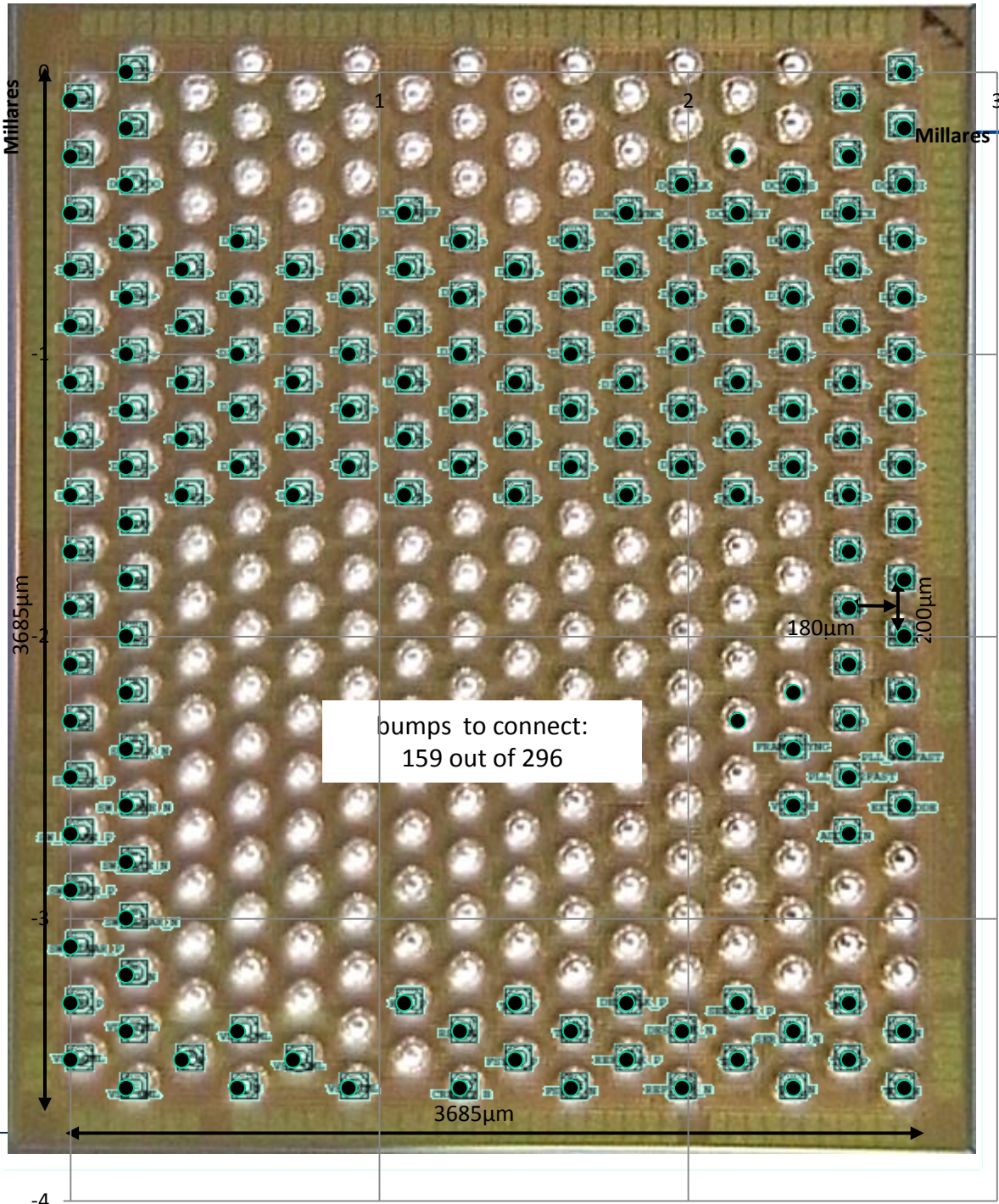


Needle Card

- Xilinx Spartan 6 (DCD emulator)
- Cantilever Needles
- Power Connector
- Infiniband Connector to DHHe (Data, JTAG)





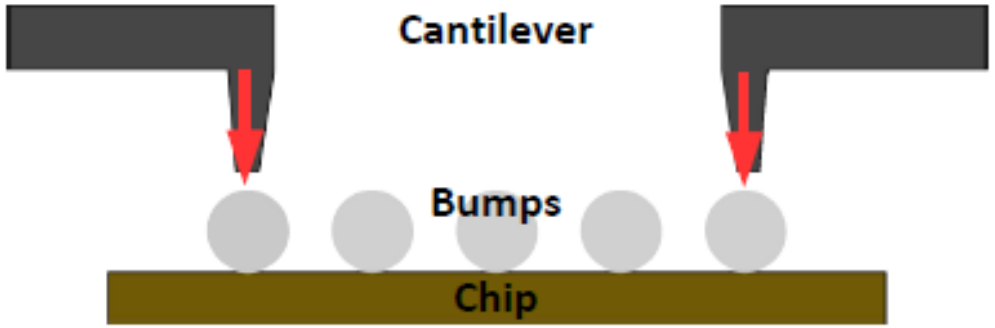
- 159 bumps need to be connected
- Material: SAC
- Pitch: 200 µm (y), 180 µm (x)
- ~110 µm diameter
- Connections:
  - JTAG (4x LVDS)
  - Timing (4x LVDS)
  - Data Link (1x CML)

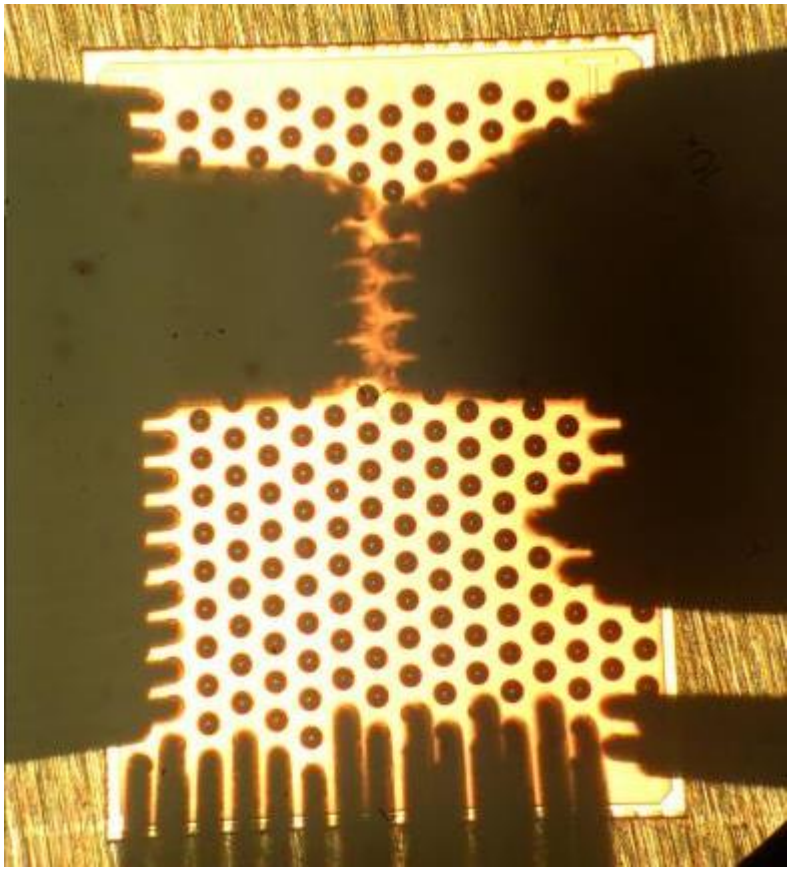
  DHP test system
  - Aux clock (2x LVDS)
  - SWITCHER (4x LVDS)
  - DCD out (8x 8 HSTL)
  - DCD in (8x 2 CMOS)
  - DCD timing (2x CMOS)

  FPGA
  - DCD JTAG
  - DCD_ref (analog)
  - Power (8x VSS, 4x VDD, 2x VDD_CML)
  - PLLxx2Fast
  - FrameSync
  - ResetB (CMOS)
  - Analog IO test signals

Bump Connection

- 159 bumps connected
  Power, JTAG, DCD I/O and SW
- Over travel after last needle contacted ~10 µm
- Manual alignment and touchdown
- If card not used for days, needles pre-cleaned





Bump Connection

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- 159 bumps connected
  Power, JTAG, DCD I/O and SW
- Over travel after last needle contacted ~10 µm
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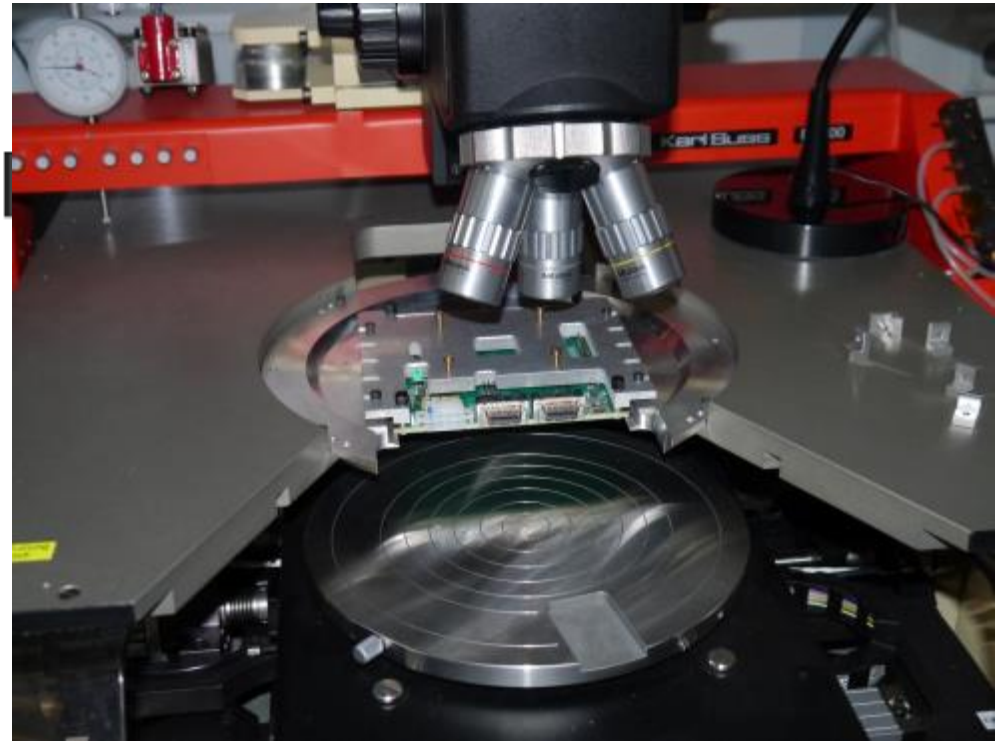
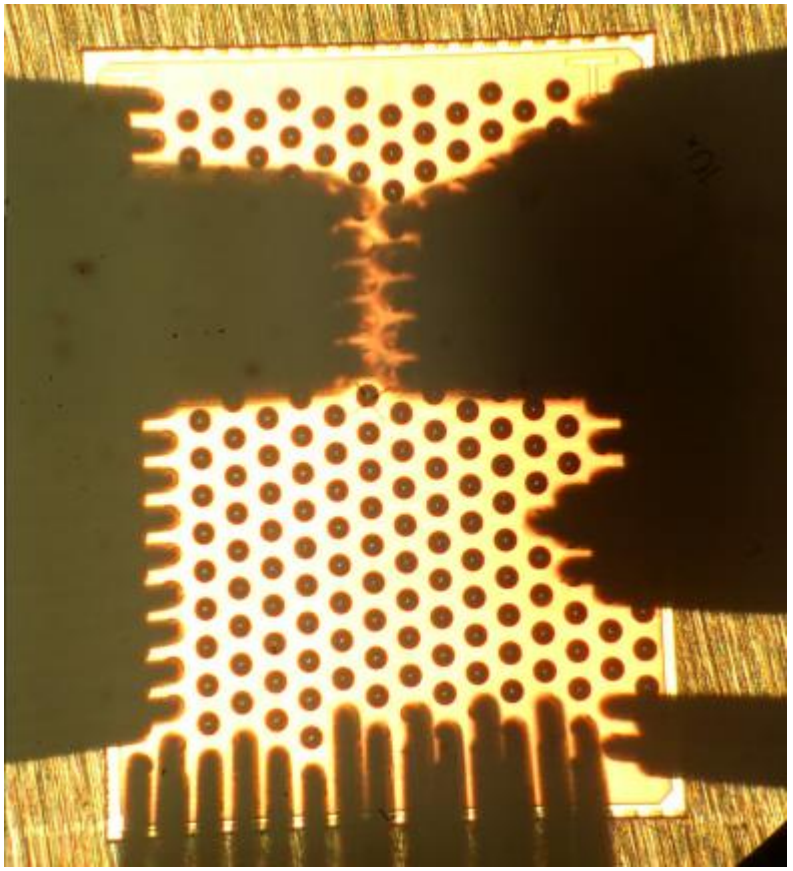
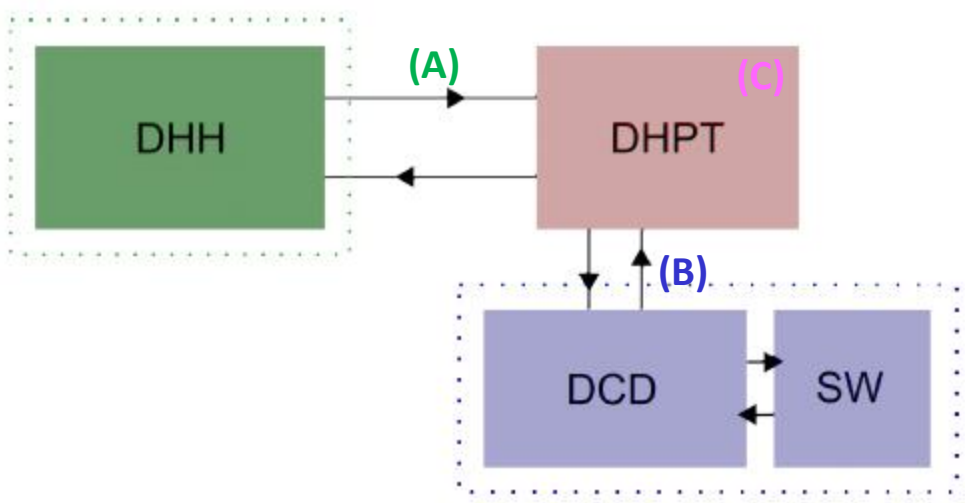
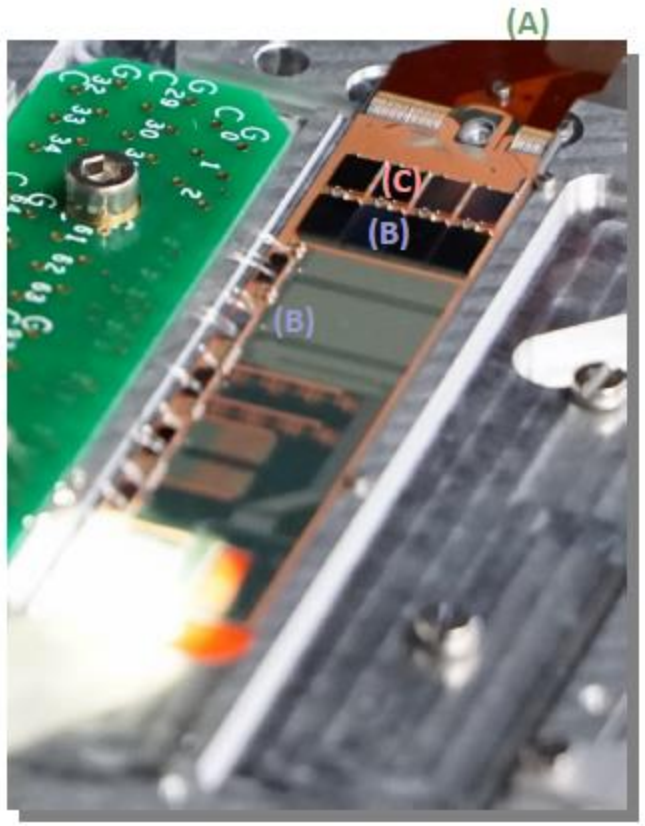




Test System

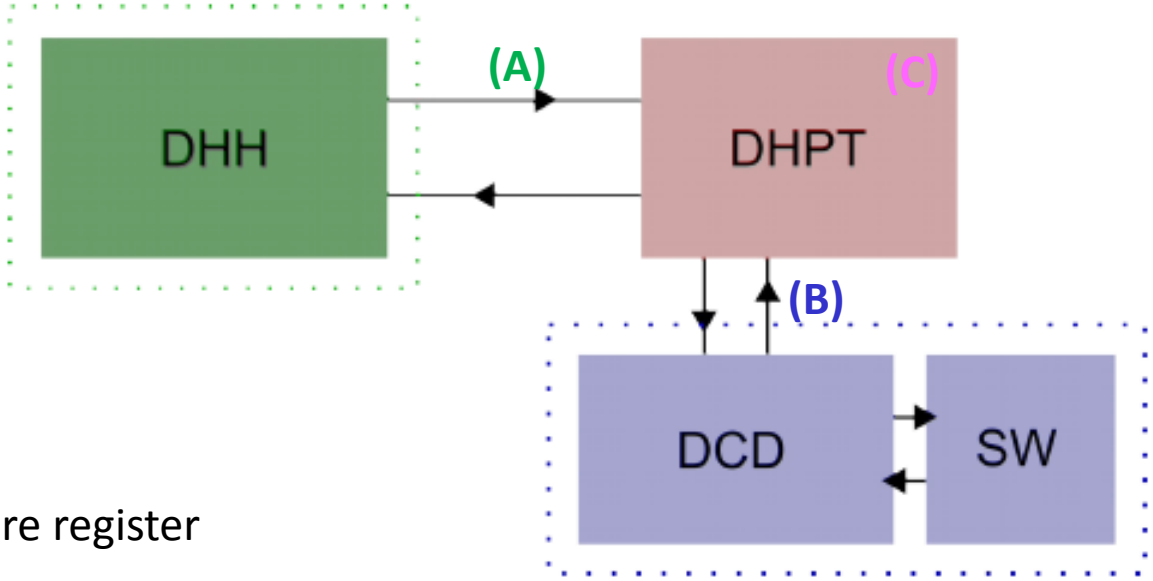




The tests must include 3 blocks:

- JTAG/Link (A)
- I/O (B)
- Logic (C)

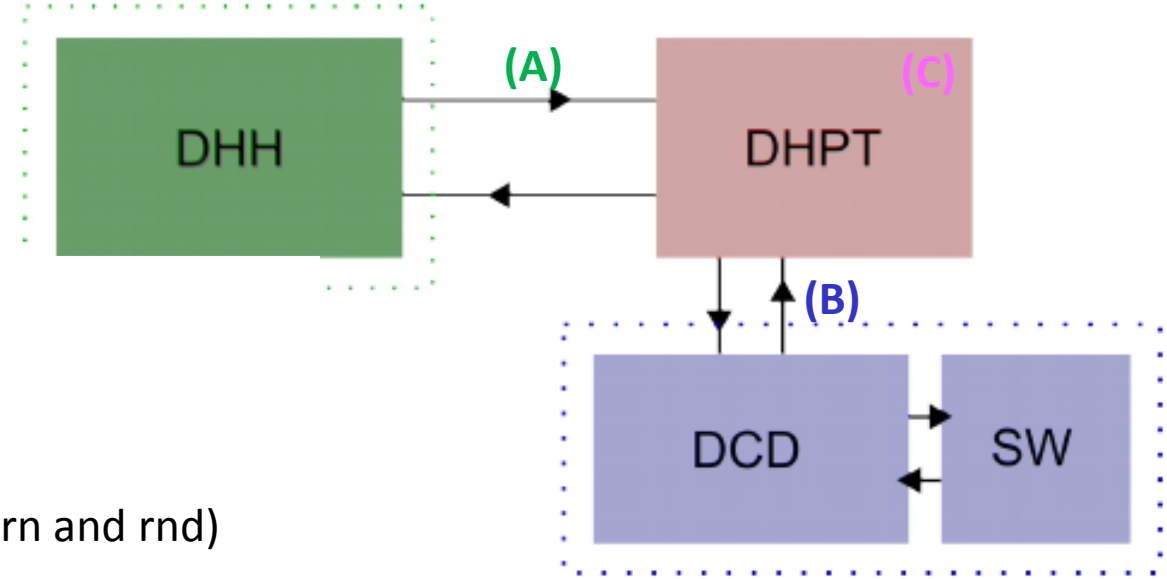
Test System



JTAG/Link (A)

- Configuration of Global & Core register
- JTAG chain to DCD
- Temperature DACs
- Check CML driver DACs (Gbit Serial Link) via current consumption

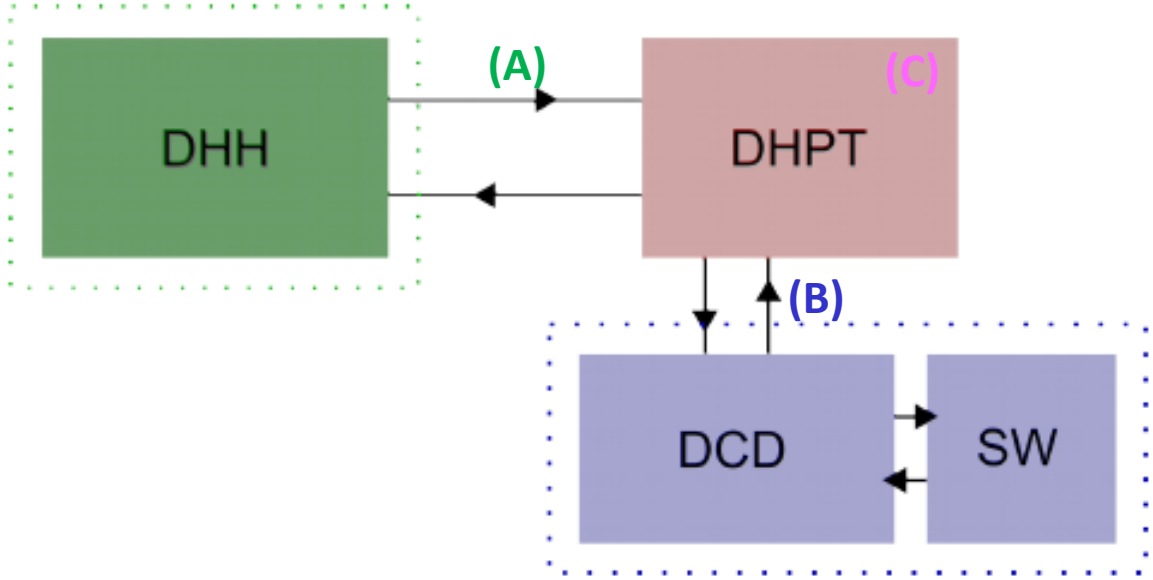
Test System



I/O (B)

- DCD data (DCDpp test pattern and rnd)
- Switcher sequence generator
- DCD offset bits

Test System



Logic (C)

- Zero-suppression
- Occupancy tests
- Threshold/hit finder
- SRAM tests
  - Standardized pattern (0xaa)
  - Bit error counter (single bit flip compensation)

Status of the Funcional Verification

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	IP Block / Task	Status	Comment
Custom IP	Gbit Link Driver	✓	
	PLL / Serializer	(✓)	Works with adjusted VCC / CLK freq.
	Temperature Sensor	✓	
	LVDS IO	✓	
	Interface DHP-DCD	TBD	Need new WB adapter (LVDS DCDCLK)
	Interface DHP-Switcher	(✓)	Gated mode operation not verified yet
	Bias DAC, Current reference	✓	
Data Processing	Command Interface (Manchester encoded)	✓	
	Memory Access (via JTAG)	✓	
	Data Processing: Channel Masking	TBD	
	Double Precision Common Mode Processing	✓	
	Overflow Handling	TBD	

DHPT 1.0 Status

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- Functional verification
  - Analog blocks ✓
  - Digital signal processing → ✓, ongoing (high occupancy test)
  - Interface DCD, Switcher → (✓) **gated mode operation, tbd.**
  - Serializer too slow → needs non standard operation conditions (higher VDD supply)
- Probe station test to deliver KGD for prototype module assemblies ongoing
- Continue with in-system verification using E-MCM and PXD9 pilot modules
  - Switching of operation modes
  - Signal integrity (high speed link)
  - TID sensitivity
- Planned re-design DHPT 1.1
  - Serializer bug fix
  - Anything else that eventually shows up (Data processing, E-MCM operation …)

Testing Plans

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- Hybrid 5.0:
  - Tests communication DCD ↔ DHP
    Irradiation, temperature, 2b DAC, timing and phase alignment
  - Planned within the next 4 weeks

- EMCM:
  - System related aspects
    Link stability and parameter optimization
  - After B2GM

- Pilot Run PXD9
  - Gated mode and timing
  - April 2015

→ Final submission after positive feedback from these tests

Yield

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- 33 DHPT1.0 tested

4 non operational (1 broken, 3 with bump issues)

#Chip ID	Power			JTAG			DCD	Serial Link		Issues
	GCK	VDD+VDD_CML	DVDD	DHH	DCD	sw sequence	Data	PLL	CML dirver	
1	x	<10mA	<30mA	x	n/A	n/A	n/A	n/A	n/A	no response
2	ok	~90mA	~37mA	ok	ok*	ok**	n/A	ok	ok**	
3	ok	~82mA	~42mA	ok	ok*	ok**	n/A	ok	ok**	
4	ok	~104mA	~31mA	ok	ok*	ok**	n/A	ok	ok**	
5	ok	~105mA	~39mA	ok	ok*	ok**	n/A	ok	ok**	
6	ok	~102mA	~38mA	ok	ok*	ok**	n/A	ok	ok**	
7	ok	~103mA	~38mA	ok	ok*	ok**	n/A	ok	ok**	
8	ok	~90mA	~32mA	ok	ok*	ok**	n/A	ok	ok**	

ok* loop back: DHH emulator → TDI → DCD emulator → TDO → DHH emulator
ok Oscilloscope inspection (incl. Gated mode via veto (trigger) and LFSR output)**

Quality Control

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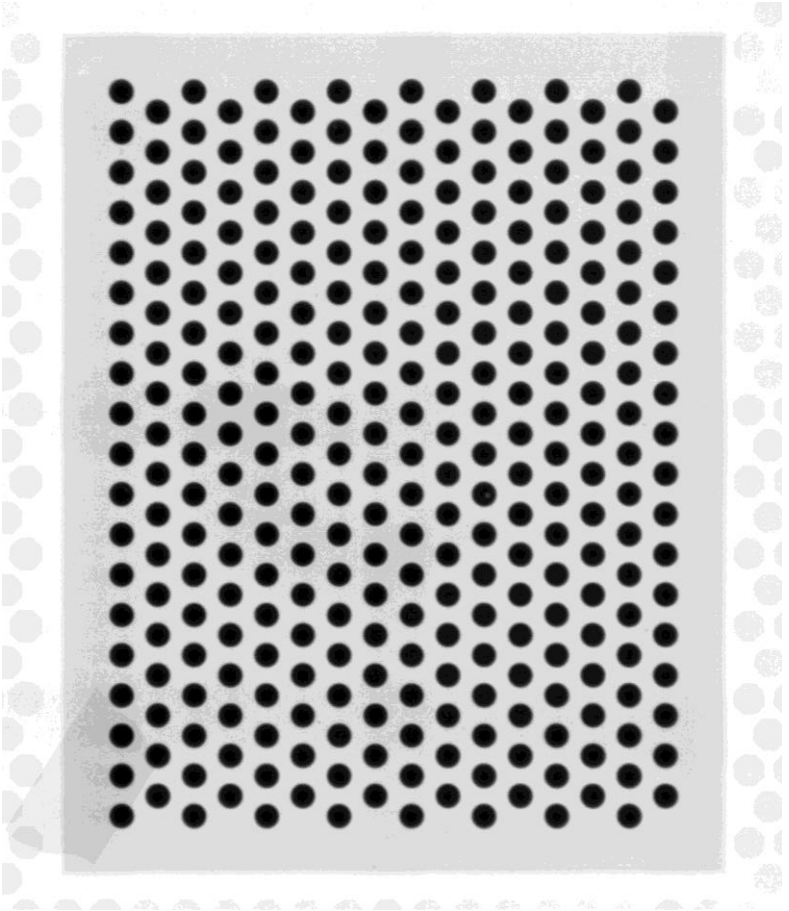
- Optical inspection: Missing balls, scratches on the passivation
- Tests with needle card (grounding, handling, reinforcing plate)
- Metrology after needle card testing (flattened balls ~3-5 µm)
- No issues found after several flip chip assemblies at IZM



DHPT Production Details

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- MPW submission
  - Two MPW runs per month, turn-around ~12 weeks
- PXD production
  - Can be done with MPW production + extra wafers, no engineering run needed
  - 30 wafers on PXD9, 6 modules per wafer, 4 DHPT1.1 per module = **720 DHPT1.1** units
  - We assume so far a yield of 65 % (extrelemy pessimistic) → 1100 DHPT1.1
- Full scale testing
  - 'Chess board' fixture with 10x10 array of cavities for production testing
  - Backup needle card
  - Realistic scenario: 85 % yield, 5 chips/day, 5 days/week → 8 months to deliver fully tested DHPs enough to populate the 180 modules from PXD9

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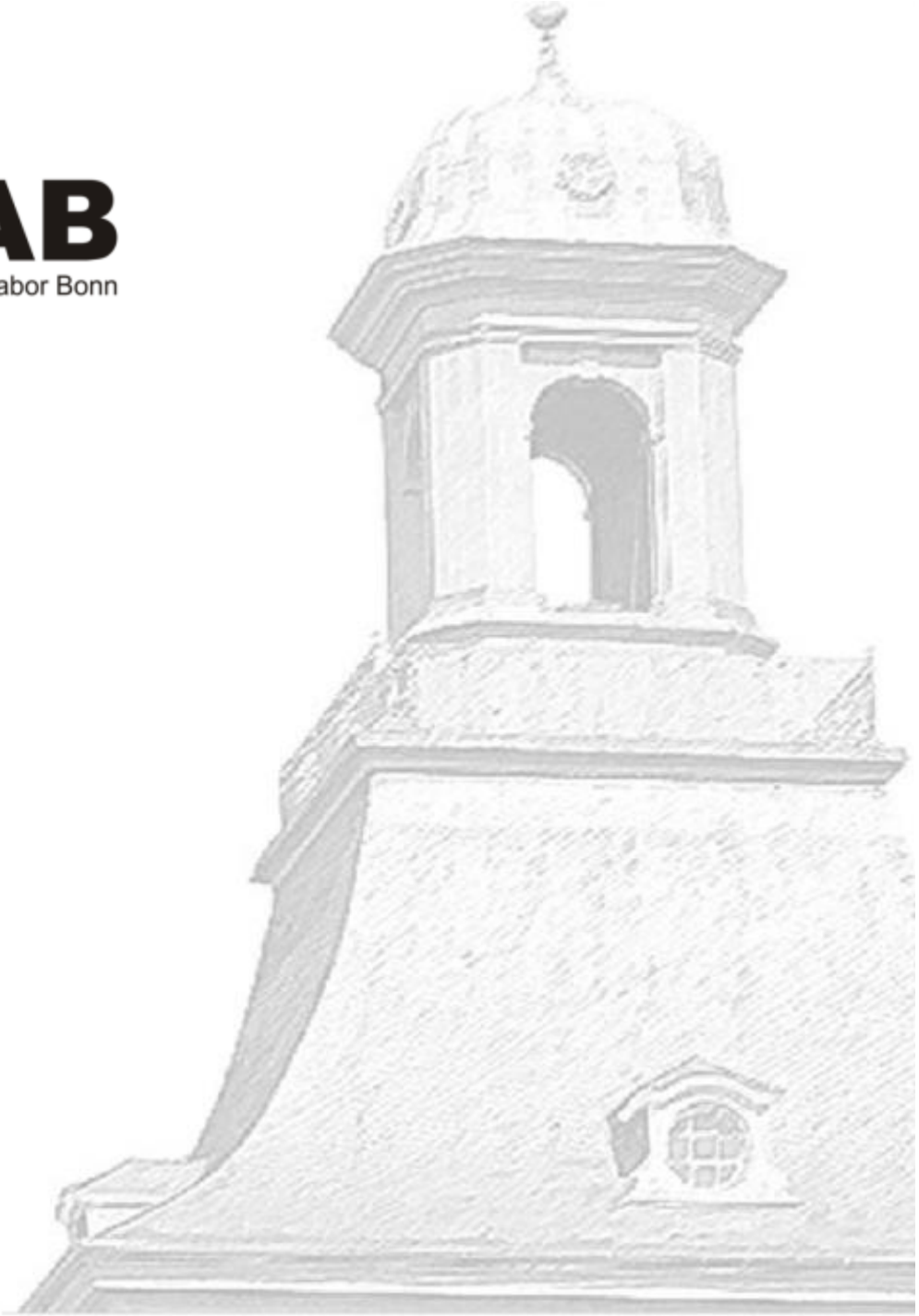

Thank you

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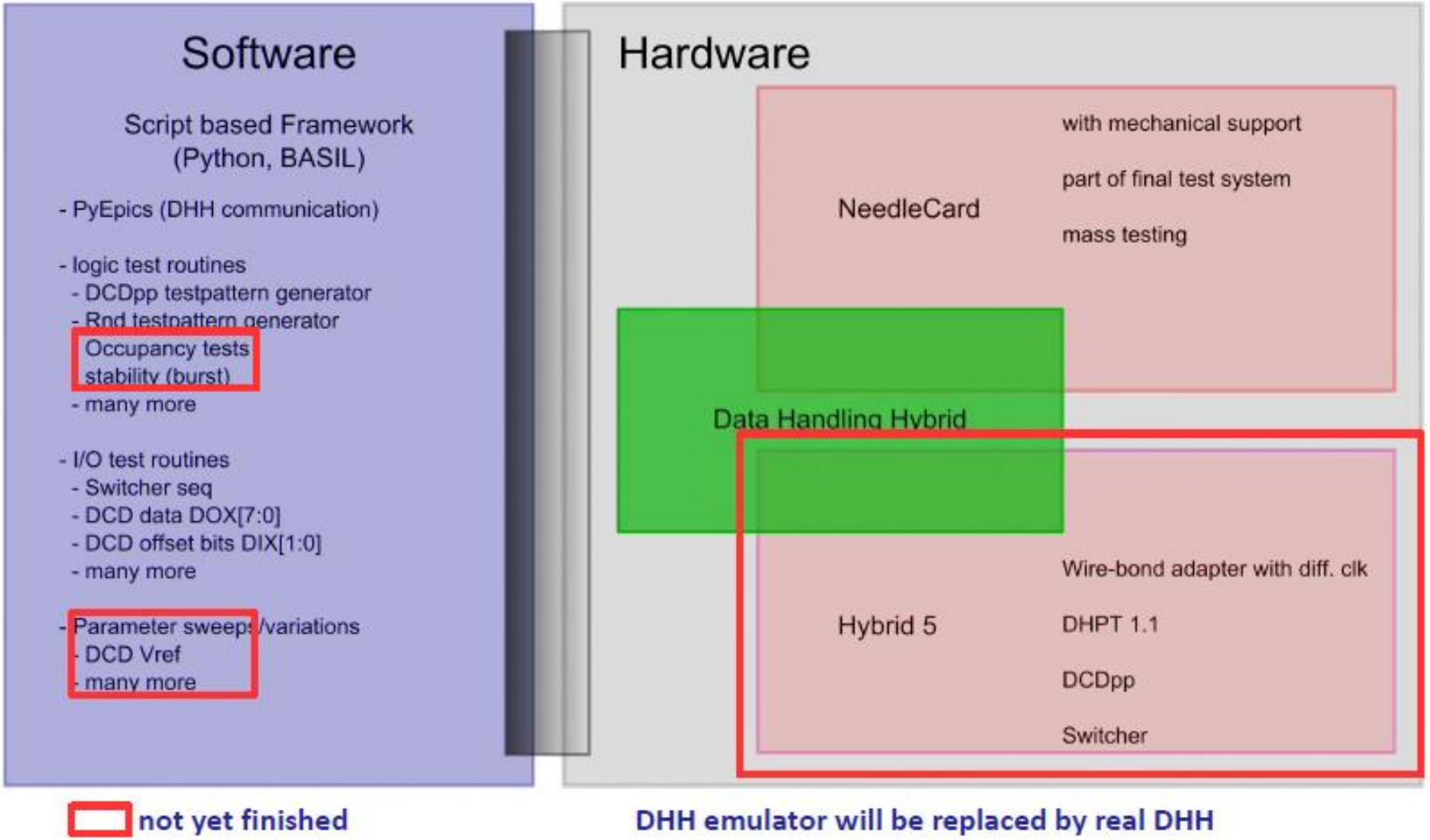
Status of the Test System



DHPT1.0 Testing

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Automatic test system

1) Current and Voltage check (so far manually)
2) Configuration of JTAG registers
3) I/O testing
    - 3a) DCD emulator memory filled with random data (random bit gen.) and read by DHPT
        → Comparison (5 cycles)
    - 3b) DHPT switcher sequence is filled with random data
        → Switcher sequence is read and switcher mem blocks are swapped back and forth (5 cycles)
    - 3c) DHPT offset bits are generated and read by the DCD emulator
        → Comparison (5 cycles)