




# PXD Gated Mode

**ASIC Review Meeting**

**October, 27 2014, Munich**

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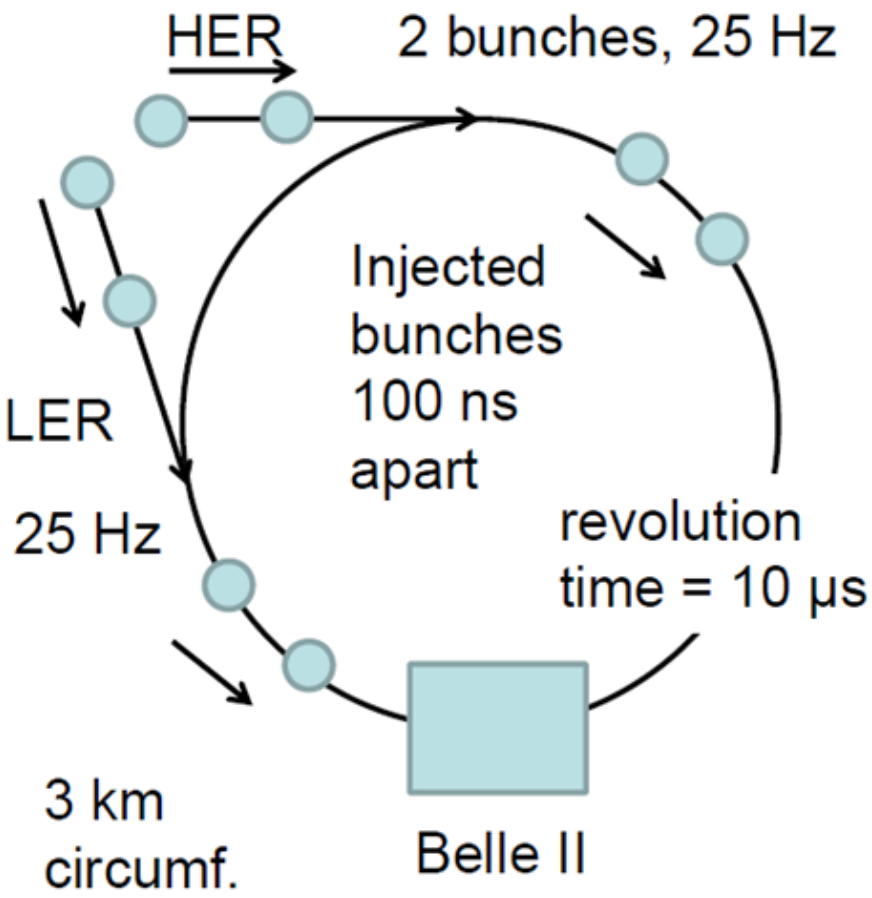
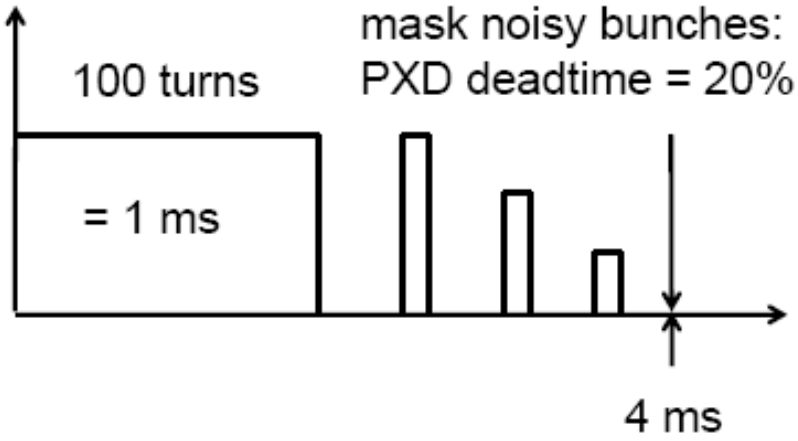
On behalf of the DEPFET collaboration

# Injection Scheme of SuperKEKB



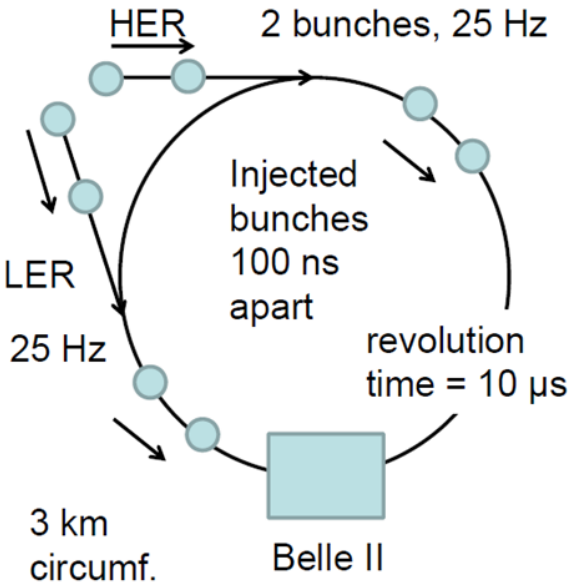



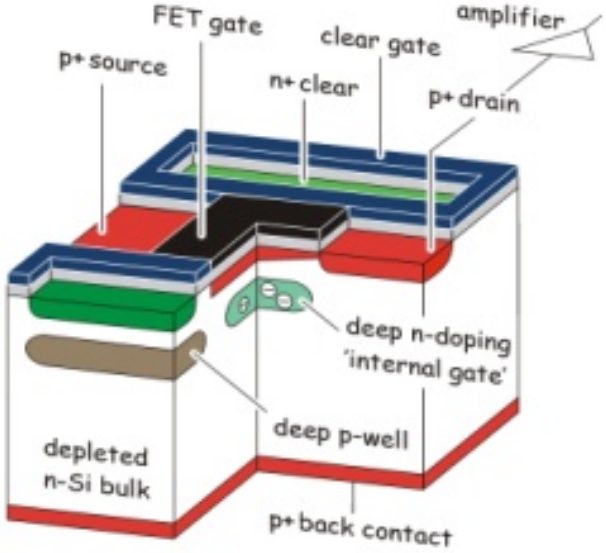

4ms for cooling mechanism

=> Loss of particles (‚noisy' bunches)

**→ How to gate DEPFET pixels during bunch injection?**

# Principle of the DEPFET gated-mode

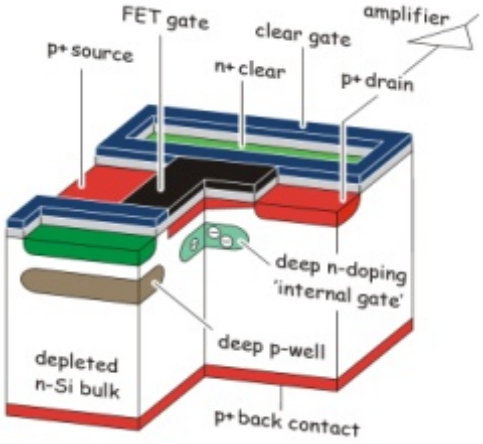



- "Noisy bunches" create (junk) electrons within the PXD detector
- These junk electrons have to be removed while the number of stored electrons in the internal Gate should **not** be changed!

# Principle of the DEPFET gated-mode

- Applying appropriate voltages to **Clear** and **Gate** one can apply an electronic shutter:
  - Clear pulse to all pixels during the noisy bunch injection (every 10µs, ΔU = 15V)
  - Keep the Gate in the off state (+5V)




Two questions (sensor related):

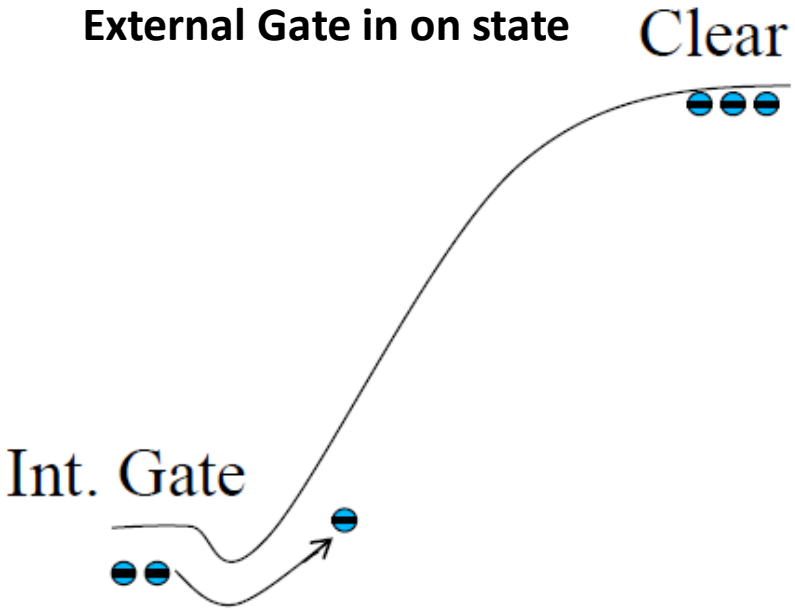
1) Can we protect charge in the internal Gate from being cleared?

2) How much of the junk charge will arrive in the internal Gate?

# Selectivity of the Clear Process

## Real Clear

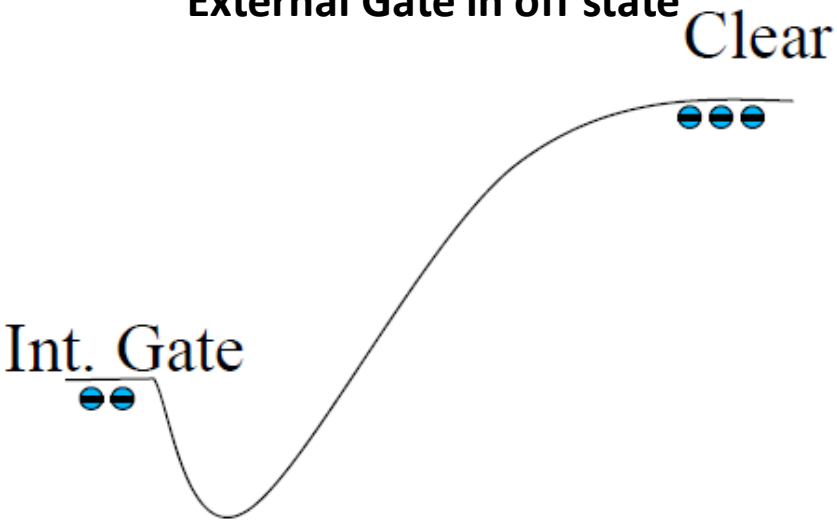
**External Gate in on state**




Electrons can overcome the small potential barrier by thermionic emission.

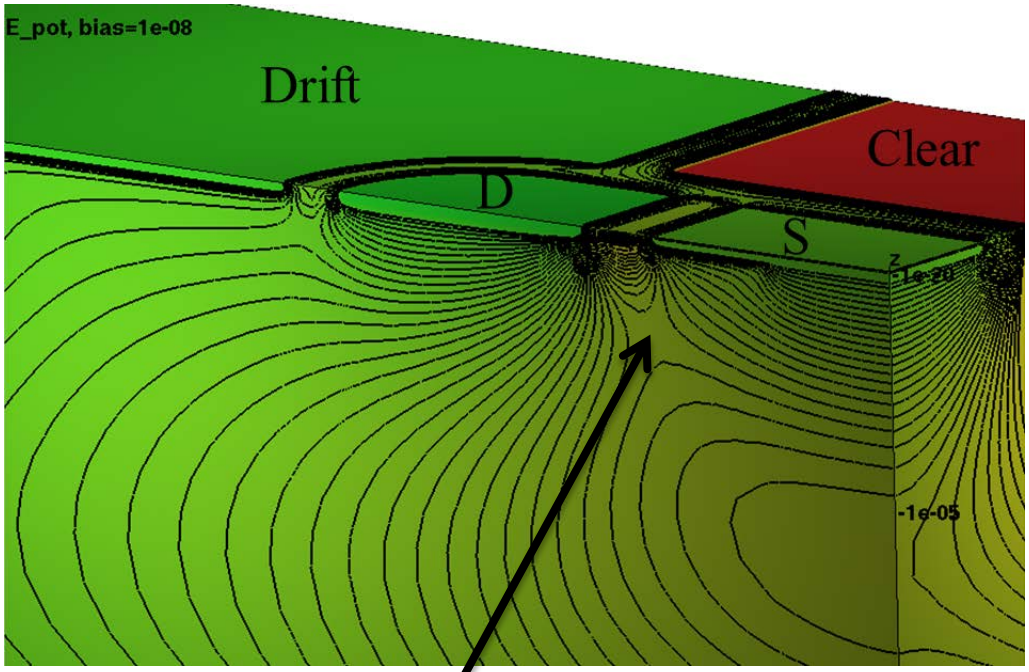
## Suppressed Clear

**External Gate in off state**




→ The difference is due to the applied voltage at the external Gate.

# Shielding of the Internal Gate

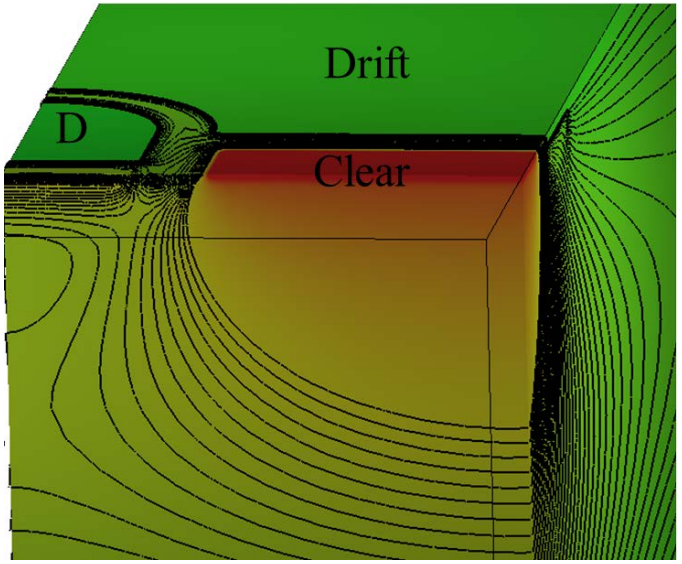



Clear region is much larger than internal gate

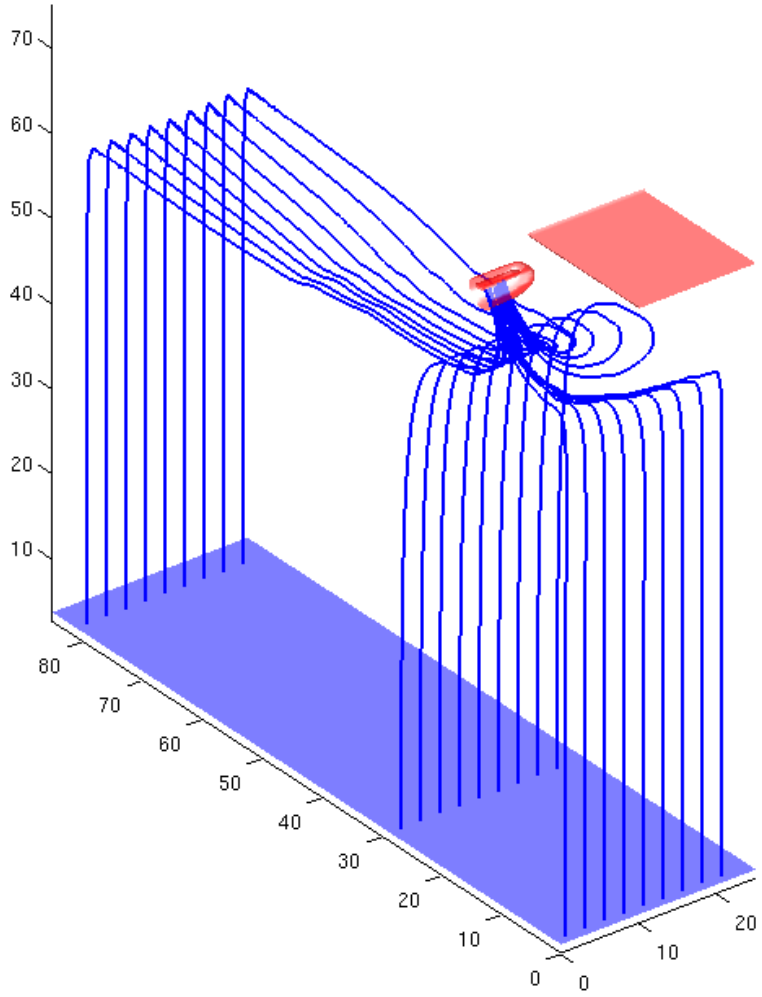
→ Good for dumping electrons into the clear

Potential barrier
→ Caused by the reach through of the drain to the source

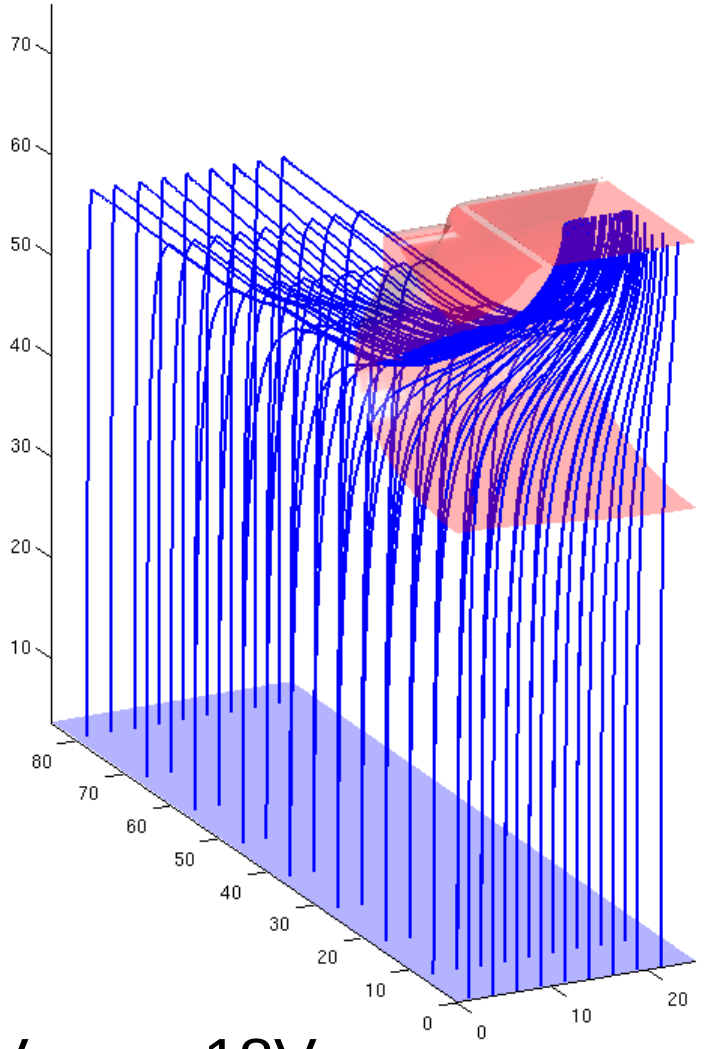
First results: No additional electrons in the Int. Gate @Vclear=18V



# Shielding of the Internal Gate




$V_{Clear}$ = 3V



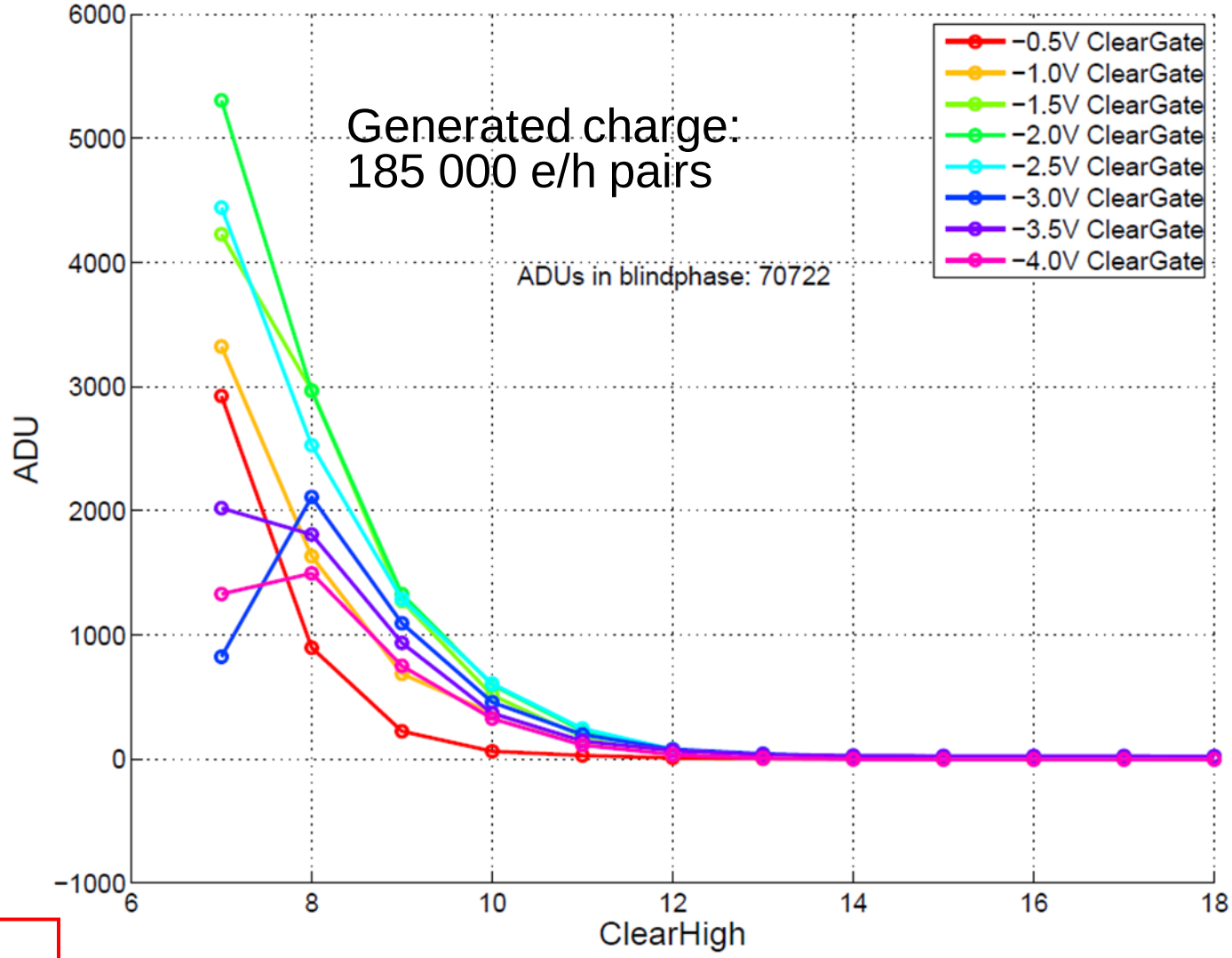

$V_{Clear}$ = 18V

# Gated-Mode - DEPFET Sensor

- MiniMatrix setup used to investigate the gate-mode operation with PXD6 DEPFET prototype

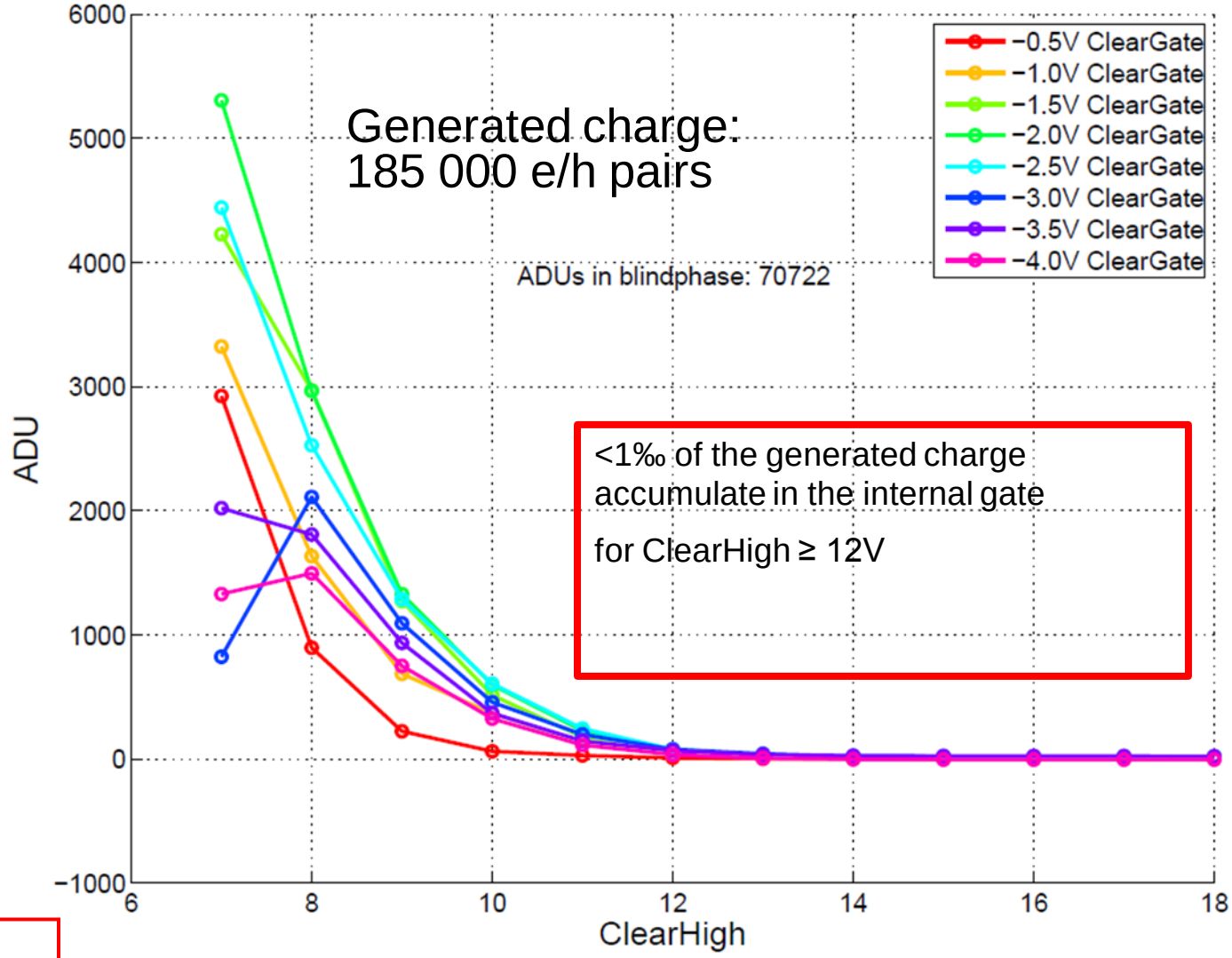
- DEPFET sensor shows the gated-mode characteristic
  → Measurements by Jan Scheirich and Felix Müller

# Gated-Mode - DEPFET Sensor



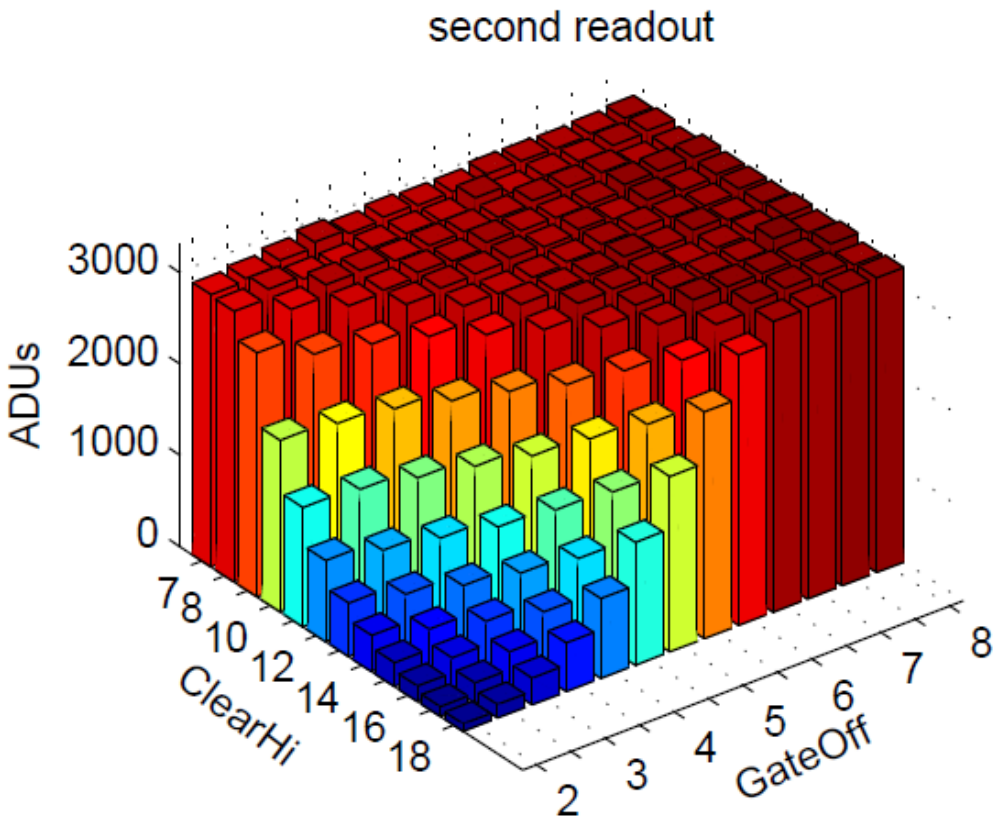

**1ADU = 2.61 electrons**

# Gated-Mode - DEPFET Sensor




**1ADU = 2.61 electrons**

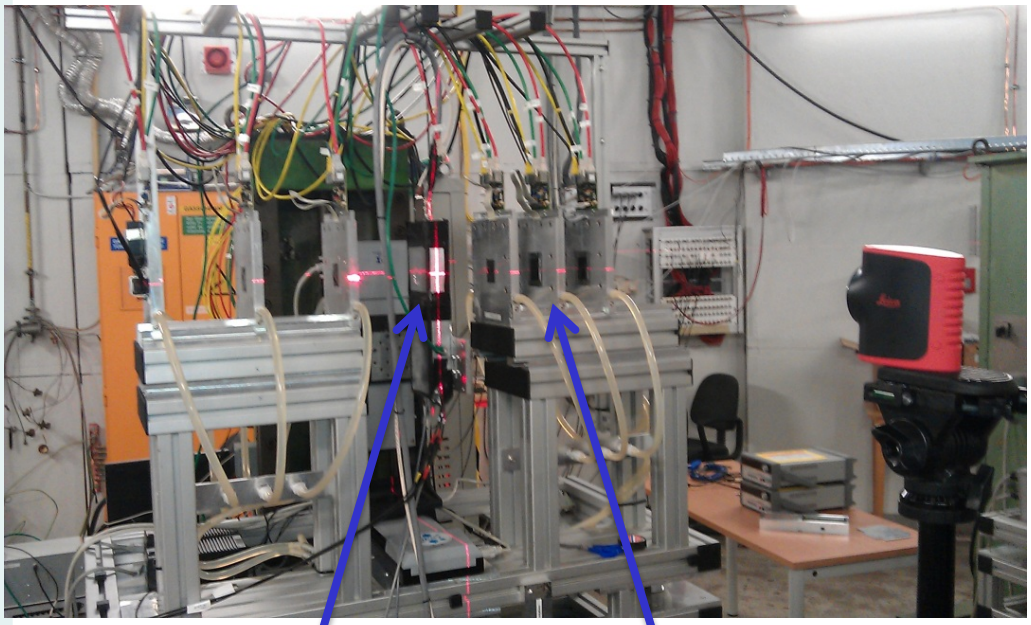
# Signal Loss during Gated-Mode




- Charge loss depends on the Clear On and Gate Off voltag
- For Gate Off > 5V there is no charge loss

# Test Beam 2012 - Setup at DESY

Program dedicated to gated-mode with Hybrid H4.1.11



PXD6 Hybrid

EUDET telescope with 6x M26 sensors

Hybrid H4.1.11

→ thin standard Belle II design

→ 5 micron gate length

→ SWB and DCDBv2 @ 100MHz

→ 4 GeV electron track

→ track extrapolation error ~6µm

# Beam Test Program

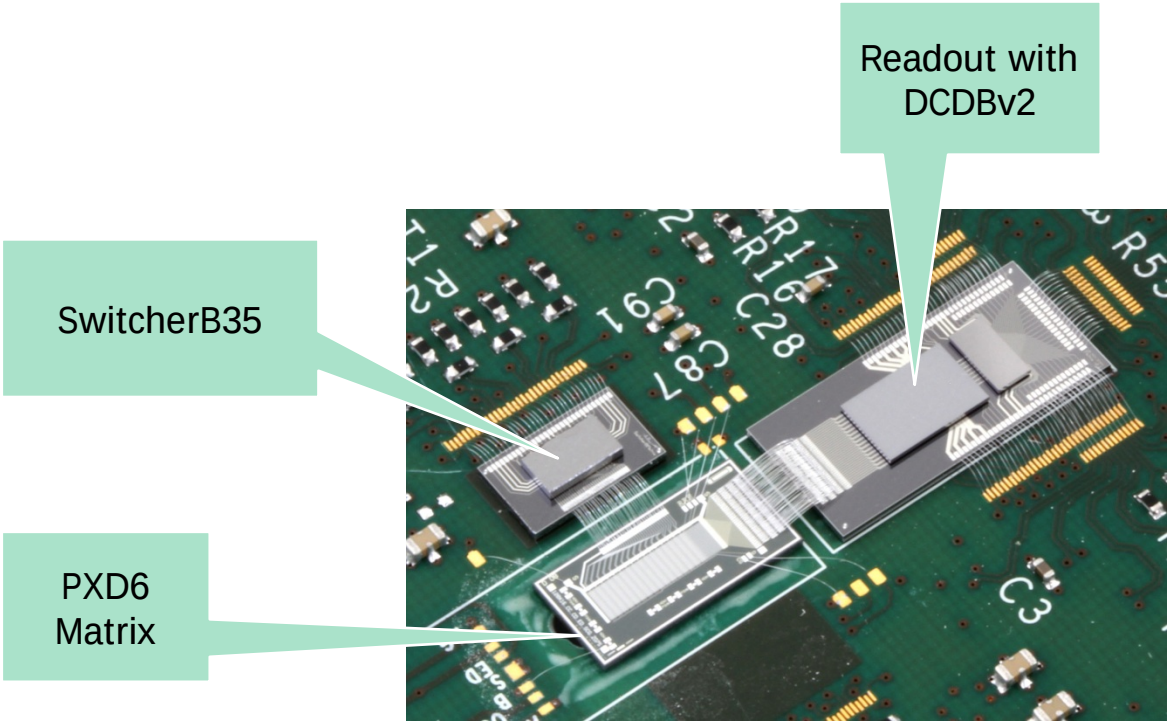
➢ To evaluate if the gated-mode works, readout of 8 consecutive DEPFET frames for each trigger.

- Exp. A: 'Standard Operation'
  - ▷ Normal readout of DEPFET with nominal voltages
  - ▷ Check everything works as expected before gated mode sequence
- Exp. B: 'Junk Charge Generation'
  - ↳ • Track crosses DEPFET in blind mode → internal Gate is shielded
  - ↳ • Exit blind mode in consecutive frames

  → Goal: Check hit pixel collects **no** charge from track
- Exp. C: 'Signal Charge Restore'
  - ↳ • Track crosses DEPFET in sensitive mode → hit pixel collects charge
  - ↳ • Enter and exit blind mode in intermediate frames

  → Goal: Check no signal loss from IG to clear

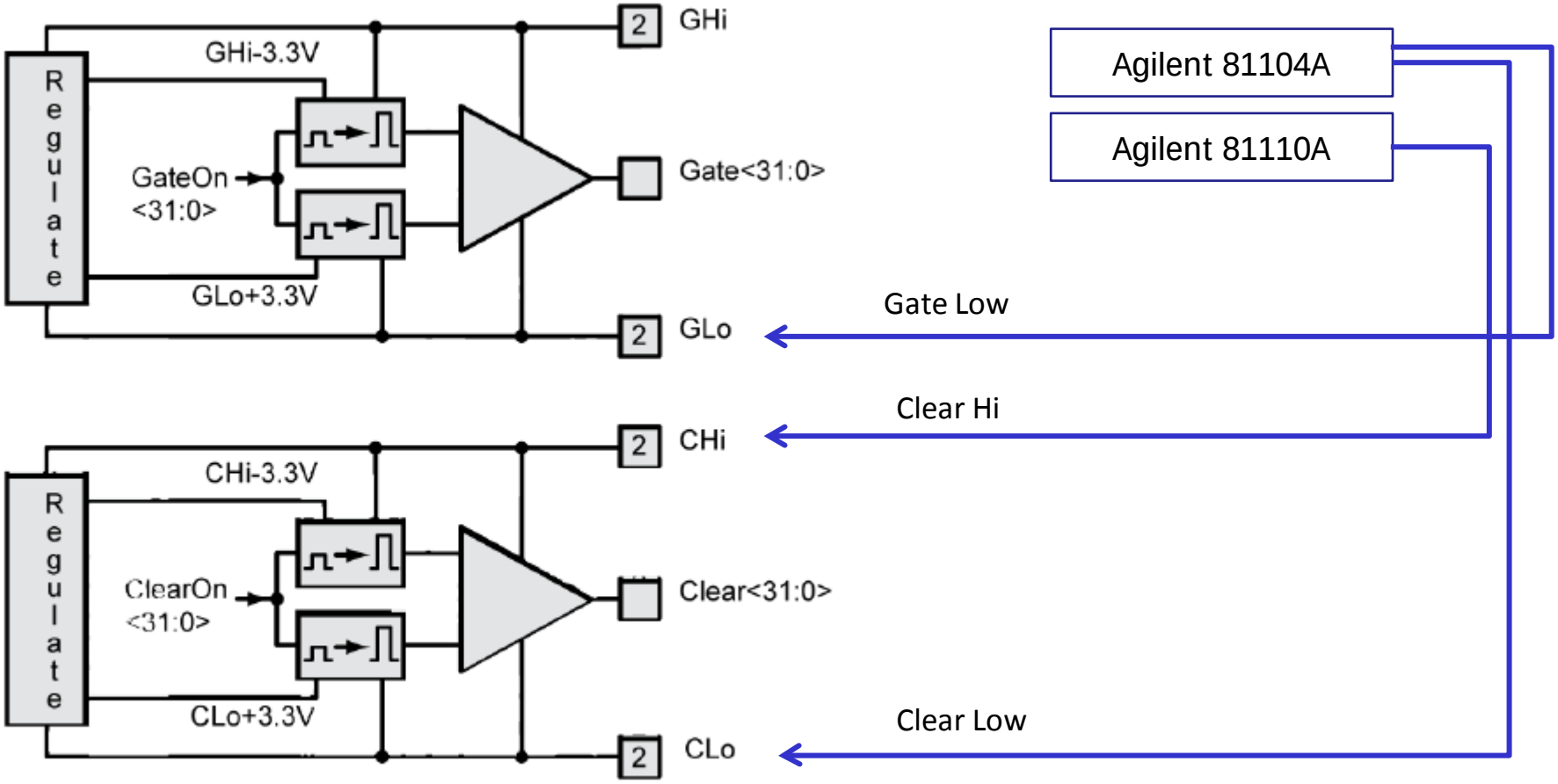
# Hybrid Board H4.1.11




Switch the DEPFET into blind mode by changing

1) the GateOn, ClearLow and ClearHigh voltages which are supplied to the Switcher
2) the operation mode is controlled by a Trigger (TLU or Pulse Generator)

# Gated-Mode Operation Setup w/ SwitcherB




Not the recommended operation for the SwitcherB.

# Experiment **A** – Normal Operation

Operating voltages (wrt. Source)

ClearHigh: +20V

ClearLow: +3V

GateHigh: +3V

GateLow: -3.4V

CCG: -1.7

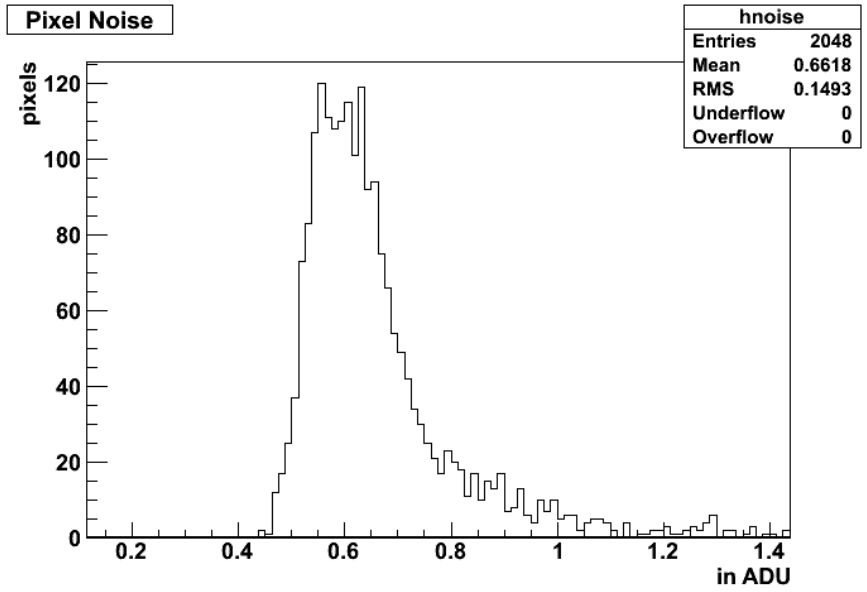
Back: -19V

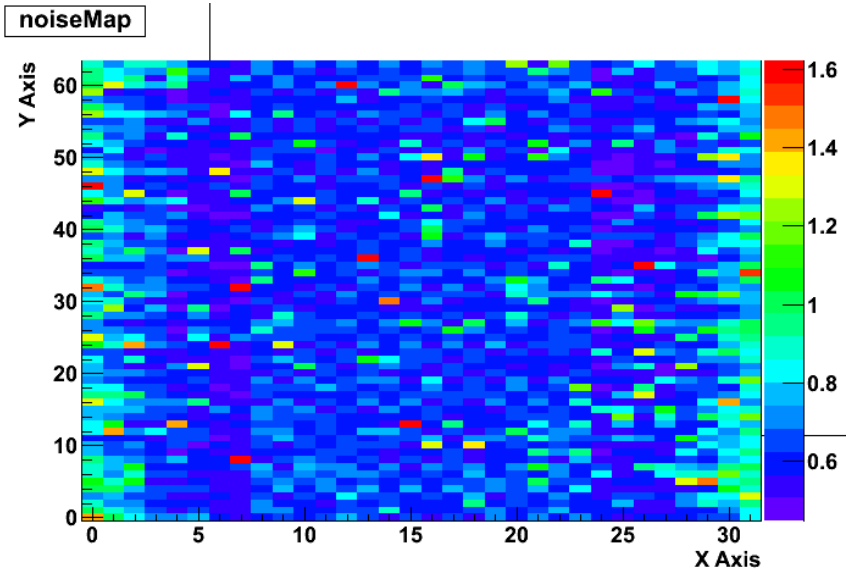
Drift: -2V

Calibration constants

- DCD at 100MHz → 5us per frame
- LSB is ~82nA
- Gq is ~500pA/e

Noise peaks ~0.66ADU; Pedestals, CM and firing frequency ok.

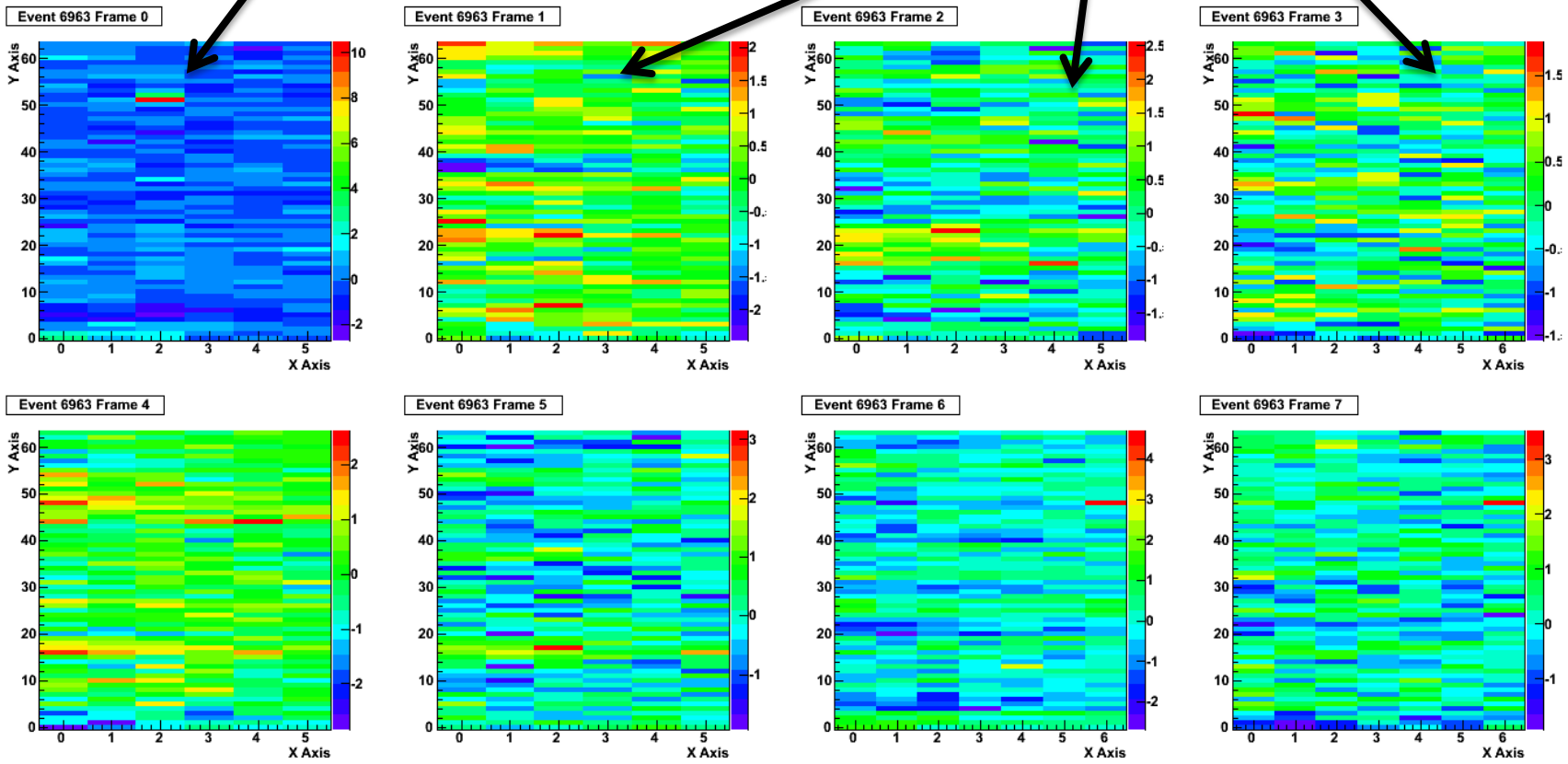


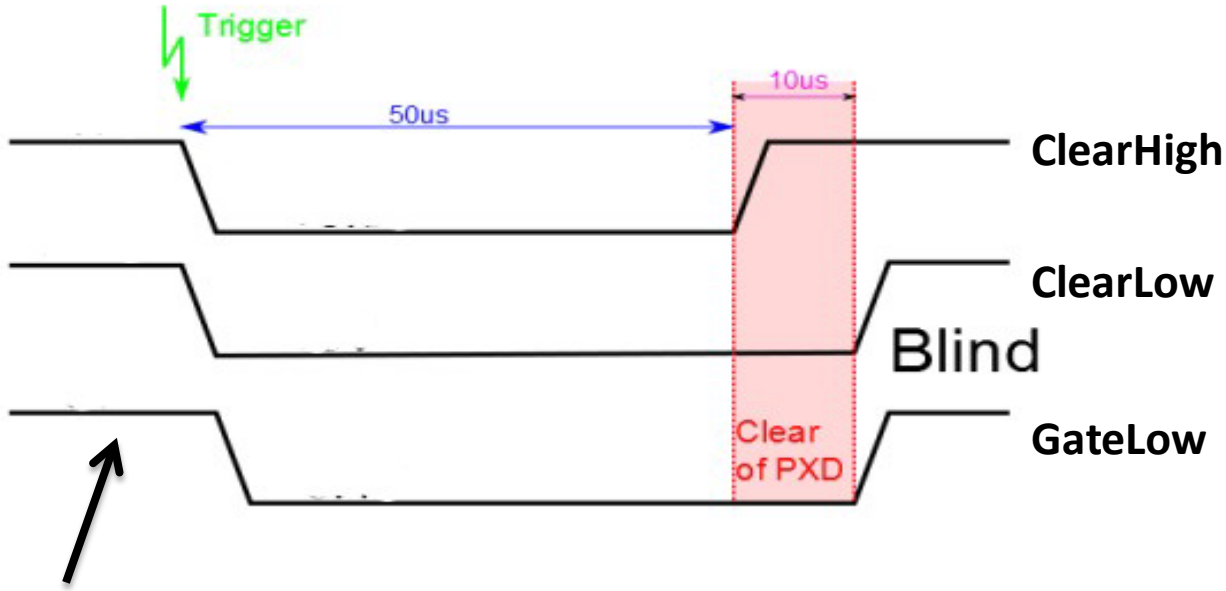
# Event data after pedestal and cm correction

**MIP in triggered frame**

**Only noise in other frames → good clear**



# Experiment B: 'Junk Charge Generation'

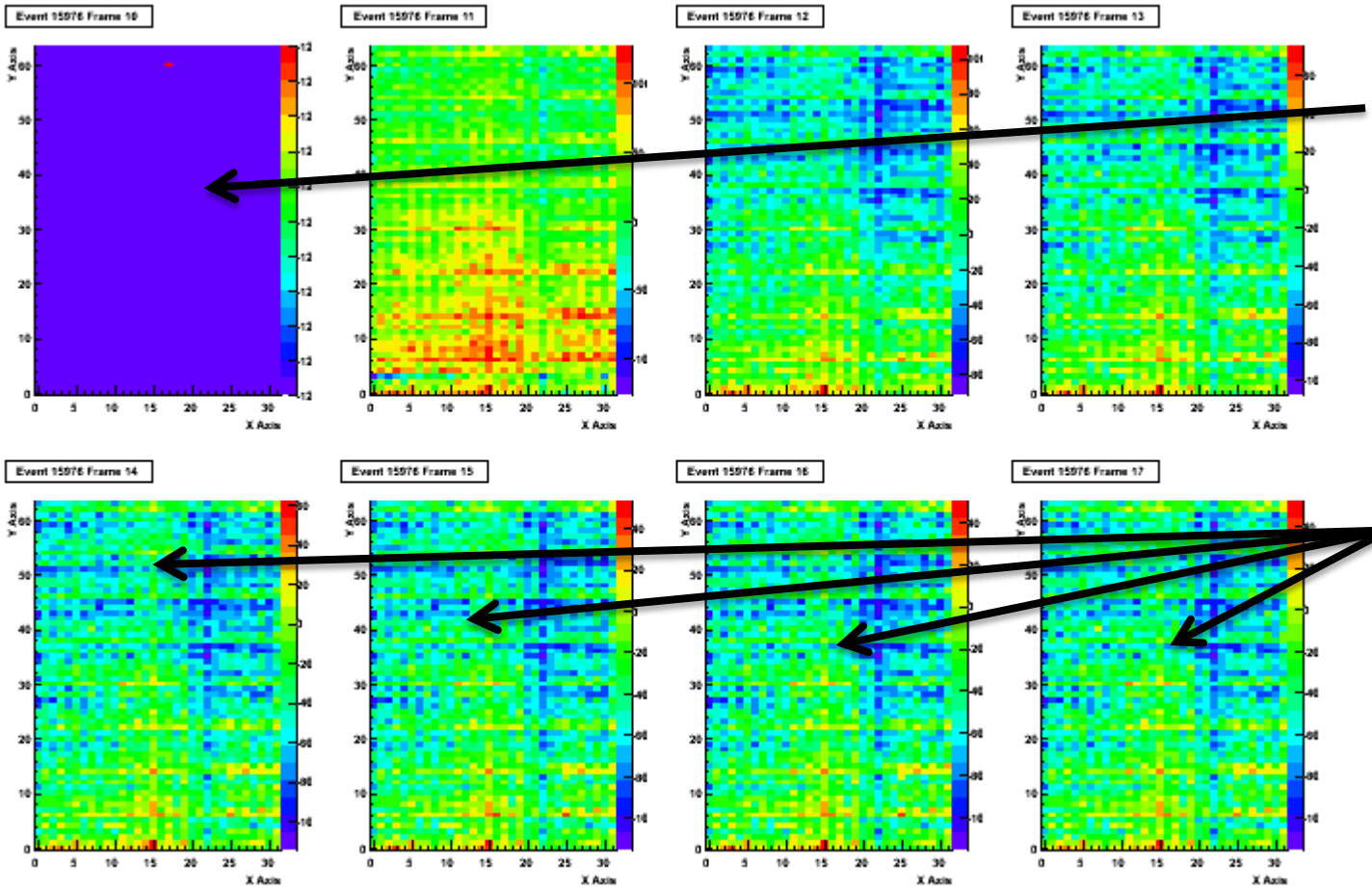



Matrix in blind mode
when track crosses.
Readout is stopped.

Exit blind and readout
8 frames

Scanned ClearLow 'HiLevel': +20V (nominal), +16V, +10V

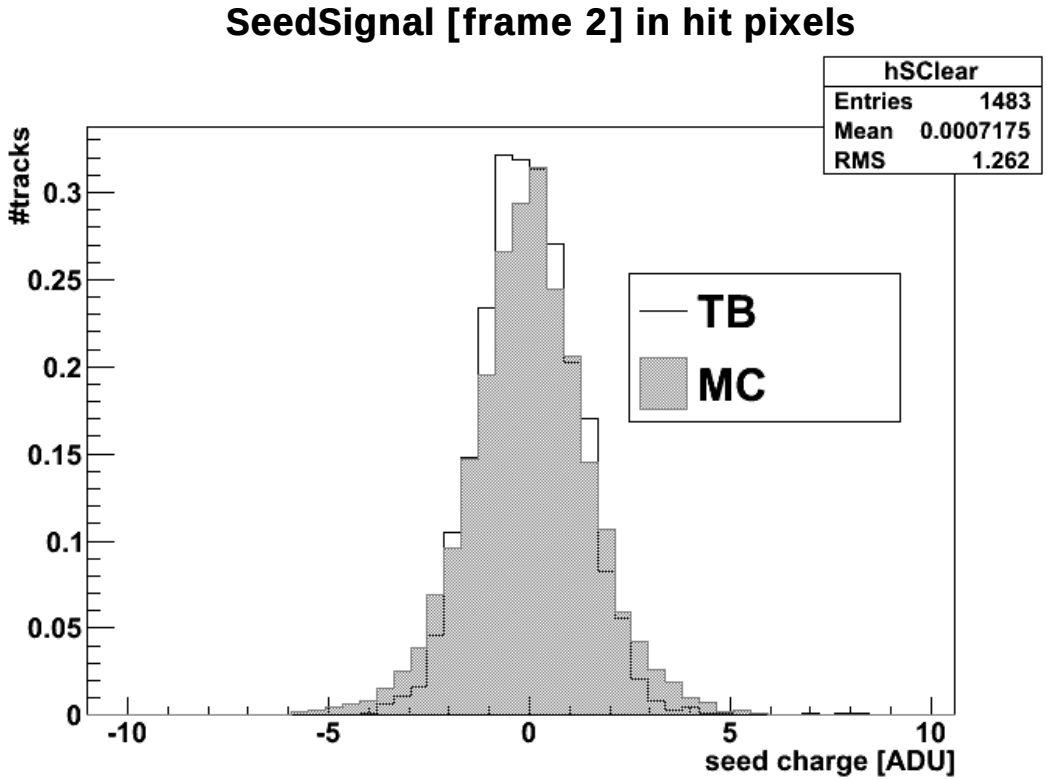
# Typical 'RawData' Event Run4108




Most pixels at -127ADU
→ I_drain out of ADC range

Stable signals

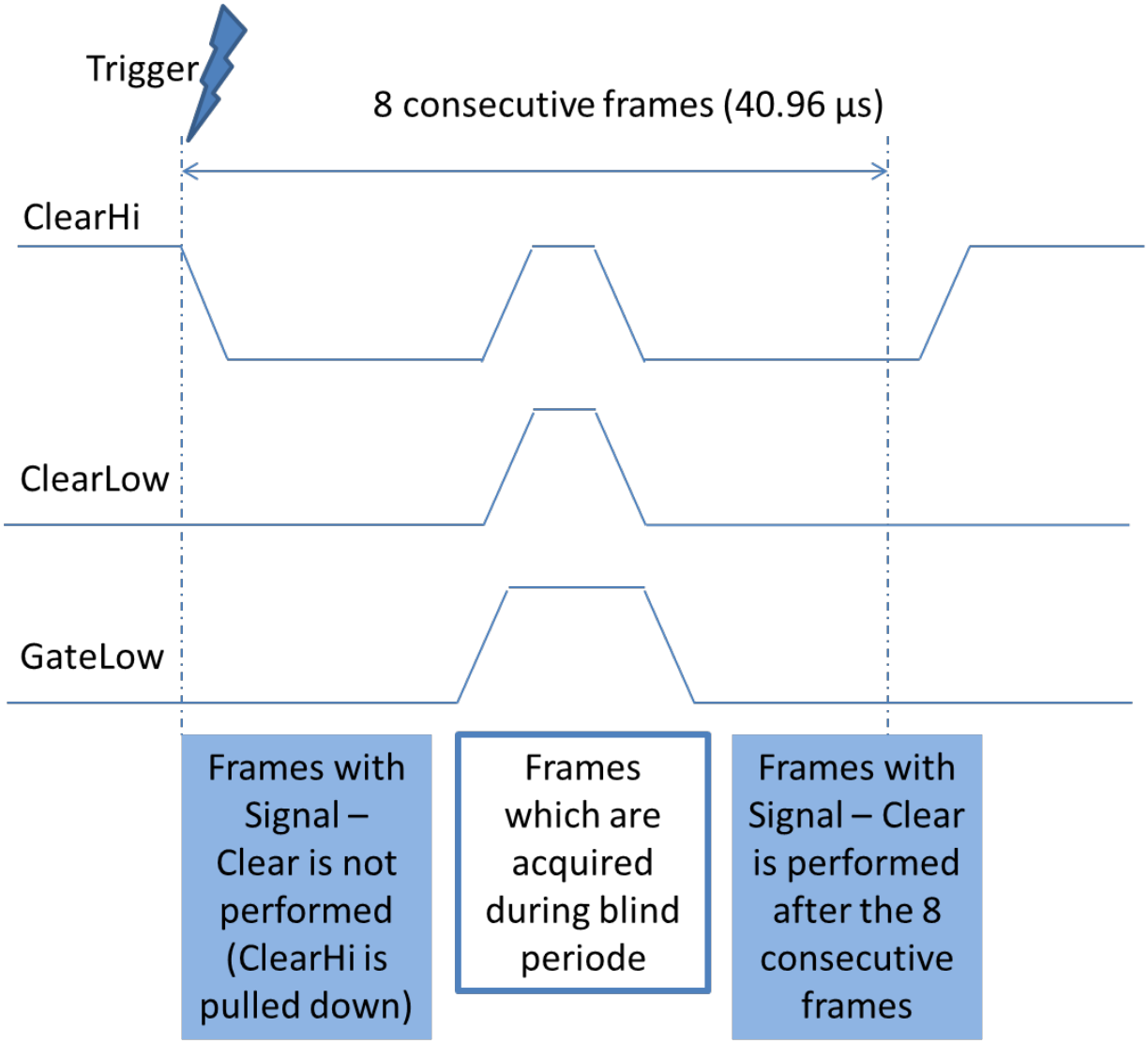
# Clear Selectivity

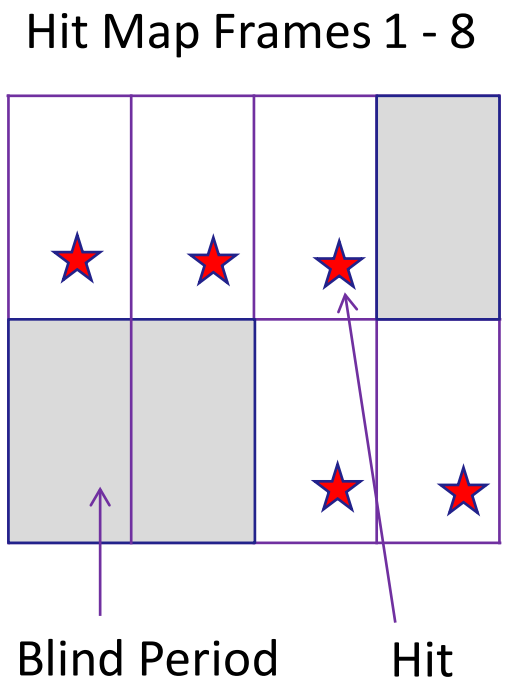



**+20V shields IG perfectly, but noise higher!!**

- Hit pixel given by track extrapolation
- Track crossed DEPFET in blind mode!!
- Require good quality of seed pixel
- MC for perfect blinding
  - Just histogram noise values
  - Using measured(!) noise distribution
- Similar results for later frames (3,4,5,6,7)

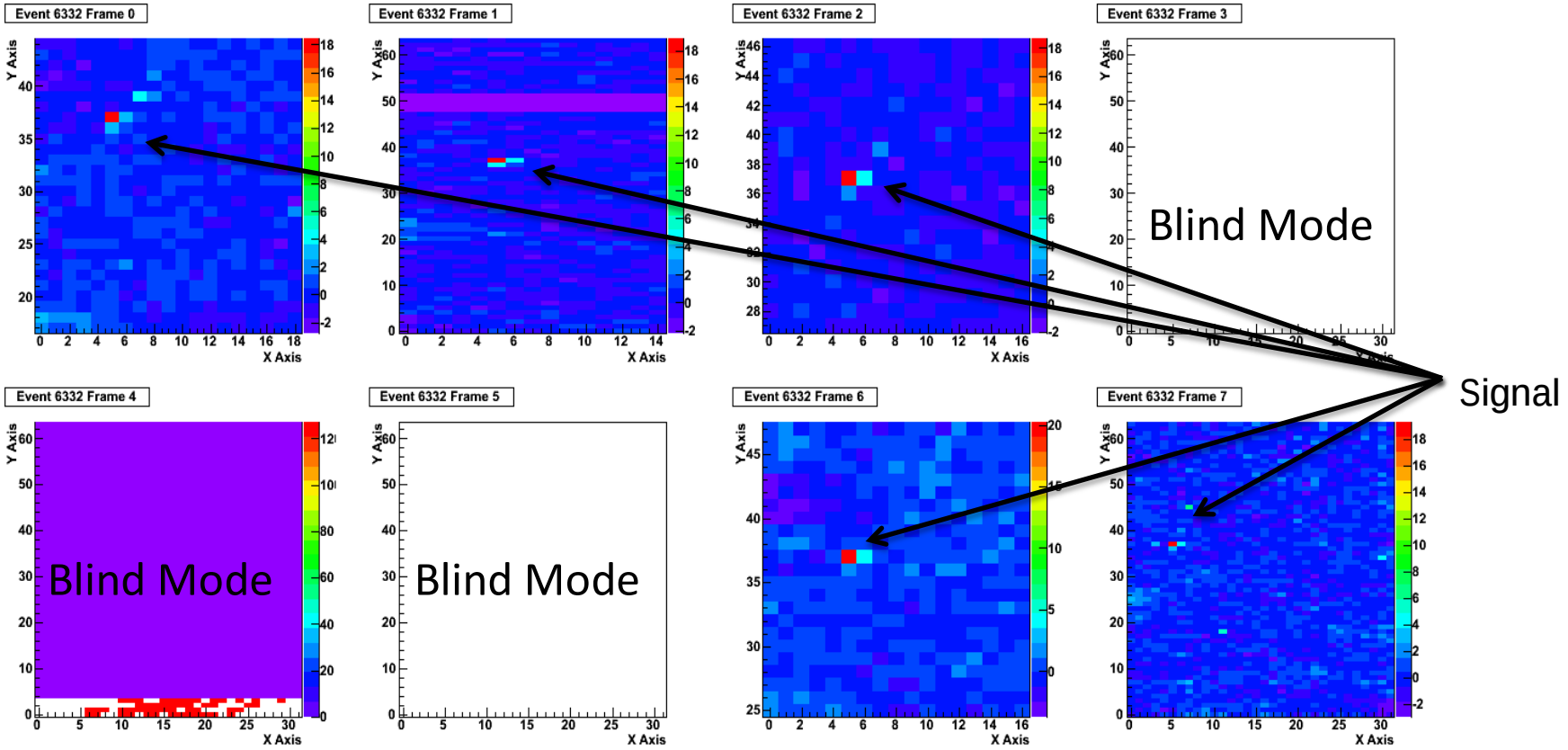
# Experiment C: Signal Charge Restore



# Data Event with track Run4263

Data after preprocessing

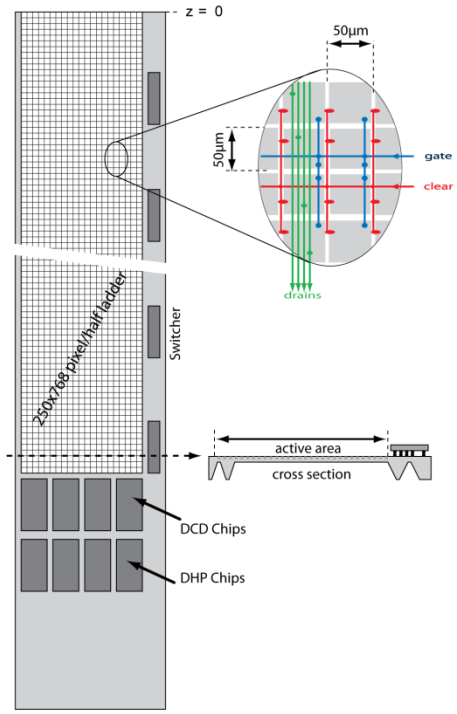


# Gated Mode - System Aspects

- clear capacitance for the large matrix compared to the PXD6 prototype used on Hybrid 4.1.11
  - Clear capacitance Large matrix: approx. 26nF (small matrix: 0.2nF)
- additional power consumption (ΔVclear:=15V, tcycl=10µs): 0.36W /half ladder
- averaged current into the clear capacitance: 30mA

→ additional coupling capacitors placed: in total 2 x 200nF (20V)

→ Tests with large PXD9 module and close to final ASICs needed to confirm metal routing (e.g. qty. of caps)



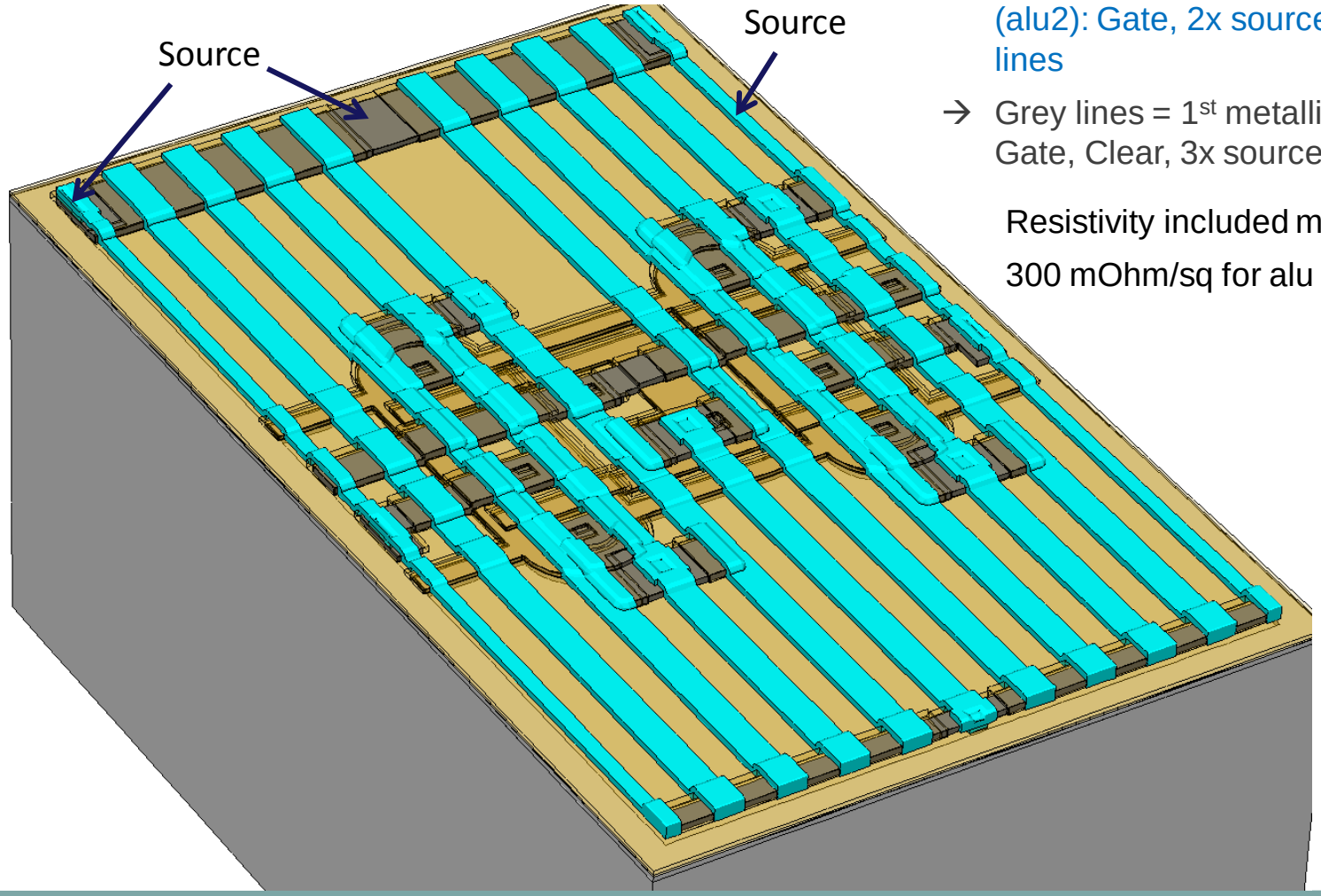
# Summary & next steps

- Concept of the gated-mode was presented
- First beam test (even with old Switcher) shows encouraging results
  - But only small PXD6 matrix used!
- Hybrid board with DCDPipeline and SwitcherB18v2 (Gated Mode) is prepared, next step is to mount a small PXD6 matrix ...
- To test the gated-mode operation on large modules the PXD9 pilot run is necessary

Thank you for your attention!

# From RC Extraction to Full Matrix Layout

- 3D model of the PXD9 design to extract the parasitic capacitance

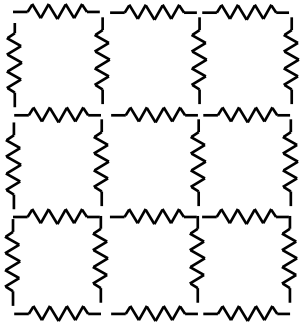



→ Light blue lines = 2nd metallization (alu2): Gate, 2x source, 8 drain lines

→ Grey lines = 1st metallization (alu1): Gate, Clear, 3x source, 4 drains

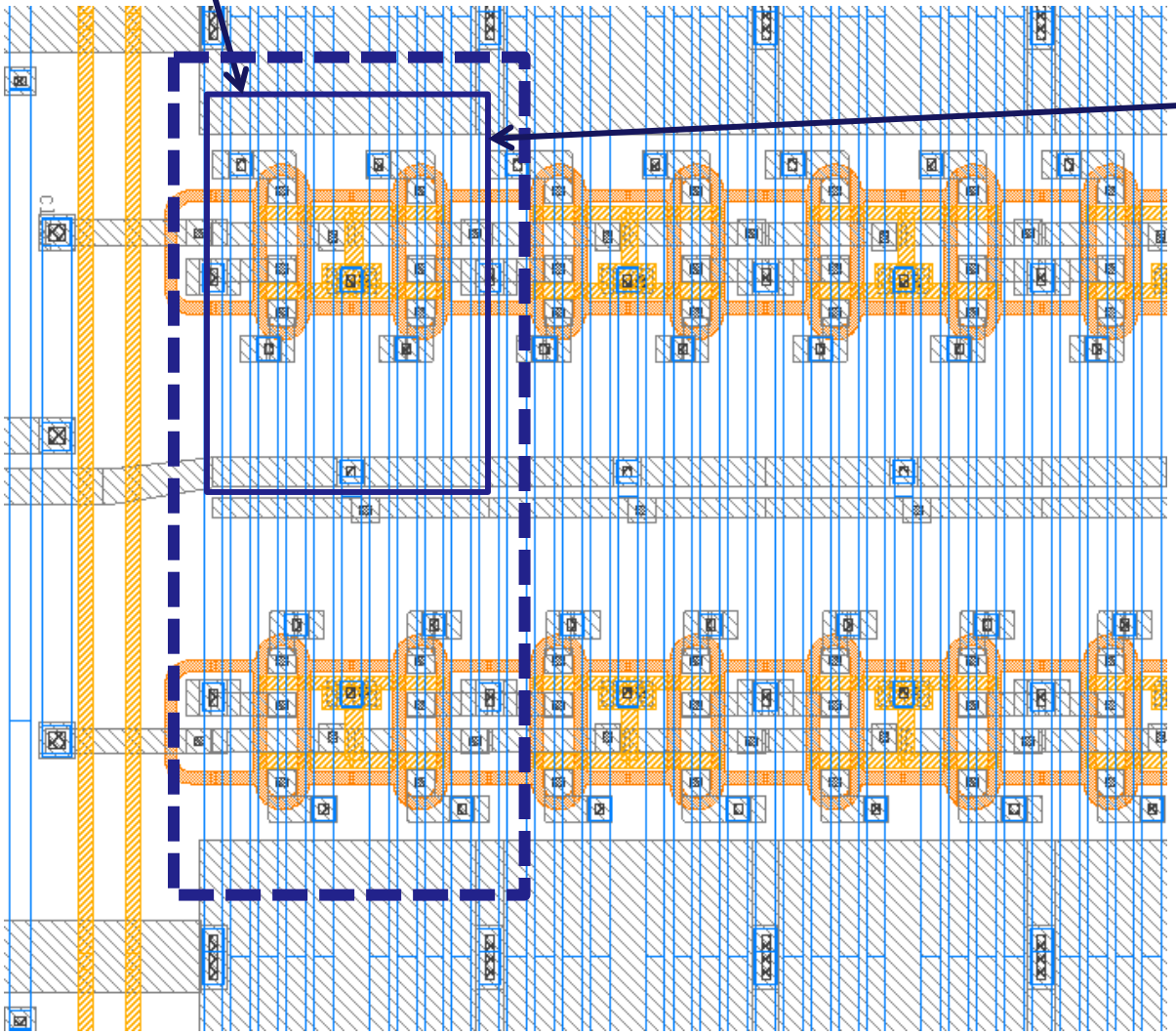
Resistivity included manually:

300 mOhm/sq for alu



# From RC Extraction to One Electrical Row

Cell for parasitic extraction

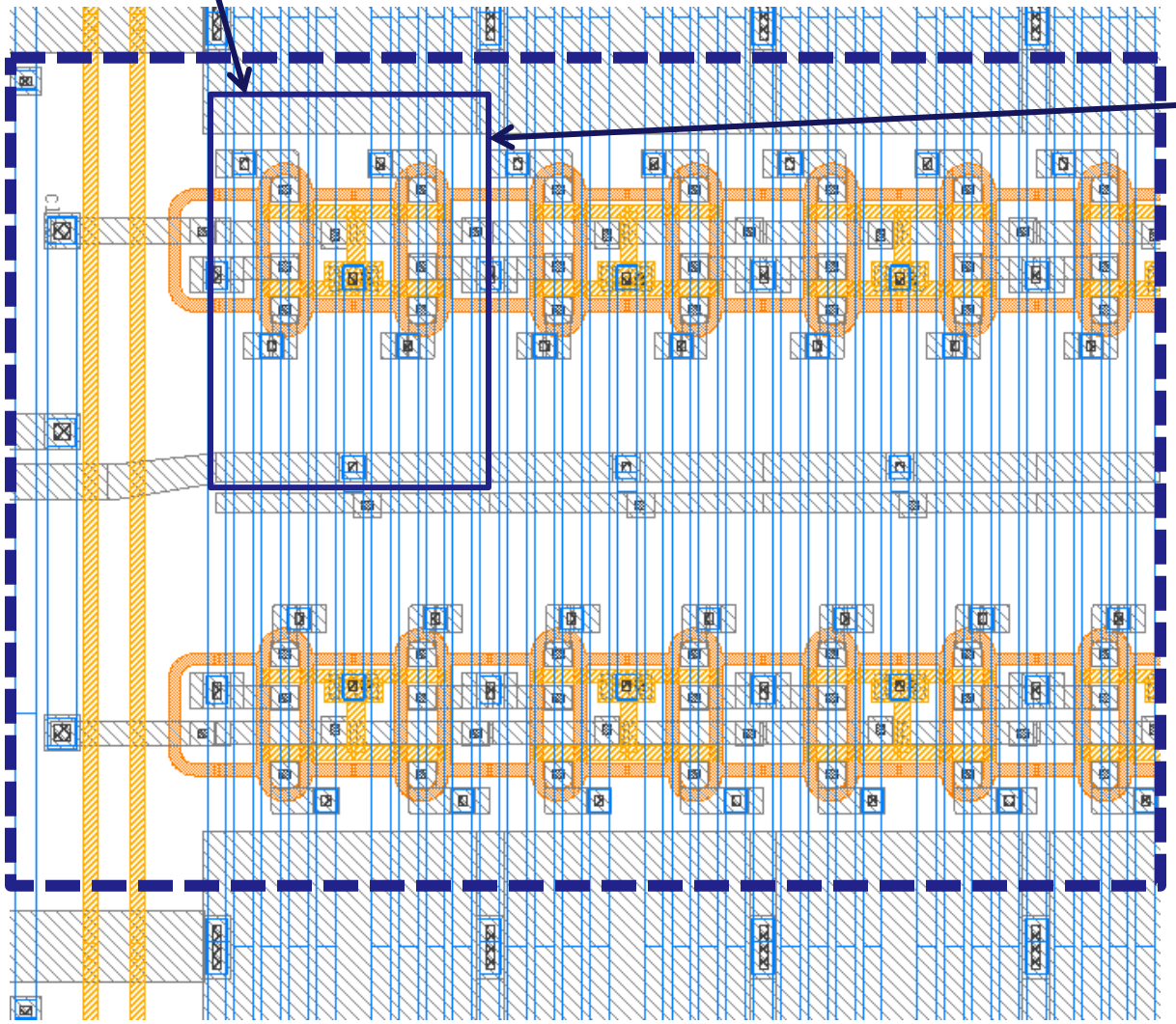


For 4 Pixels
C Clear = 542fF

For 8 Pixels:
C Clear = 1.09pf

Block of one electrical DEPFET row

# From RC Extraction to One Electrical Row



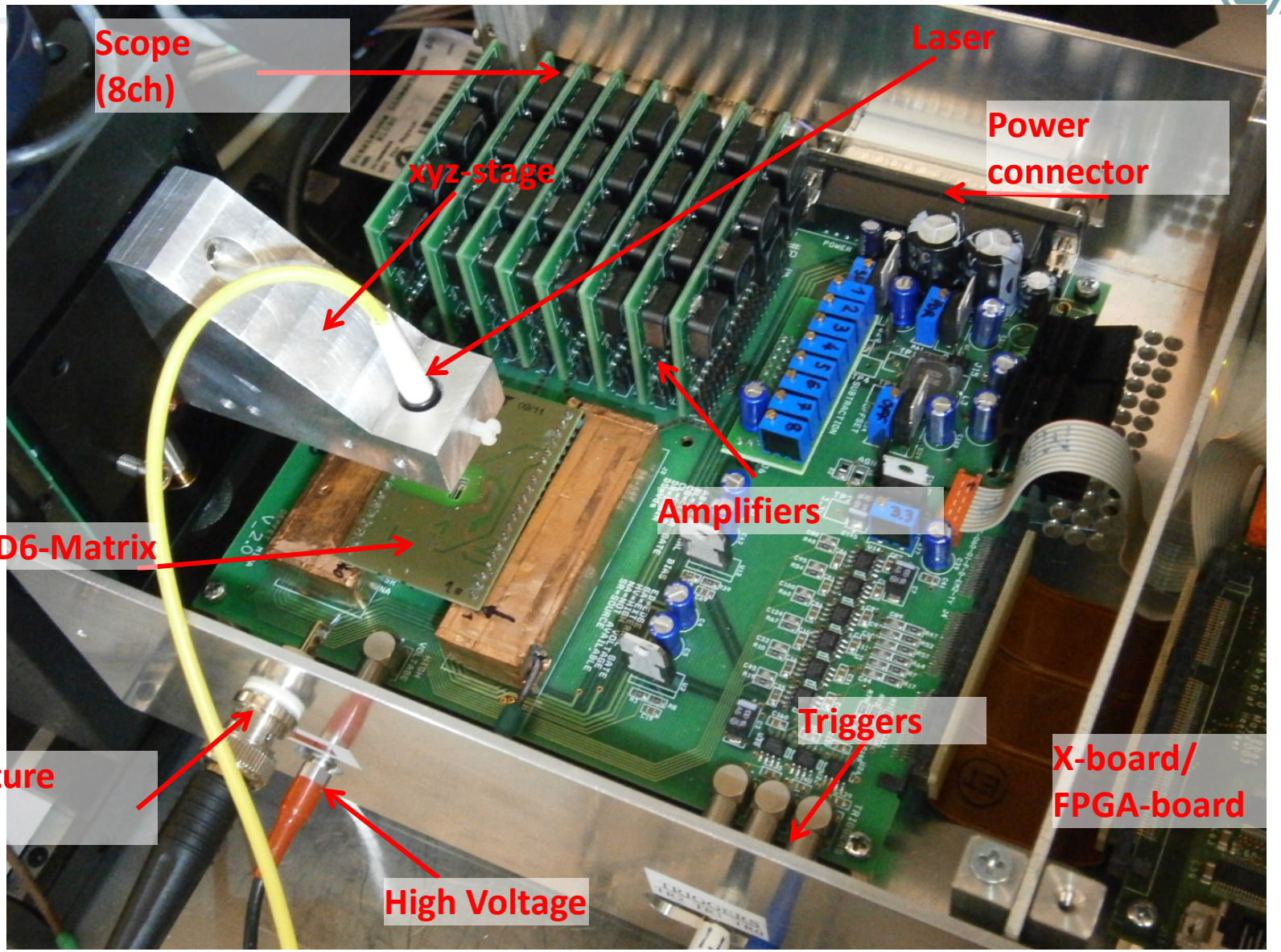

For 4 Pixels
C Clear = 542fF

For 8 Pixels:
C Clear = 1.09pf

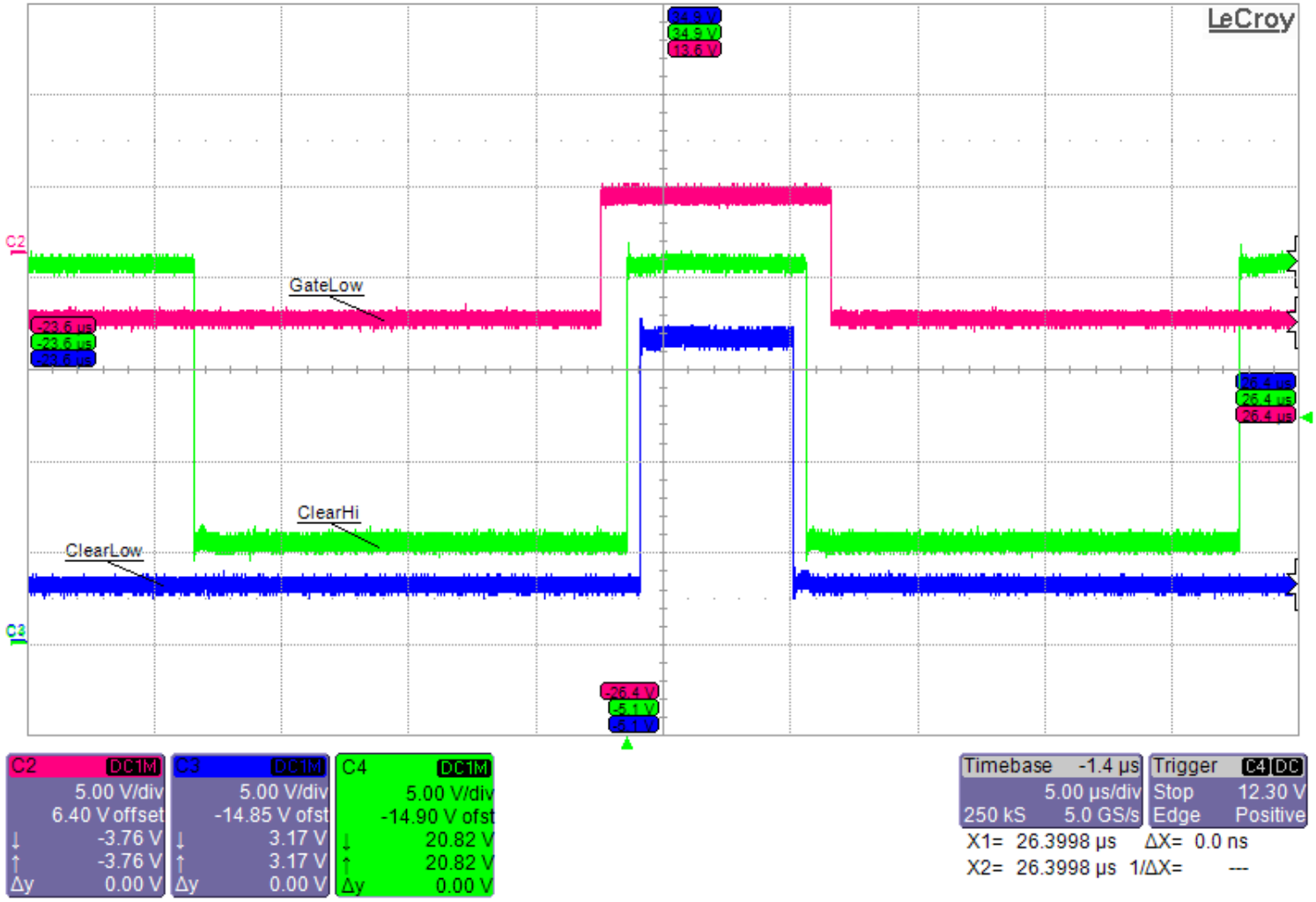
**For 1 electrical row**
**C Clear = 1.09pF *125 = 135pF**
**C Gate = 99pF**
**C Drain = 29pF**

Block of one electrical DEPFET row

# Gated-Mode DEPFET Sensor



# Experiment C: Output Pulse Generator



# Read-Out Schemes

Scenario 1)

Stop the read-out (don't clock DCD). Information is kept, but read-out cycle gets out of phase

Scenario 2)

Continue read-out (clock DCD) during blind time interval  e.g. 2µs

Scenario 3)

Continue read-out with special sequence:

- switch on one row during blind time interval