PXD9 Pilot Run Status

Belle-II PXD SeeVogh Meeting
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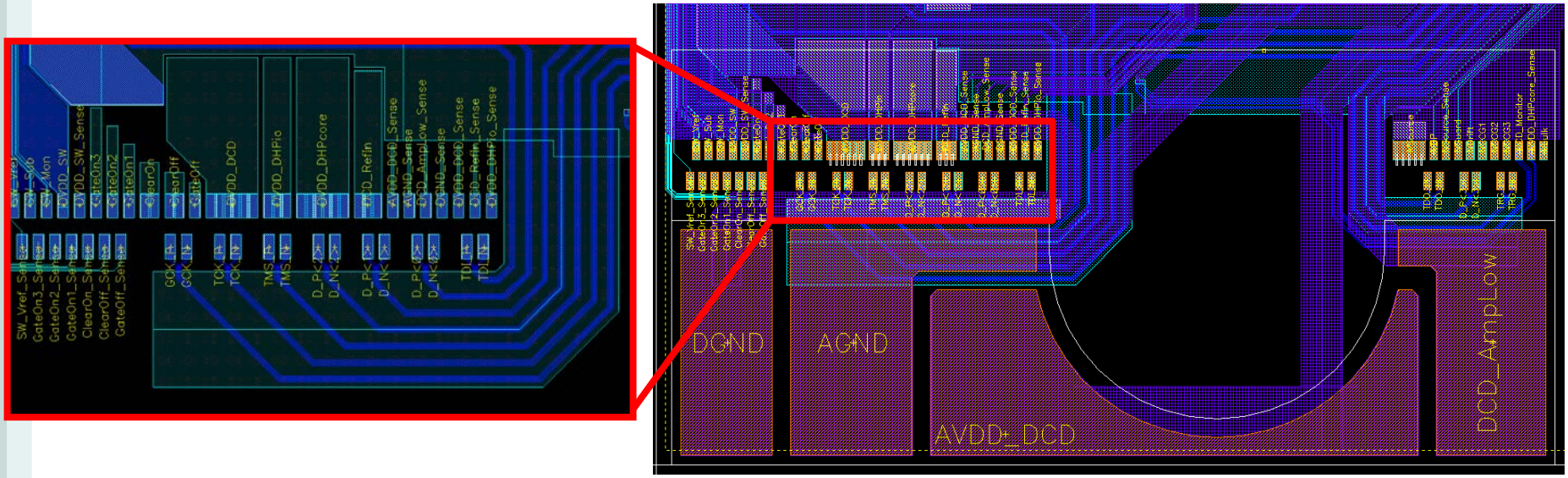
Christian Koffmane, Halbleiterlabor der Max-Planck Gesellschaft, München

On behalf of the PXD9 design team

Changes to PXD9 Layout (done by Christian Kreidl)

- Remove not used differential lines (not needed by DHPT anymore)
- Re-size the wirebond pads for several voltages
  - ▷ DHPCore ca. 700mA -> 6bonds = 117mA/bond
  - ▷ DHPIO ca. 220mA -> 3bonds = 73mA/bond
  - ▷ DCD_DVDD ca. 720mA -> 6bonds = 120mA/bond
  - ▷ RefIn ca. 200mA -> 3bonds = 67mA/bond
  - ▷ ClearOn and ClearOff -> 2 bonds for gated-mode transition
- Increase trace width of differential lines to 30µm
- Increase spacing of the termination resistors to 200µm
- Increase width of the power routing on copper



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- Schematics for all four modules (inner, outer, backward, forward) prepared by Christian Kreidl and available in Twiki
  - http://www.hll.mpg.de/twiki/bin/view/DepfetInternal/DesignResourcesPXD9
- Layout of ASICs and matrix regions are LVS and DRC clean (available in the shared Cadence design environment)
- 8 wafers: 3 hot wafers + 5 wafers from PXD9-3 batch (which had problems with some implantation)

→ From design and technology we are ready to proceed with metallization
  → Chance to feedback on the schematic and layout now.
  → Do we have to wait for the ASIC review ... or can we start processing?

Thank you for your attention!