Pilot run – test results after first metal

7th Belle II VXD workshop
and 18th International Workshop on DEPFET Detectors and Applications

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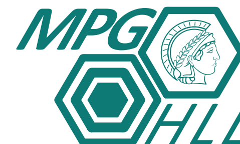
Outline

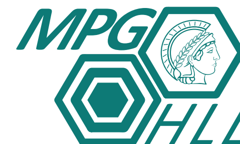


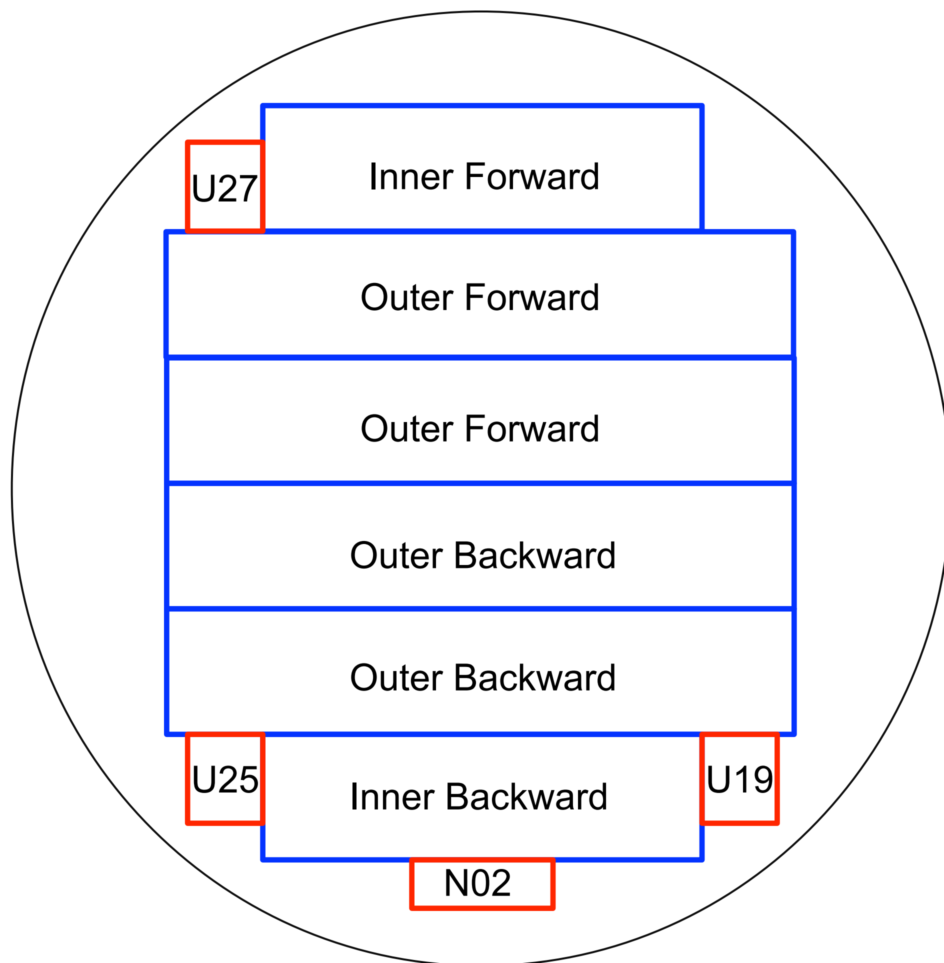
- Pilot run wafer summary and testing plan
- Test structures characterisation
- Transistor test results
- Conclusions and future developments

Pilot run wafers

Batch	W	Type	Contacts	Testing status
I	24	dummy	to poly, poxn, noxn	ongoing
I	25	dummy	to poly, poxn, noxn	ongoing
I	26	dummy	to poly, poxn, noxn	ongoing
I	27	dummy	to poly, poxn, noxn	ongoing
II	23	dummy	all	from 26.01.15
II	**30**	project	all	from 26.01.15
II	**35**	project	all	from 26.01.15
II	**36**	project	all	from 26.01.15

PXD9 wafer layout





Each wafer contains 6 half ladders:

- 1 Inner Forward (IF)
- 2 Outer Forward (OF1 & OF2)
- 2 Outer Backward (OB1 & OB2)
- 1 Inner Backward (IB)

Many test structures and small sensors to get information on the technology and to measure DEPFET parameters:

- Small PXD9 matrices
- Single DEPFETs
- MOSFETs with various technological variations
- MOS capacitors and diodes
- Contact chains
- Comb structures
- Continuity structures

Testing plan after first metal

- First yield info from test structures on:
  - status of Al1-poly/Si vias (contact chains)
  - presence of lateral shorts in Al1 (comb structures)
  - status of Al1-poly dielectric (comb structures)
  - transistor measurements (single DEPFET)

(Covered by Rainer – following talk)

- In long matrices, test of
  - discontinuities in poly1 (not repairable)
  - lateral shorts in Al1 source/clear lines due to topography (**repairable, if any!!!**)

- Preliminary calculations of DEPFET parameters (e.g. threshold voltage, internal gate potential).

(Covered by Rainer – following talk)

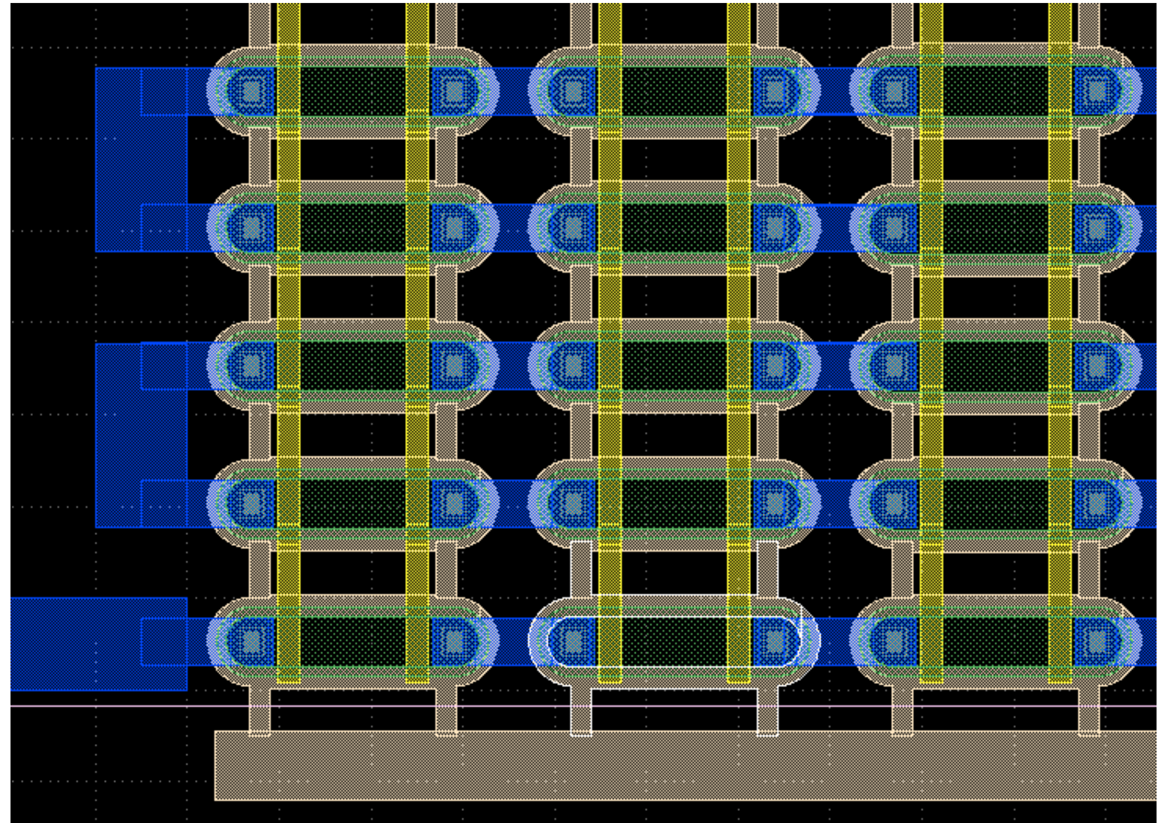
- Backside IV measurements of long and small matrices

Contact chains

Structure tested: U27 on W30.

It contains six different contact chains typologies:

1. Cu to Al2
2. Al2 to Al1
3. Al1 to poly2
4. Al1 to poly1
5. Al1 to poxn (p^+ implantations)
6. Al1 to noxn (n^+ implantations; embedded in a p-well, with an additional DEPFET-like topography)



The typologies no. 3-6 have three different contact sizes:

- 1.5 x 4 μm^2
- 2 x 4 μm^2
- 3 x 4 μm^2 (smallest size in matrix area)

- Each structure has 2000 contacts.
- The DEPFET-like type (in no. 6) has 1700 contacts.
- Each line is 60.3 mm long.

preliminary: **100% yield (one chip, i.e. 13 structures)**

Comb structures

Tested on chip U19 on W30. Info on:

- dielectric breakdown
- presence of lateral shorts in same metal

- Poly1 line width: 10 μm
- Poly1 gap size: 30 μm
  (aspect ratio comparable to PXD9 poly1)
- Al1 line width: 11 μm
- Al1 gap size: 4 μm same
  (aspect ratio as in PXD9 drift and ext gate lines)
- Poly1 and Al1 line length: 8 mm
  (12.5 mm for clear and ext gate lines)
- Total no. of poly1 lines: 199
- Total no. of Al1 lines: 531

- **Poly1/Al1 isolation yield: 100%**
- **Al1 (no) lateral shorts yield: 100%**

Continuity structures

260 crossings per segment every 20 μm

Al1 line length: 83.4 mm
(longest line 149 mm)

Tested on chip U25 on W30.
It contains 6 typologies of test structures that allow continuity and isolation measurements.
The width of the meandered line has three different sizes for each typology.

After Al1 the following structures were tested:

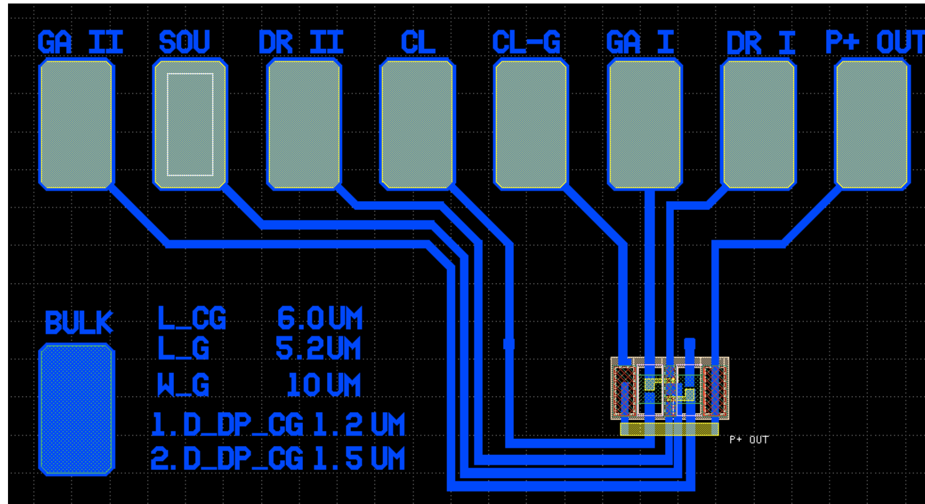
- Al1 stepping over poly1 and poly2 (most critical structure!)
- Poly1 stepping over poly2
- Al1 stepping over poly2
- Al2 stepping over poly1

None of the 12 structures tested showed discontinuities or breakdown (up to 50V)

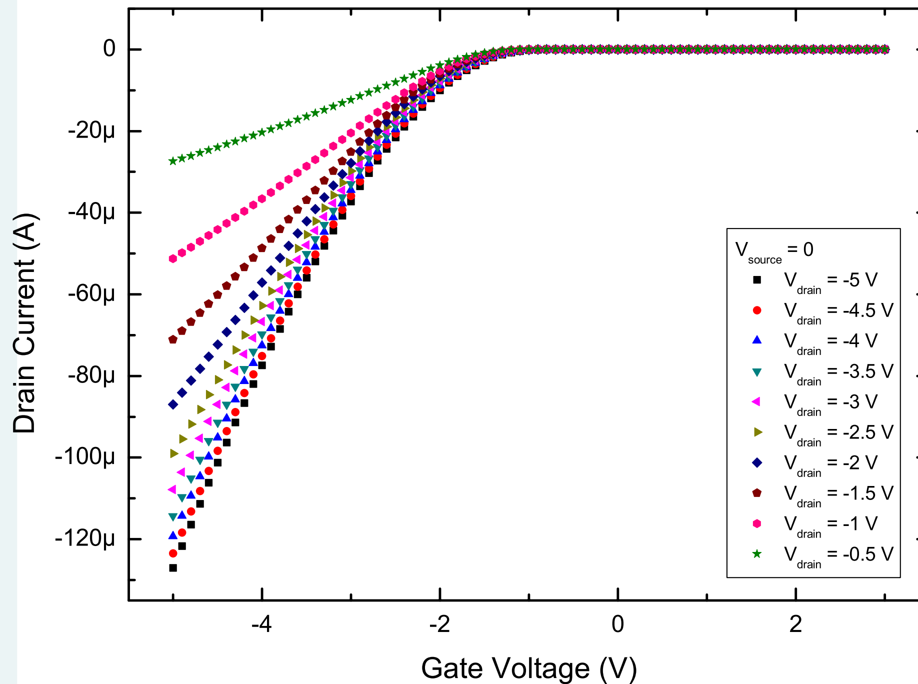
→ topography not an issue!

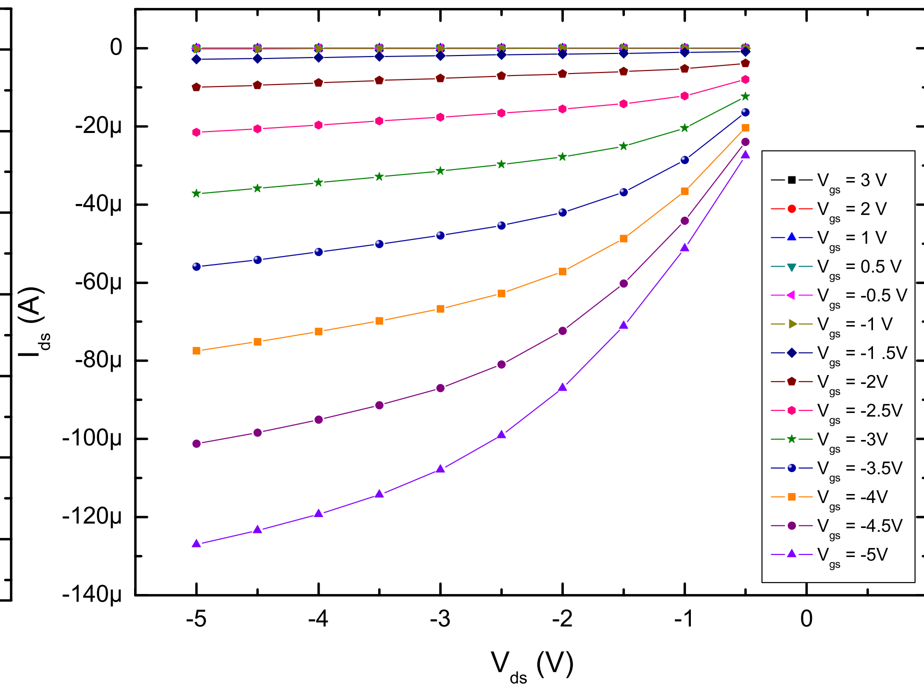
→ technology is reliable

Single DEPFET Pixel

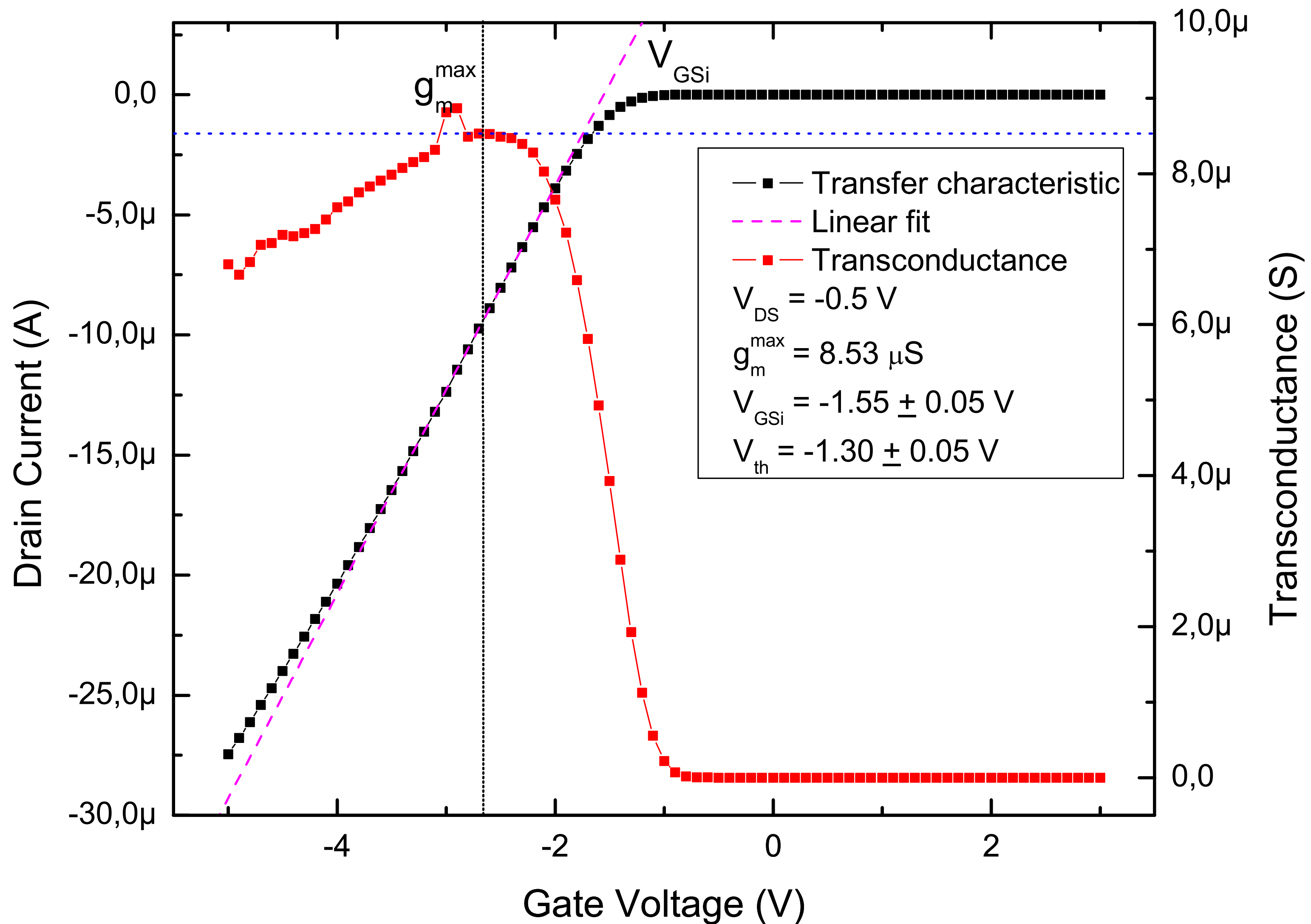


- Single DEPFET from chip N02 on W30
- Gate length, L = 5.2 μm
- Gate width, W = 10 μm
- Applied gate voltage: -5V to 3V
- Applied drain voltage: -0.5V to -5V





Single DEPFET Threshold Voltage



The threshold voltage V_{th} has been calculated with the *linear extrapolation method*, at low V_{ds} (= -0.5V).

Single DEPFET Internal Gate Potential

MPG HLL

Drain Current (A)

-40µ
-60µ
-80µ
-100µ
-120µ
-140µ
-160µ

W30, N02

V_{ig} ~ 3.3 V

0 1 2 3 4 5 6 7 8

Clear Voltage (V)

Internal gate potential extrapolated by the IV characteristic drain current vs clear voltage.

Extrapolated to V_{ig} = 3.3 V, when the internal gate is empty.

Conclusions and future developments

- PXD9 uses a technology with significant parameter changes in comparison to PXD6, among which thinner oxide and an additional Cu layer.
- The measurements presented so far, though preliminary and partial, show a robust and reliable technology and a very promising yield.
- DEPFET parameters show values in the expected ranges.
- The second batch is currently ready for testing at a semi-automatic probe station equipped with a switching system and a probe card (starting next week).
- More statistics for yield considerations will be acquired (starting next week).

Thank you for your attention!