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SI LAB Silizium Labor Bonn

DHPT Test Status

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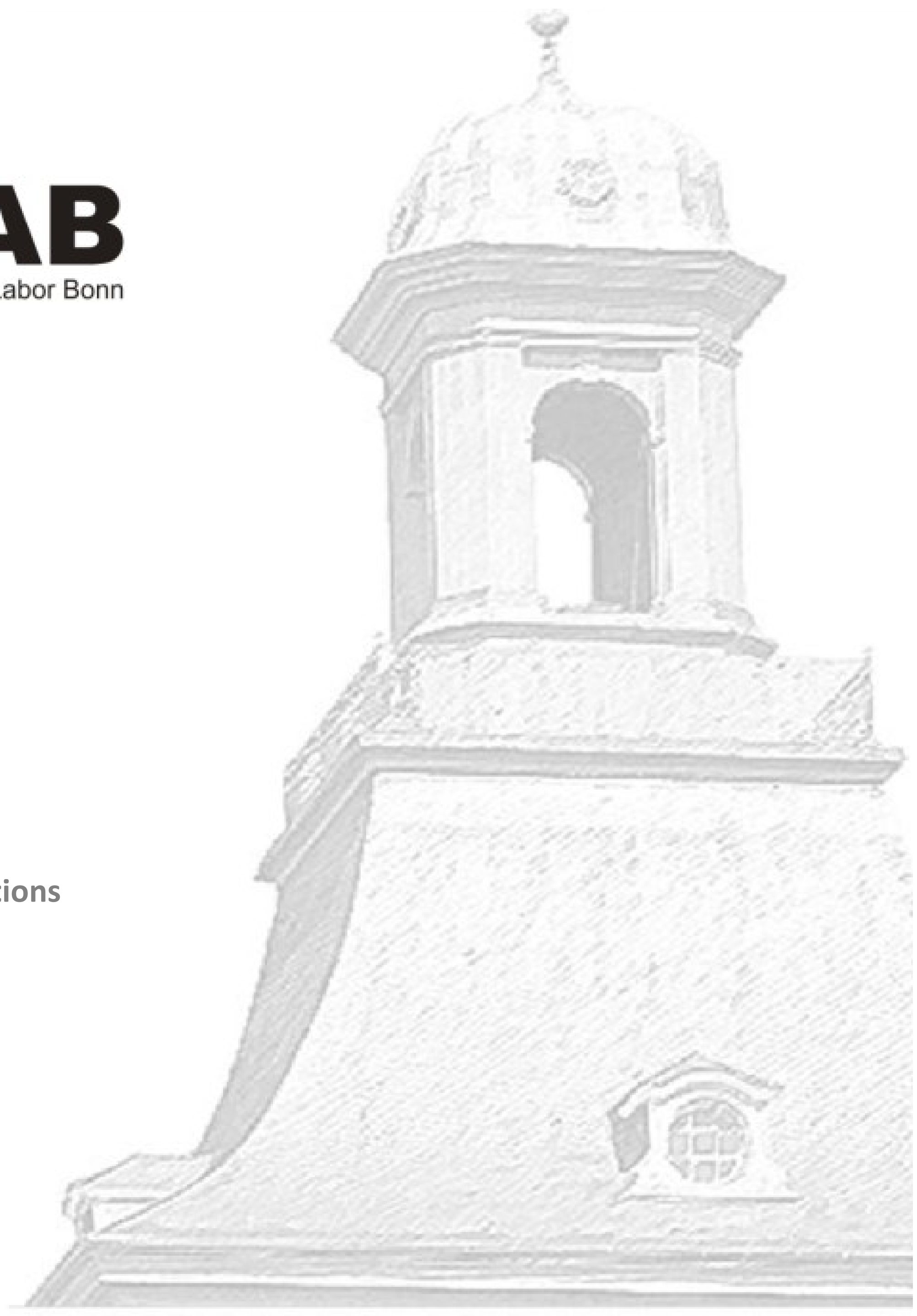

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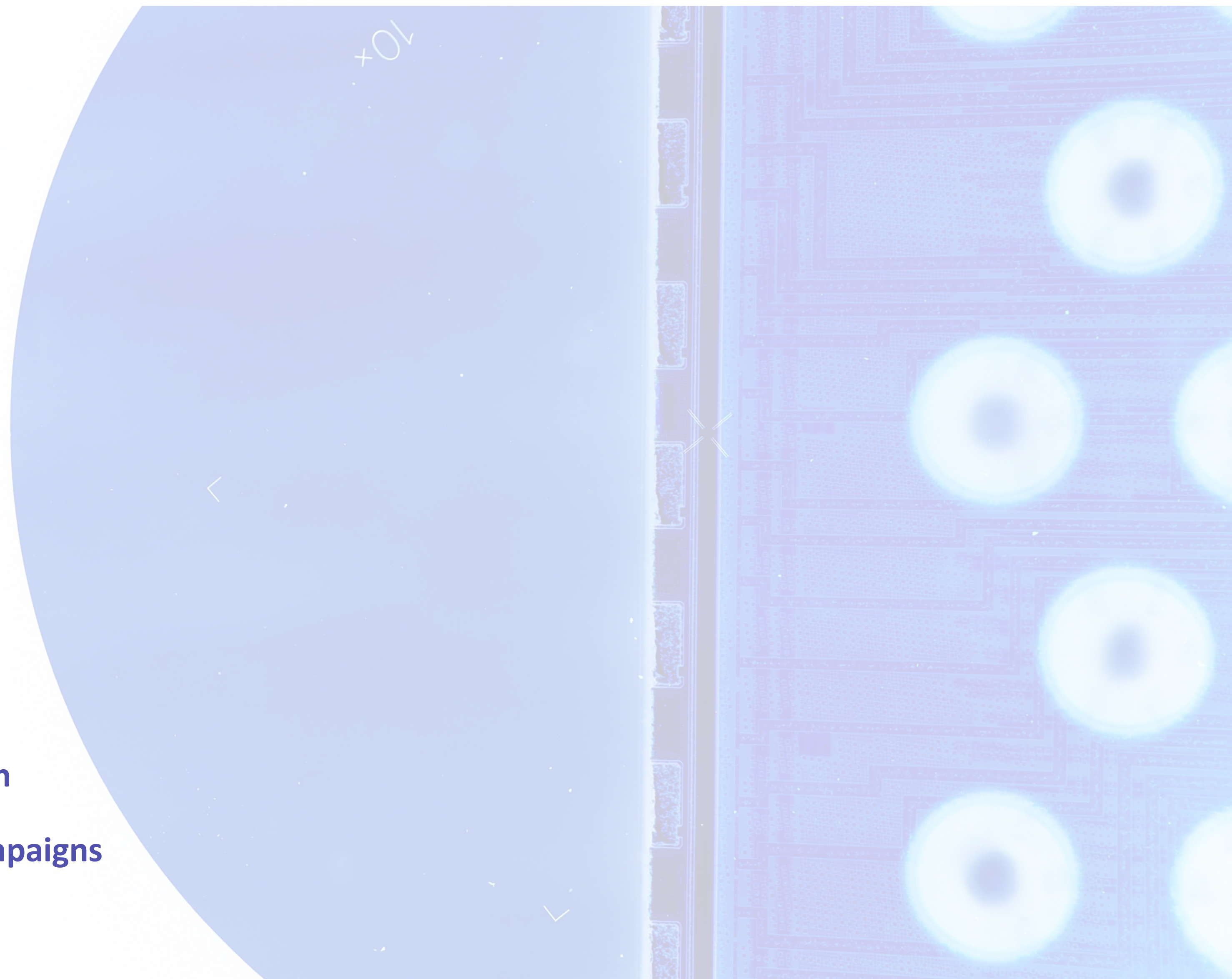

- Test System Update
- I/O Delay tests
- Memory characterization & Future Irradiation Campaigns

- Minor Hardware development since Pisa meeting
- Test system is a pcb with DHPT 1.0 and a Spartan 6 FPGA simulating the DCD and Switcher (with respect to the I/O of the DHPT)
- Most development focused on Software
  - Offset bits/ switcher sequence pattern read out via python
  - Implementation of variable DCD Vref via i2c interface (reference voltage for non standard LVDS output of the DCD)
  - DCDpp testpattern generator
  - Configuration of JTAG registers via pyEpics (although not fully tested yet)

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Software

Script based Framework
(Python, BASIL)

- PyEpics (DHH communication)

- logic test routines
  - DCDpp testpattern generator
  - Rnd testpattern generator
  - Occupancy tests
  - stability (burst)
  - SRAM error counter
  - many more

- I/O test routines
  - Switcher seq
  - Gated Mode Operation
  - DCD data DOX[7:0]
  - DCD offset bits DIX[1:0]
  - many more

- Parameter sweeps/variations
  - DCD Vref

Hardware

NeedleCard
- with mechanical support
- part of final test system
- mass testing

Data Handling Hybrid

Hybrid 5
- Wire-bond adapter with diff. clk
- DHPT 1.0
- DCDpp
- Switcher B18 v.2

I/O Delay Tests

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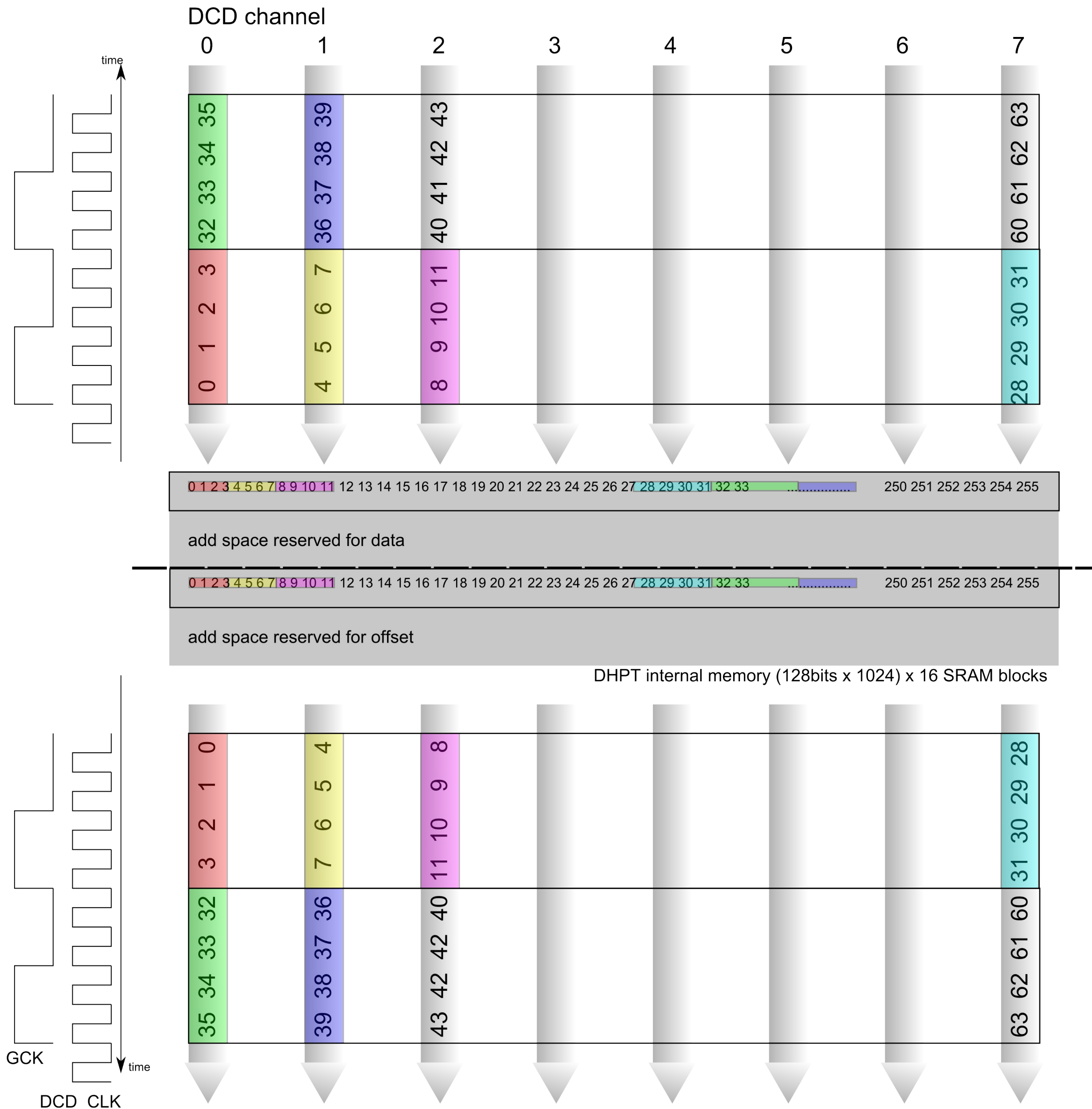

- DHPT internal data storage
- First half of the 10 bit memory address is reserved for data
- Second half is reserved for offset bits
- For each physical link (data I/O) a 4 bit delay register is assigned.
- The delays are referred to the driving clock of the I/O

I/O Dealy Tests

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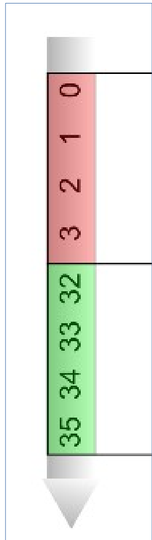
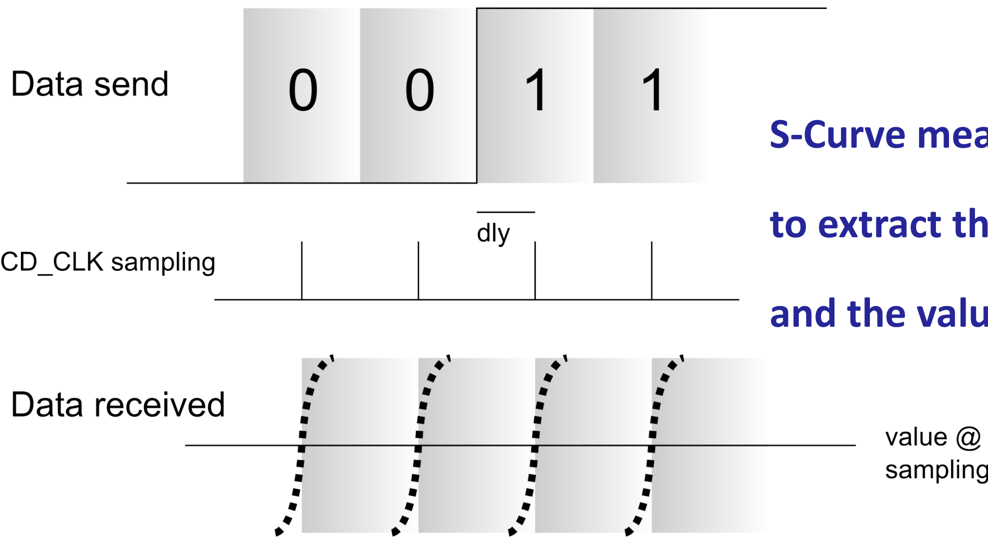


- Triggered by GCK, 4 bits are arriving after 4 DCD_CLK cycles per physical link of the channel (1 channel = 2 bit wide bus)
- Recording an offset pattern like 0x05 for the 4 x 2 bits (left picture, red) results in a sequence of ((0,0) , (0,0) , (0,1) , (0,1)) → for the LSB 0 0 1 1
- Recording the data for all delay setting of the link will result in a transition

0 0 1 1 → x 0 0 1 hence the 1 will be delays for a particular dly setting

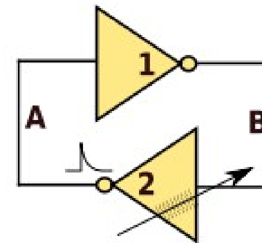


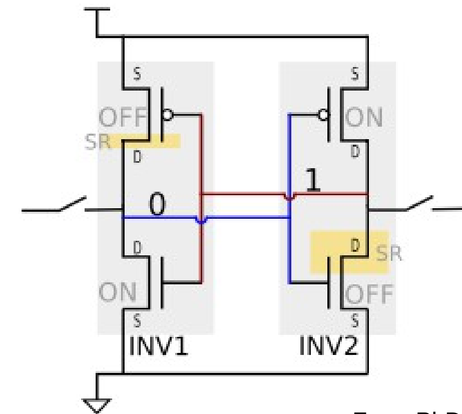
S-Curve measurement can be performed to extract the jitter (slope of the transition) and the value for one delay element (LSB)

value @ sampling

Memory and Single Event Upset (SEU)

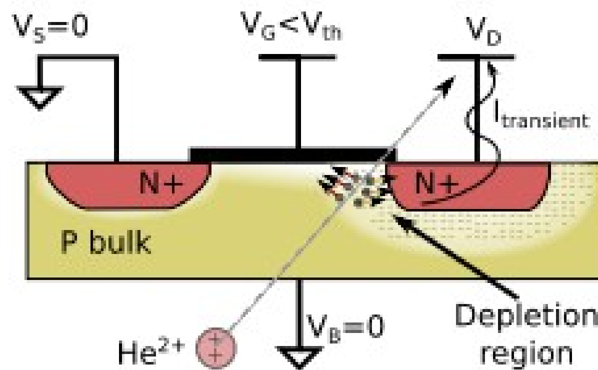
- 65 nm TSMC Standard Library SRAM cells of 0.525um² (6T)
- Two cross-connected inverters form a two state system
- State is preserved while supply voltage is applied





From PhD Thesis of
M. Lemarenko

- PN junction of the 'OFF' transistors act as charge collecting diodes



Memory and Single Event Upset (SEU)

- Quantification of SRAM properties related to Irradiation damage

  (Bit flip due to induced charge, Single Event Upset)

  - Fluence ϕ and relative bit errors (w.r.t. total number of bits) can be used to define

    SEU cross section $\sigma_{SEU} = \frac{N_{error}}{\Phi \cdot N_{Cells}}$

- From Vienna meeting 02/2012 – Expected flux of neutrons

	Switcher-B		DCD		DHP	
	-Z	+Z	-Z	+Z	-Z	+Z
Touschek	1302	3197	2976	2380	2605	2306
Beam-Gas Coulomb	2133	473	744	0	1786	297
Radiative Bhabha	1420	6398	3869	2822	5060	5805
4-fermion final state QED	1049	1023	1543	1730	1859	2100
Total # neutrons per cm^2s	5904	11091	9132	6932	**11310**	**10508**

- Neutron Irradiation campaign (in March?, with Igor)

- X-ray Irradiation for the digital processing part @ KIT (date to be defined)

Summary

- DHPT test system development still under progress (most Software)
- I/O delay measurement currently ongoing
- Irradiation campaign in near future (Neutron for SEU and x-ray for digital processing part)

Thank you

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