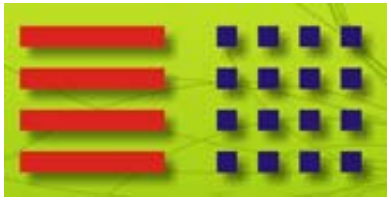


7th Belle II VXD Workshop, 18th Intl. Workshop on DEPFET Detectors and Applications

- PXD Overview-

- DEPFET Collaboration Matters
- Status of PXD9 sensors and ASICs
- Assembly Procedures
- Services, DAQ and Cooling
- Preparation for BEAST Phase 2

DEPFET Collaboration Matters

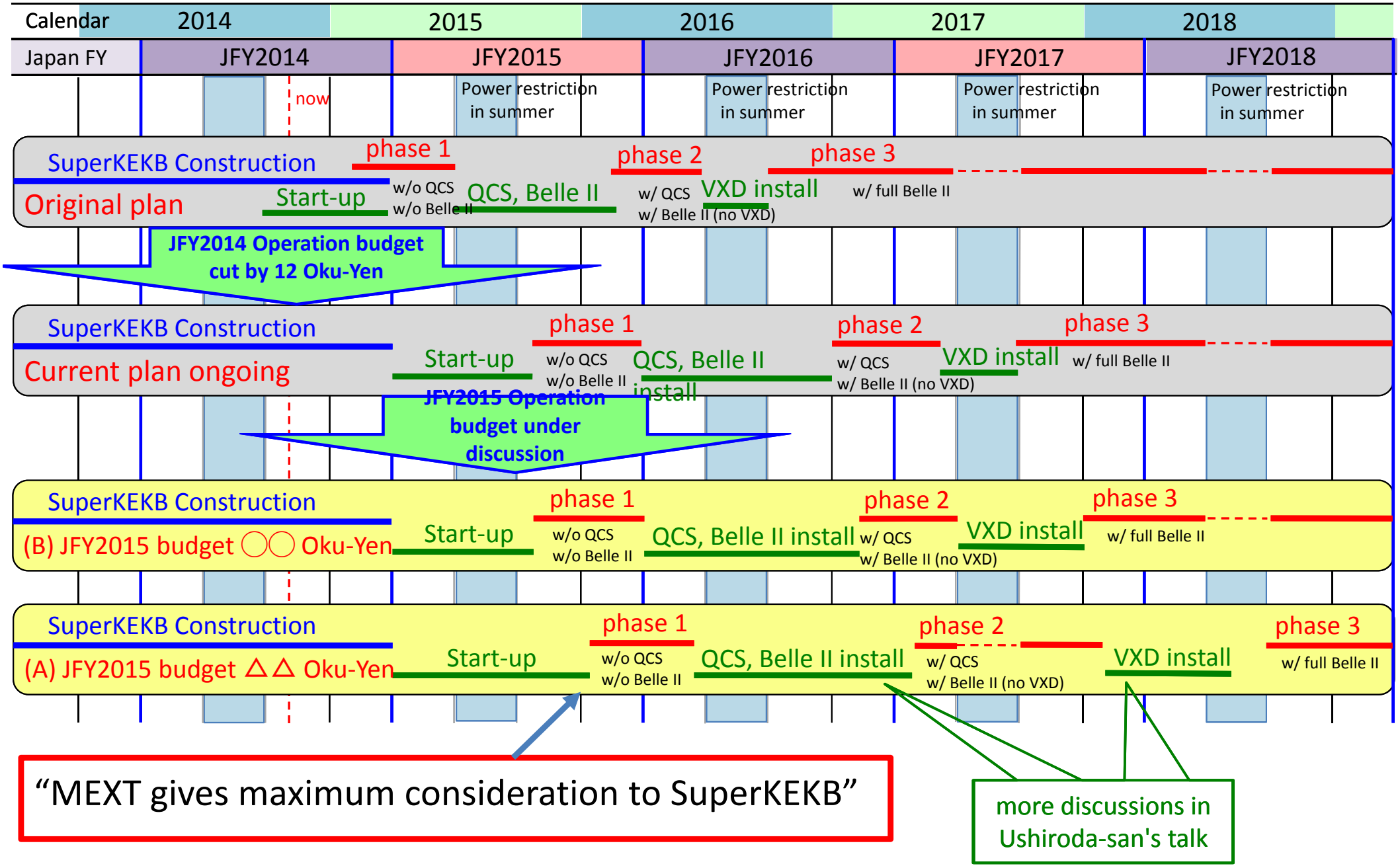
- Prof. Concettina Sfienti's group (University of Mainz, DEPFET member since September 2014) has also joined Belle II during the last B2GM (Nov. 2014)
  - Physics interest: Hadron Physics with strangeness
  - PXD Services: Slow Control
  - Presentation of plans during this meeting (M. Hoek)

- Prof. Ivan Peric left Heidelberg University, now at KIT (IPE)
  - will continue the ASIC development for the PXD (DCD, SWG)
  - (KIT is already member of DEPFET and Belle II Collaborations)

- Prof. Fischer's group (Heidelberg University) will stop ASIC development for the PXD, but concentrate on Slow Control of the VXD and Belle II (together with Mainz and TUM)

Nov. 3, 2014

SuperKEKB/Belle II Schedule

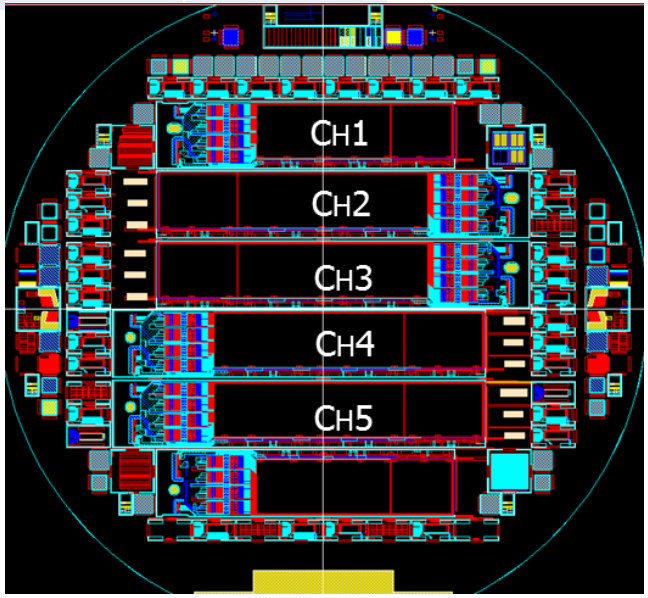


Status of DEPFET Sensors (Phase I)

	0	1	2	3	4	5	sum
Chip1	10	9	2	2	1	6	30
Chip2	16	7	1	0	0	6	30
Chip3	16	4	3	2	0	5	30
Chip4	11	4	5	3	1	6	30
Chip5	12	4	4	2	2	6	30
Chip6	15	4	2	2	1	6	30

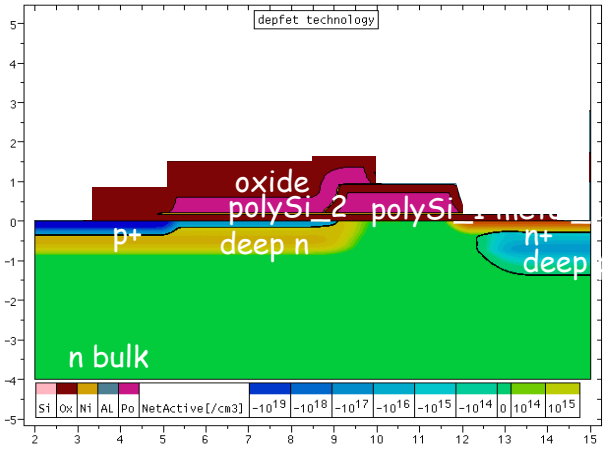
0 – no severe defects
1 – single pixel
2 –single rows and columns
3 – whole modul affected?
4 – whole module killed
5 –to be clarified

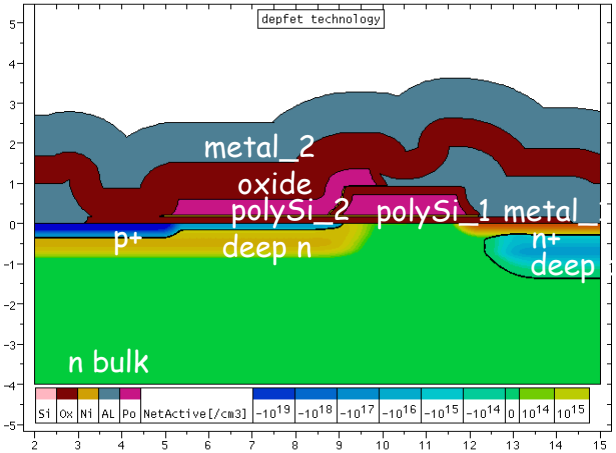
PXD9 wafer yield > 60 %

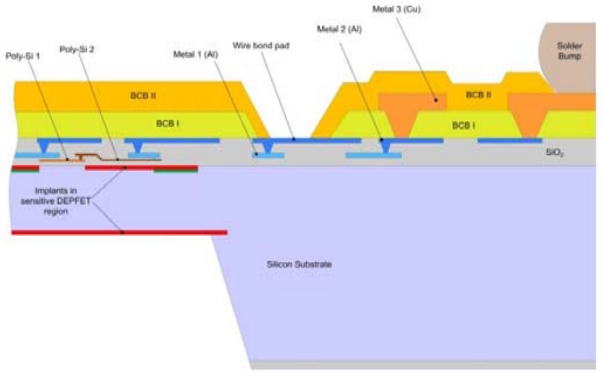


Metallization: Phase II, a Crucial Next Step

- Technology development for the PXD9 metallization via “EMCM”
- Verification: EMCM Version 4 tests finished, excellent yield, reproducible results







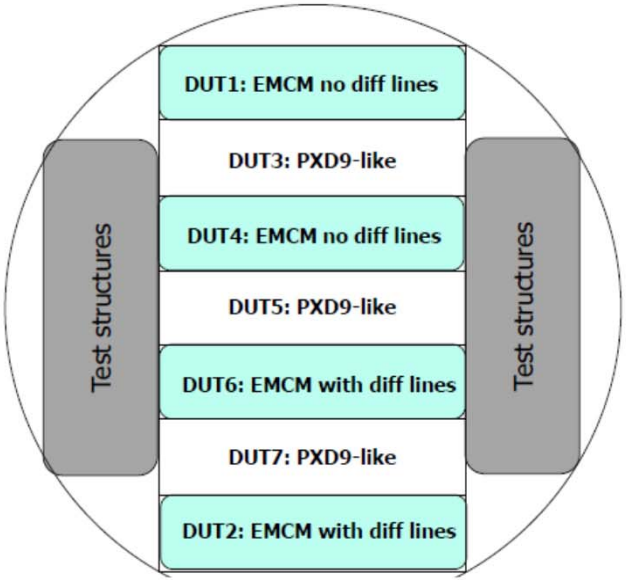
Phase I – before metal
- Implantations
- Polysilicon
- Dielectric depositions

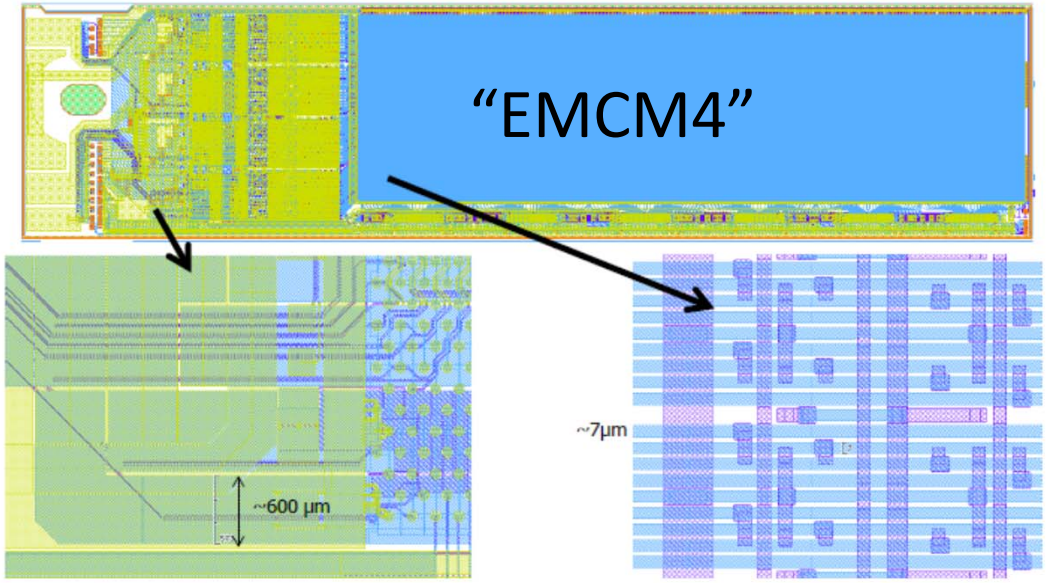
Phase II - Alu
- Metal 1
- isolation
- Metal 2

Phase III – thinning and Cu
- Handle wafer removal
- Dielectric deposition
- Metal 3
- Passivation

☑ Phase II:EMCM production(s) for Alu/Cu

Status of Metallization (Phase II)





Wafer	DUT1	DUT2	DUT3	DUT4	DUT5	DUT6	DUT7
24	0	0	0	0	4	0	0
25	4	0	2	0	0	0	0
26	0	0	0	0	0	0	0
27	0	0	0	0	4	0	0
28	0	2	0	0	0	0	0

2 = small defects, module operational

4 = lethal defects, module probably "dead"

Yield 91%

Sensor Count: Safety Factors

Yield estimate after metallization (Phase II): = 0.55

- Need a safety factor of **1.8** for the rest of the production steps

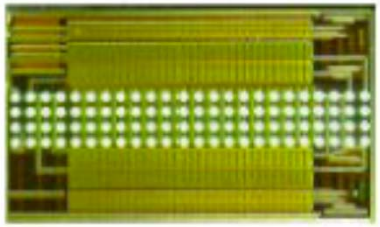
	Class 0/1	Class 2-5	Sum	PXD	Safety factor
inner	36	20	56	16	2.3
outer	70	43	113	24	2.9
Sum	106	63	169	40	2.7

Taking into account class 0 and 1 only

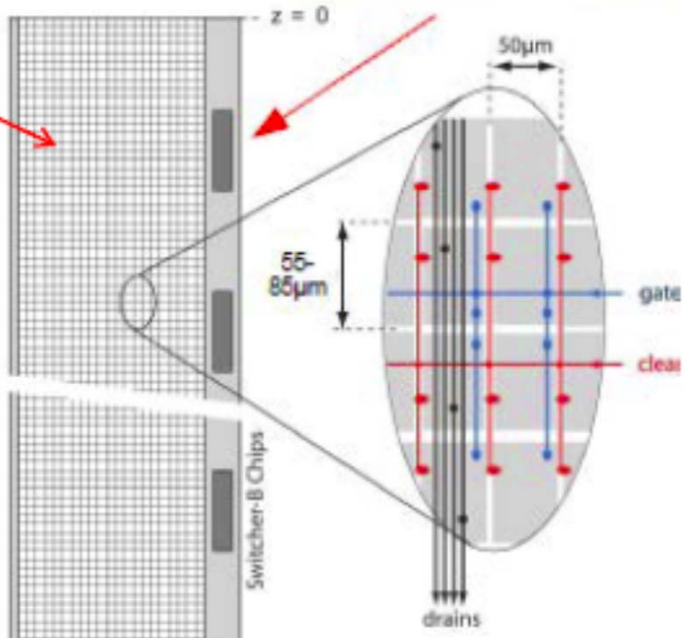
Pilot run with 3 “hot” wafers (10% of total wafers)

Status of ASICs

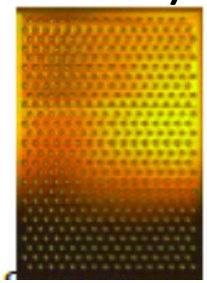
Switcher (Gated)

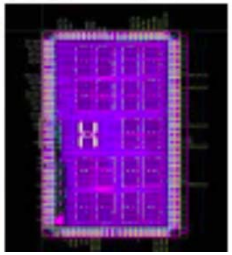


DEPFET Sensor



DCD (pipe -line)





DHP (1.0)

- 2nd generation ASICs
- used in electrical tests
- some smaller issues found
- will be used also for the **pilot run production**

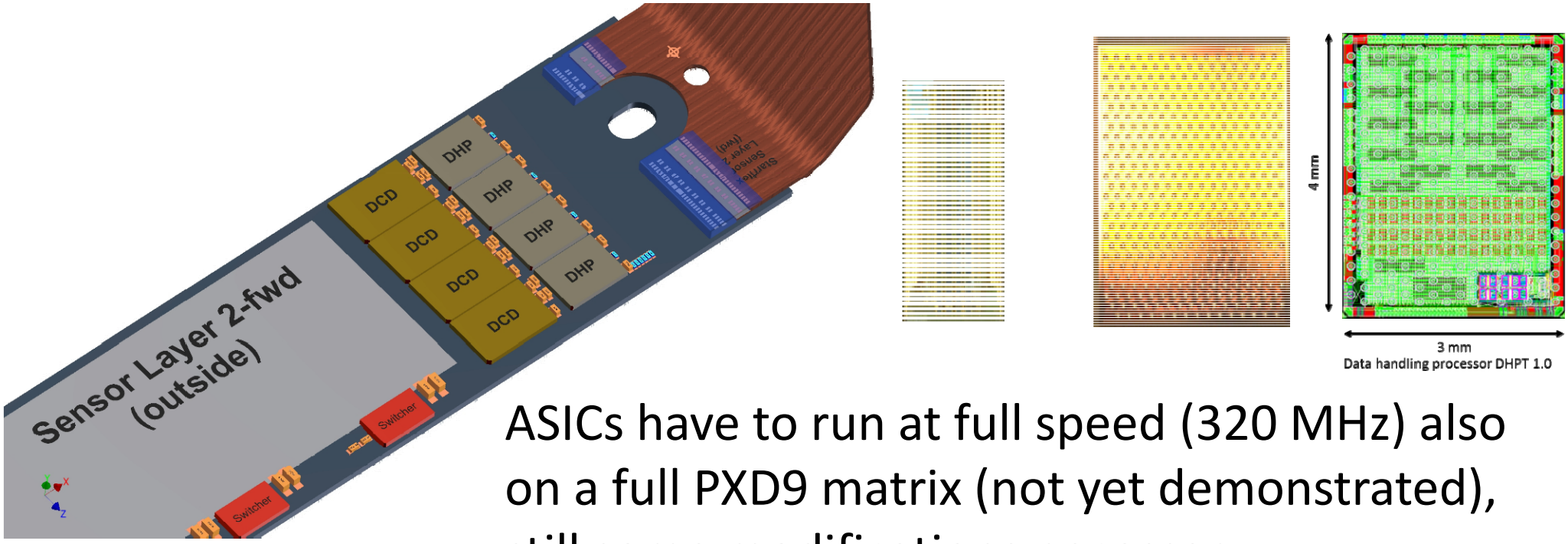
Some concerns:

- bumping of switchers
- testing of ASICs before flip-chipping

Needed for final production:

- 1080 SWG
- 720 DCDpl
- 720 DHPT

Status of ASICs



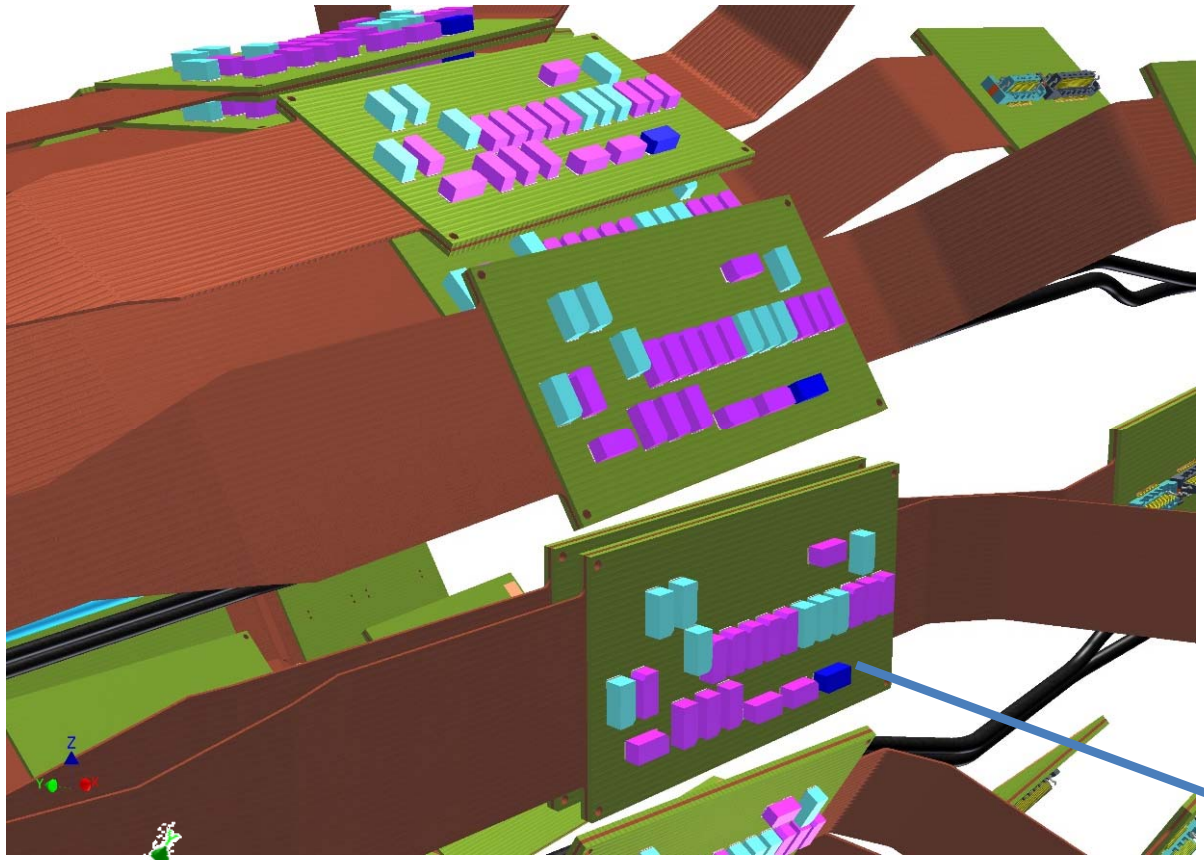
ASICs have to run at full speed (320 MHz) also on a full PXD9 matrix (not yet demonstrated), still some modifications necessary

Gated Mode operation has been demonstrated on PXD6 matrices recently with full speed using DCDpl and SWG (see Edi's talk)
- needs to be verified on (large) PXD9 sensor.
- final submission of ASICs planned for end of June 2015

(**after** pilot run !)

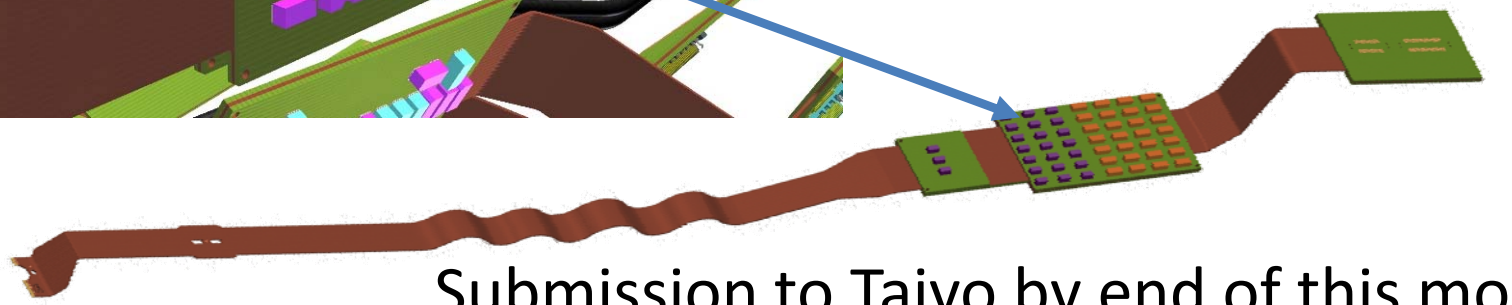
Status of Kapton Cable

Final design of Kapton cable (“outer BWD”), including passive elements, is nearing completion (4 types: FWD, BWD, inner, outer)



FWD and BWD sides different geometry (shown here is the FWD side)

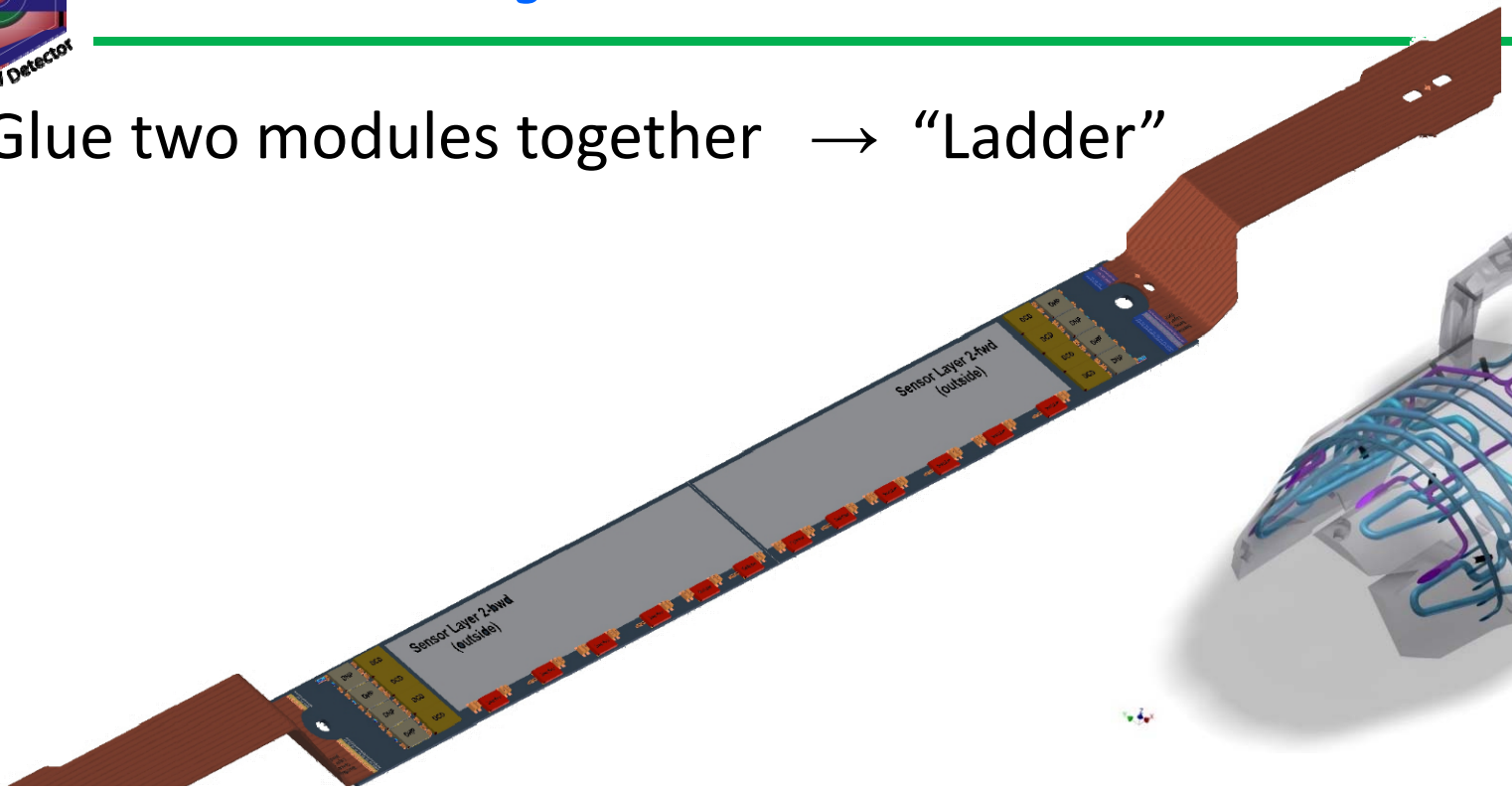
Passive elements (capacitors) necessary for Gated Mode operation



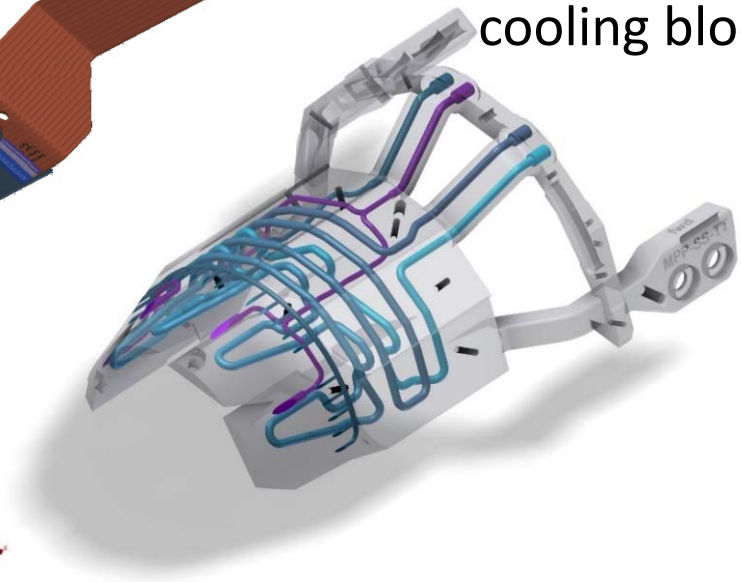
Submission to Taiyo by end of this month

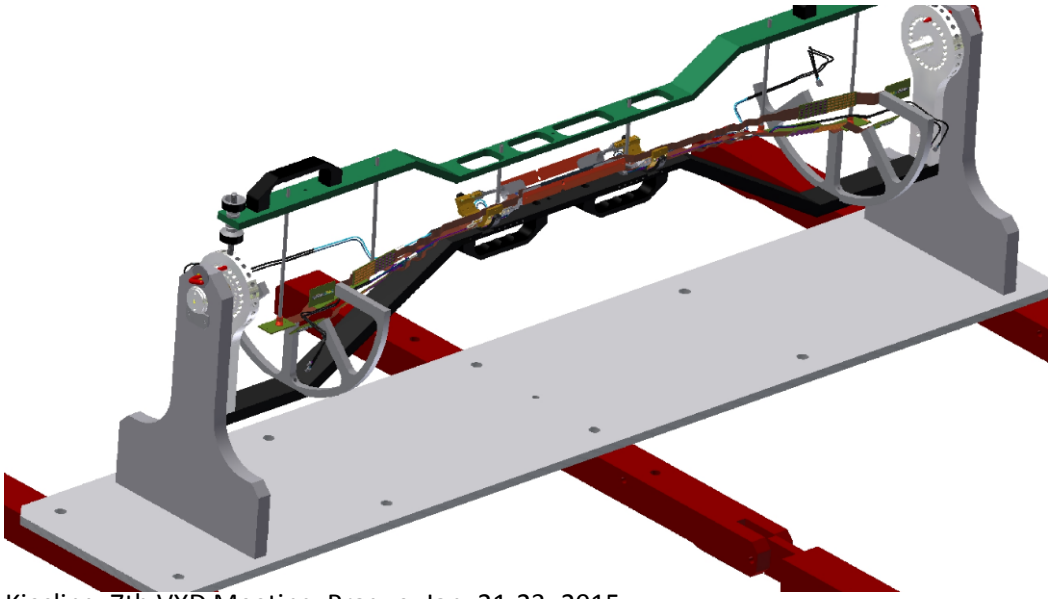
Asssembly Procedures

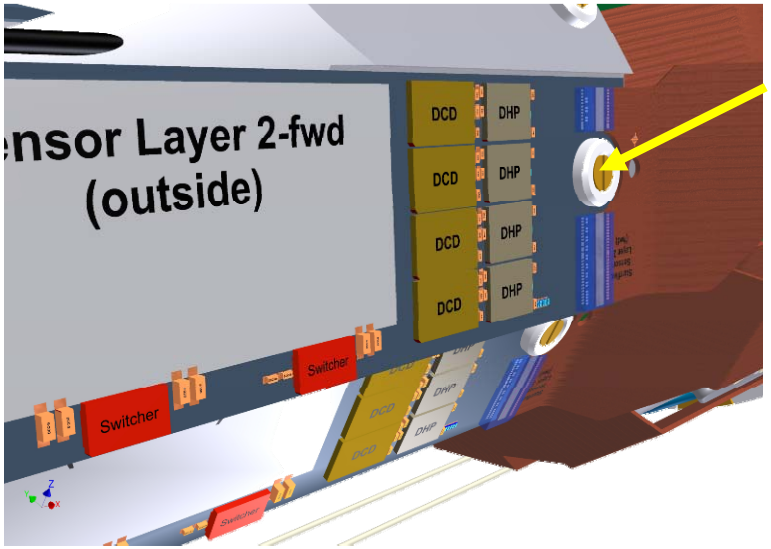
Glue two modules together → "Ladder"



Support- and cooling block







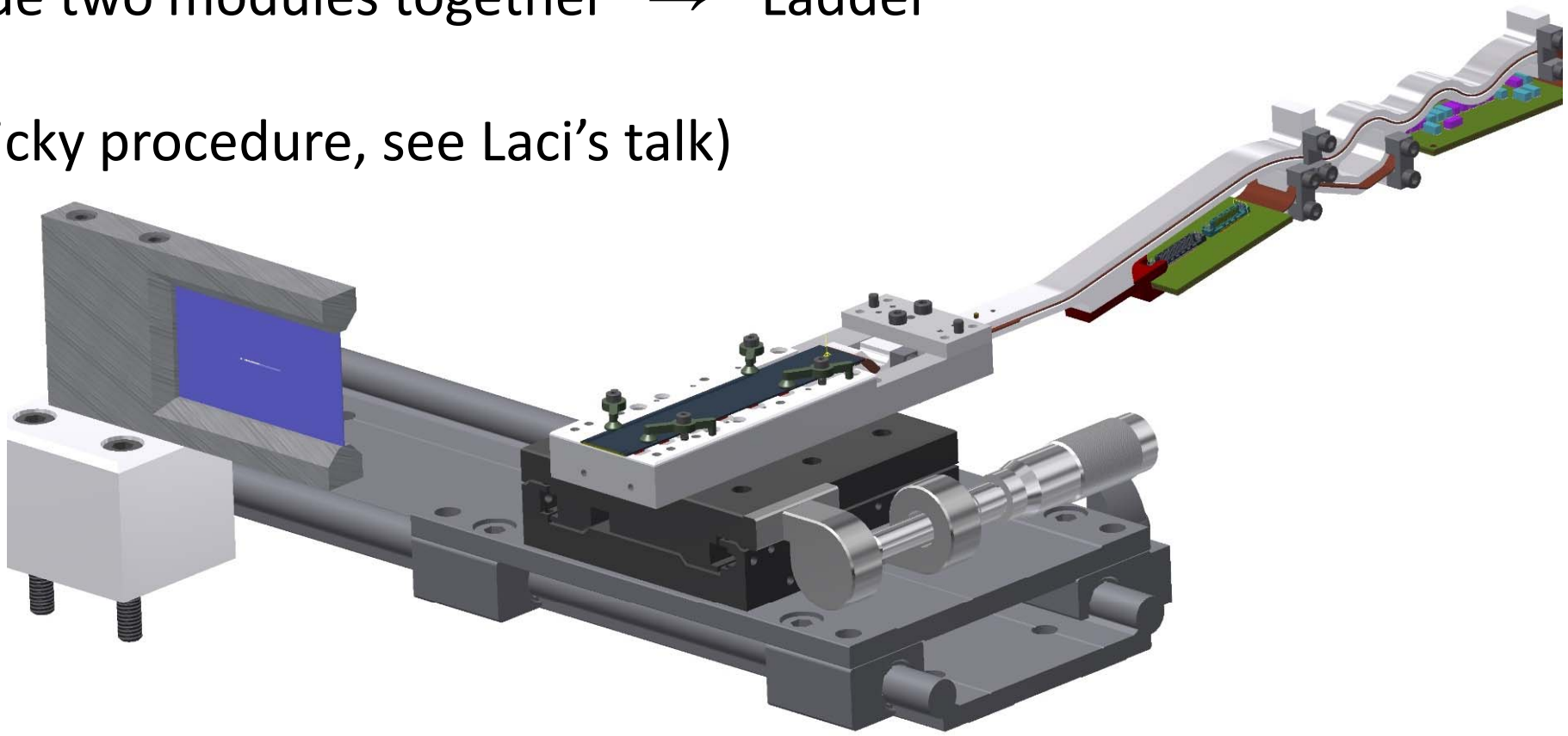
15 mNm

Asssembly Procedures

Complicated set of jigs necessary for the various production steps

Glue two modules together → "Ladder"

(tricky procedure, see Laci's talk)



Highest priority in the mechanics design right now: Tscharlie is 100% on it

Steps During PXD Production

Item	Where
DEPFET Sensor (Phases I, II and III)	Semiconductor Lab (HLL)
Flip chipping of ASICs	IZM Berlin
mount SMDs (classify, no immediate rework)	NTC Valencia & IFIC V.
Add Kapton cable, wire bonding	MPI Munich
Gluing of two modules (= „ladder“)	MPI / HLL
Assembly of PXD half shells	MPI Munich
Commissioning PXD	MPI Munich
Assembly of PXD and Beam pipe	KEK clean room (B1)
Completion of assembly with SVD (= „VXD“)	KEK clean room (B1)
Commissioning of VXD	KEK clean room (B1)
Installation of VXD into Belle II	on SuperKEKB beam line

Services for the PXD

- DHH System: nice progress, ready for series production
  but option considered to go optical from docks to the DHH/DHHC crates on top of Belle
  (see Igor's talk)

- P/S System: nice progress, ready for series production
  (see Stefan's talk)

- PXD-DAQ system: nice progress, new carrier boards
  (see Sören's session)

- PXD data reduction system (DATCON and ROI finders) under development

IBBelle CO2 System for VXD

ction box

BD016
PT116 / PT316
TT116 / TT316
⅜”
16
HX036
MV018
MV017
Dummy load
(testing only)
½”
MV036
36
FL018
FL017
EH117
TT117
TS117
BD036
PT136 / PT336
TT136 / TT336
TTz36 (DCS)
BD020
PT120 / PT320
TT120 / TT320
TTz20 (DCS)
20
¼”
⅜”
AV017
MV035

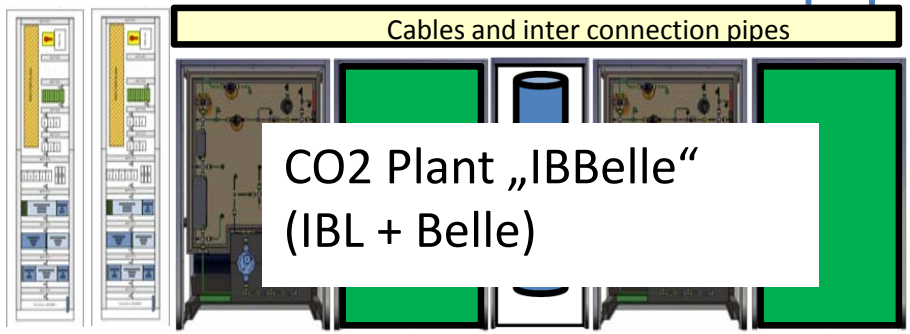
¼”
Manifold box
⅜”
½”
DN40
DN40 vacuum
06
EH122
TS122
DCS:
TTa24 - TTn24
(FTa24 - FTn24)
04
MVa24 - MVn24
nc
EV608
10
VP610
12
VP612
PT610
TT610
PT612
HX012

vacuum isol.

Two-stage dry volume
PXD / SVD

14 staves (a-g),(7 flow pairs)
(10x BW flow / 4x FW flow)

Flex
lines
~15 m



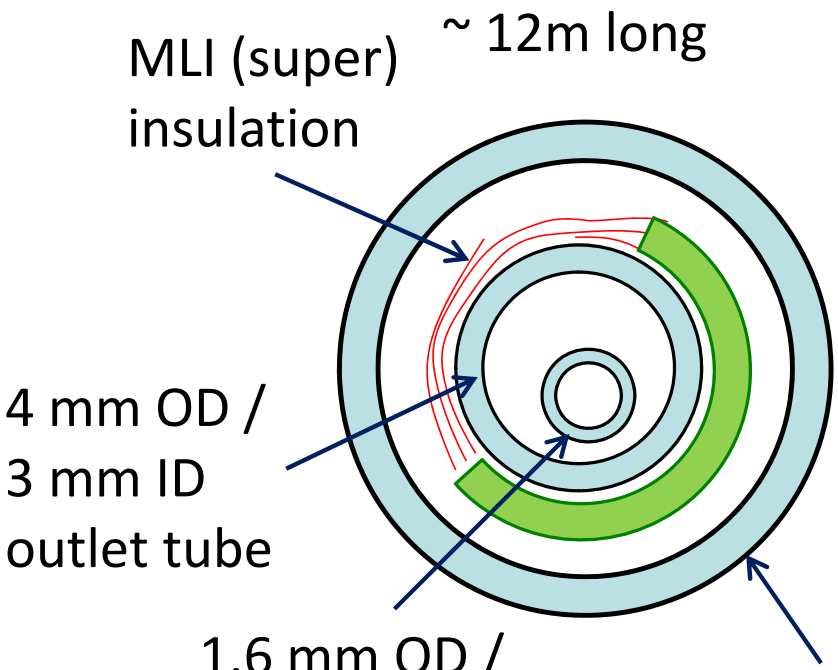
CO2 Plant „IBBelle“
(IBL + Belle)

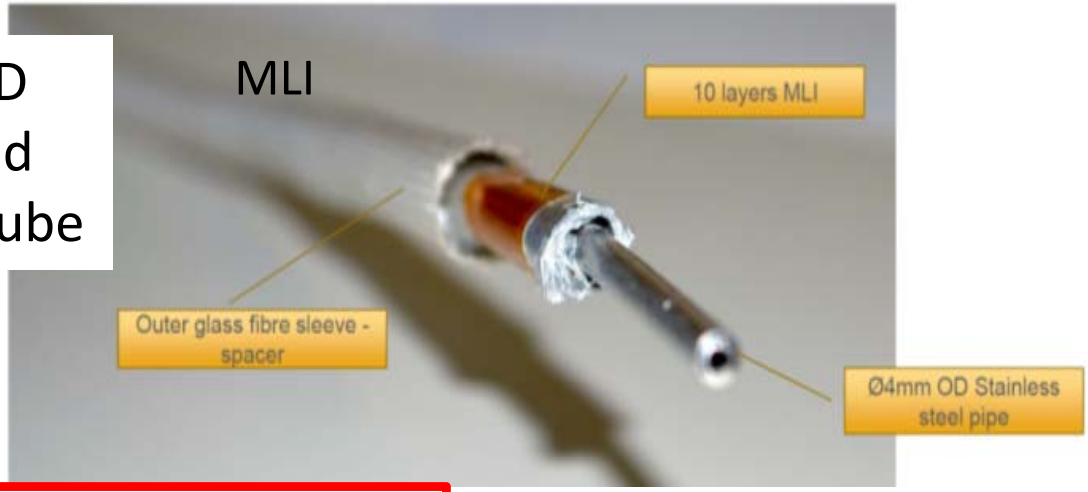
Services for IBBelle

- European standard P/S at KEK, needs to be reactivated
  Requirement: 400 [V] ± 10 % (filtering of V spikes)
- Water for the chiller cooling: 20 l/min, room temp OK,
  only filter needed, connections to be specified
- N2: 50 l/min (Gas), room temp OK
- Air conditioning: room temp ± 3°C, rel. humidity < 70 %
- Transfer lines & connection standards still need to be specified
  (depending on location of IBBelle)

CO2 Vacuum Flex Lines

Flex line design (by CERN/NIKHEF)

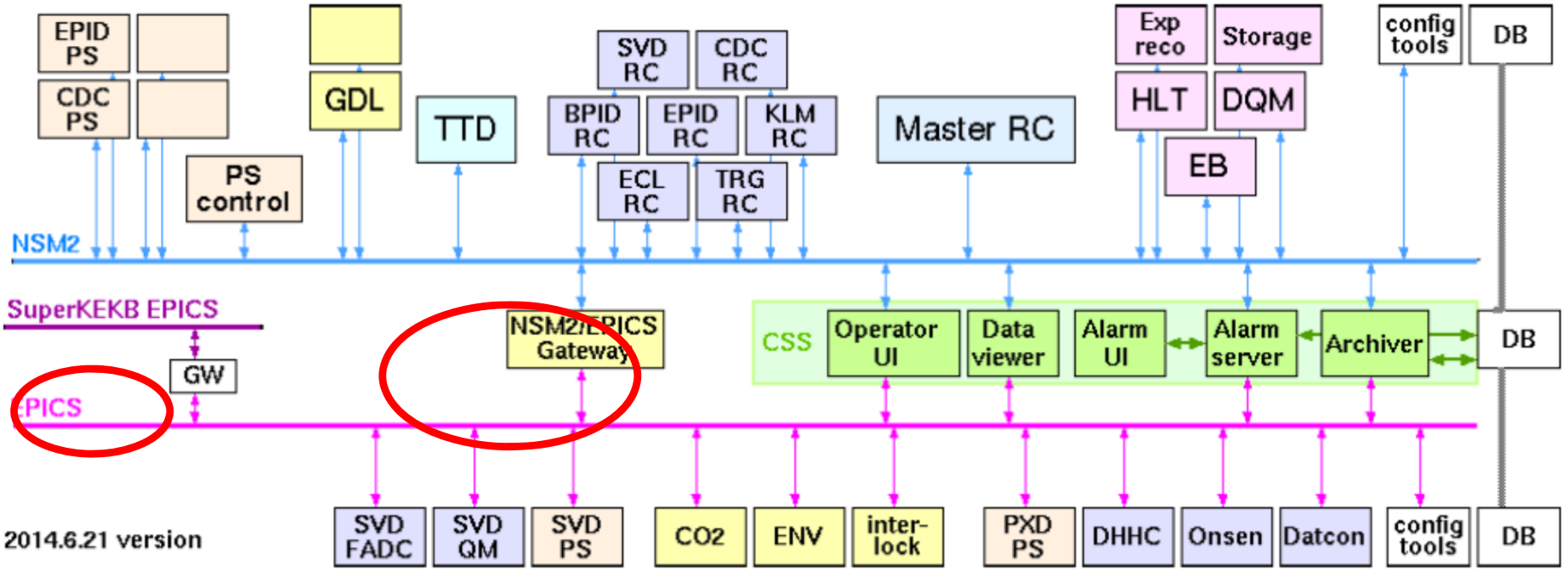




admissible bending radius:
~ 50 mm

CERN crew offers help building the tubes

Slow Control, Data Quality



Common GUI for Belle II: CSS, NSM2 (Run Ctrl) and EPICS (Slow Contr.)

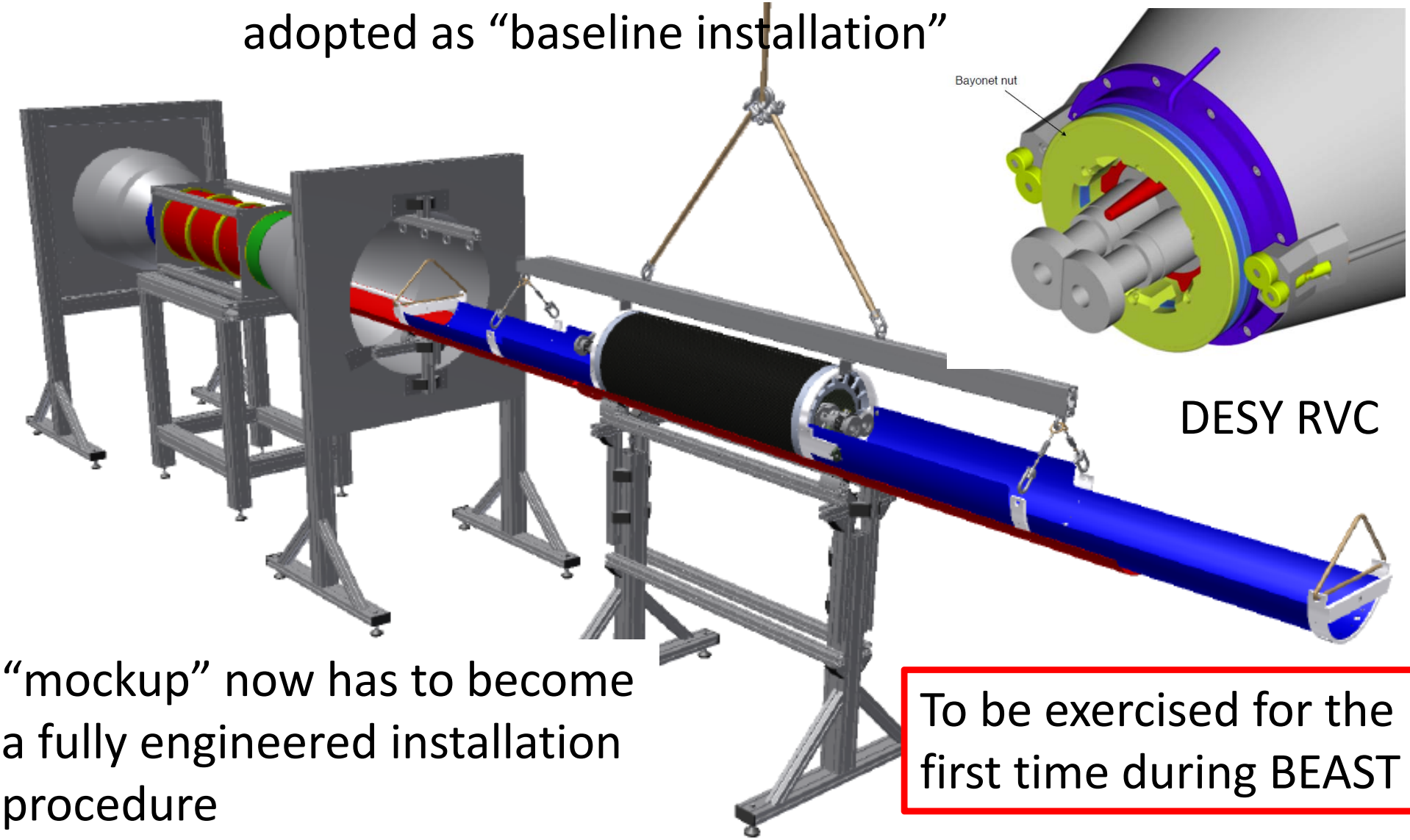
Michael Ritzert & Thorsten Röder @ KEK (September 2014):

Major Milestones achieved:

- Gateway between NSM2 and EPICS
- Present NSM2 data within CSS
- Strong support by Mainz group

VXD Installation: AIM

At KEK: Demonstrated AIM ("Alternative Installation Method")
including EDI "emergency de-installation",
adopted as "baseline installation"



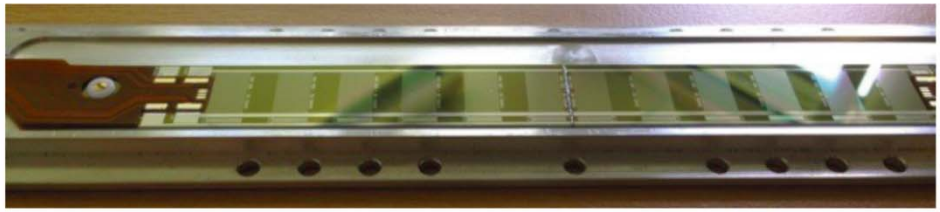
DESY RVC

"mockup" now has to become a fully engineered installation procedure

To be exercised for the first time during BEAST 2

VXD Thermal Mockup

Produced at
MPI / HLL



Thermal dummy sensors

Tscharlie
Ackermann
MPI

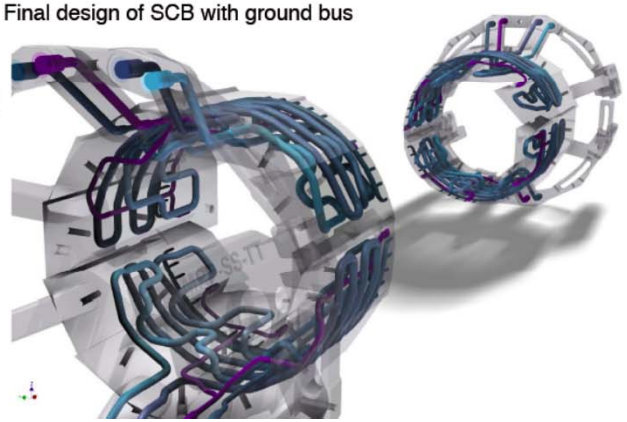
Full dummies produced,
now under measurement to
study gluing process

Kapton heating

Kapton flex

Support

Final design of SCB with ground bus



Production had some
delay, now preparing for
pressure tests at MPI

BEAST Phase 2: The "VXDP2"

- Phase 2:
  - Belle II on beamline, fully installed **except VXD**
  - Final Focus System (QCS) installed for the first time.
  - Final beampipe and HM masks around IP
  - First attempt to collide beams and achieve $1x10^{34}$ /cm s

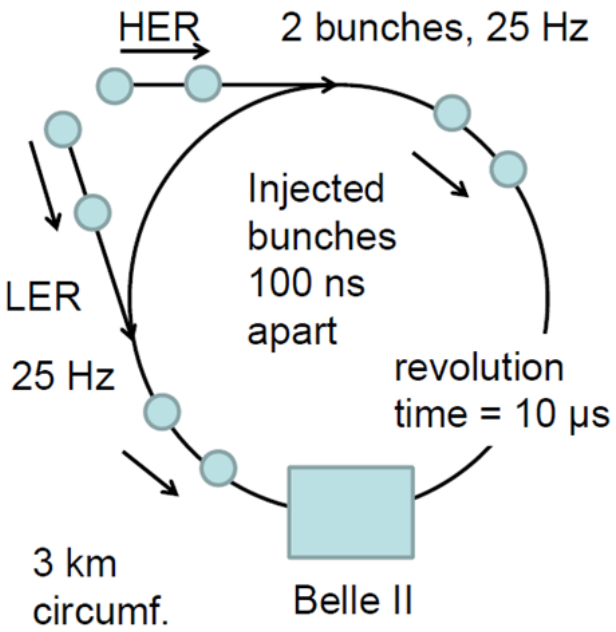
- Determine particle/photon fluxes for the individual background contributions (syn.rad., Touschek, rad. Bhabha, 2γ)

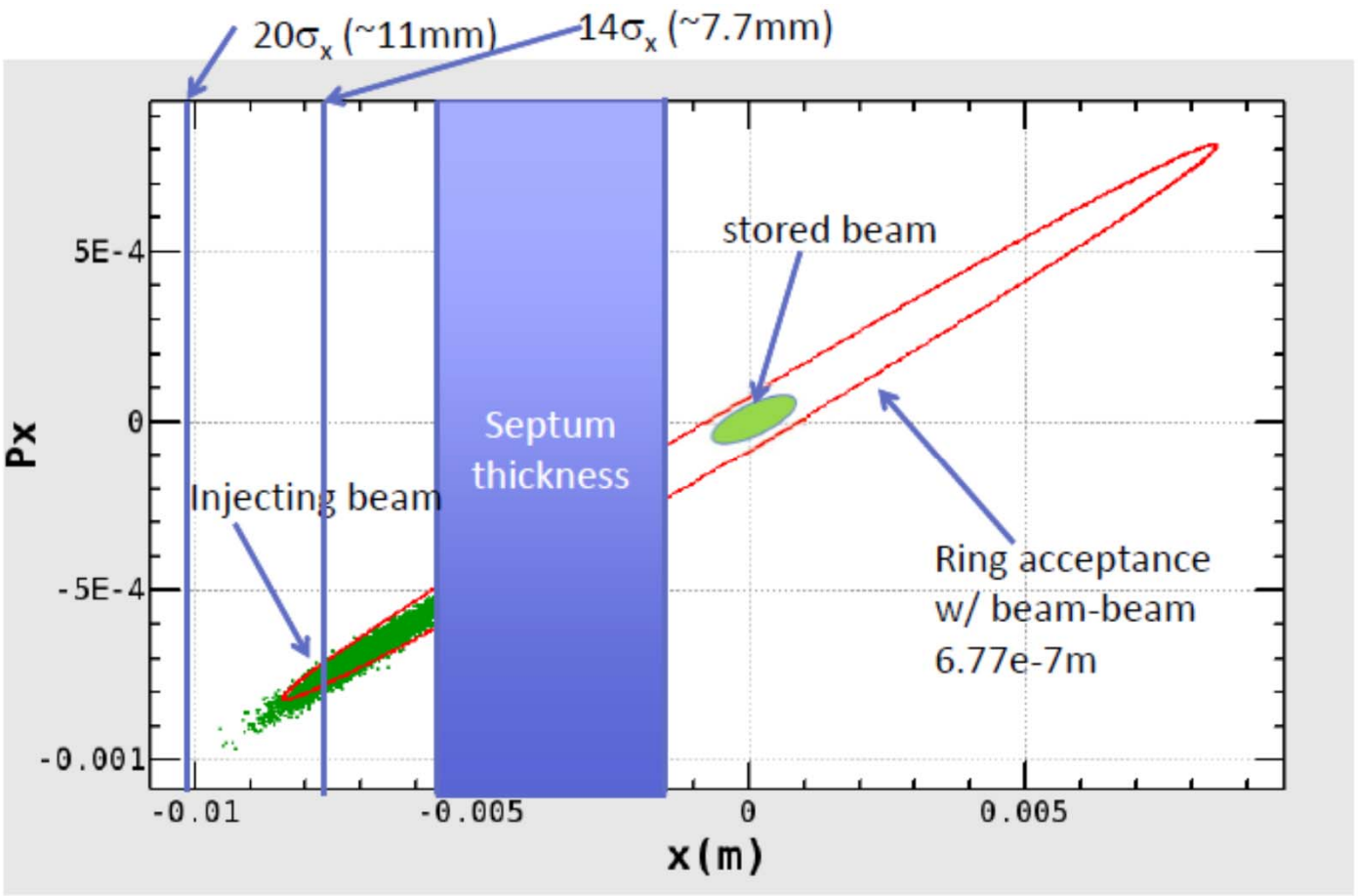
- Study injection bg and exercise gated mode operation of VXD

- Determine bg status safe for PXD/SVD, exercise H/W interlock, radiation & environmental monitoring (!)

- "Background": particle fluxes and energy spectra, correlation with rest of Belle II (full DAQ and Slow Control)

Injection “Noise”





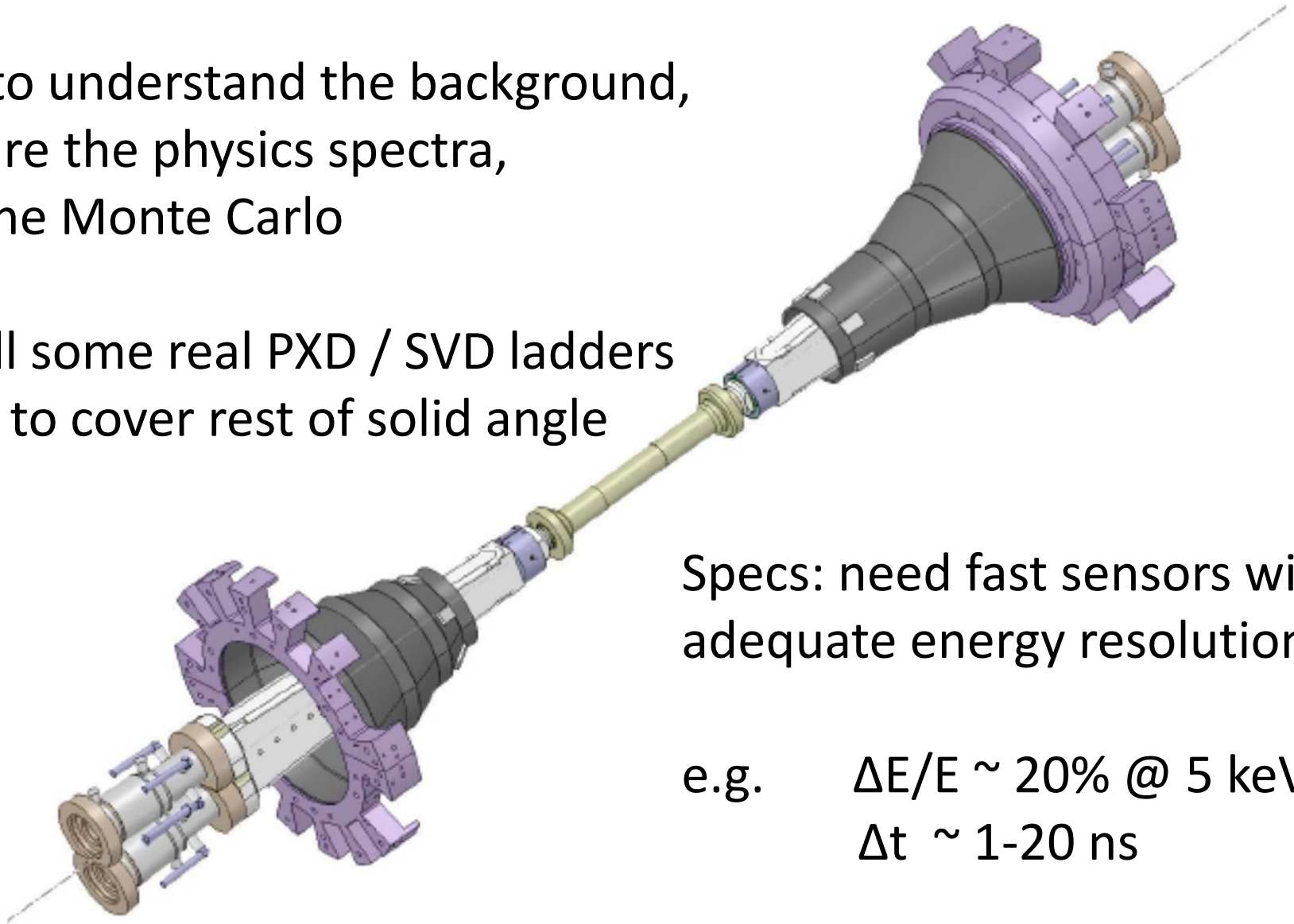
“Continuous” injection with 50 Hz keeps machine current constant (ΔI/I very small)

Injected bunch: coherent betatron oscillations with large amplitudes -> particle loss
-> “noisy bunches”
oscillations damped by special feedback system
KEKB: damping time ~ 4 ms

VXDP2 Specification

Need to understand the background,
measure the physics spectra,
train the Monte Carlo

- Install some real PXD / SVD ladders
- need to cover rest of solid angle



Specs: need fast sensors with adequate energy resolution

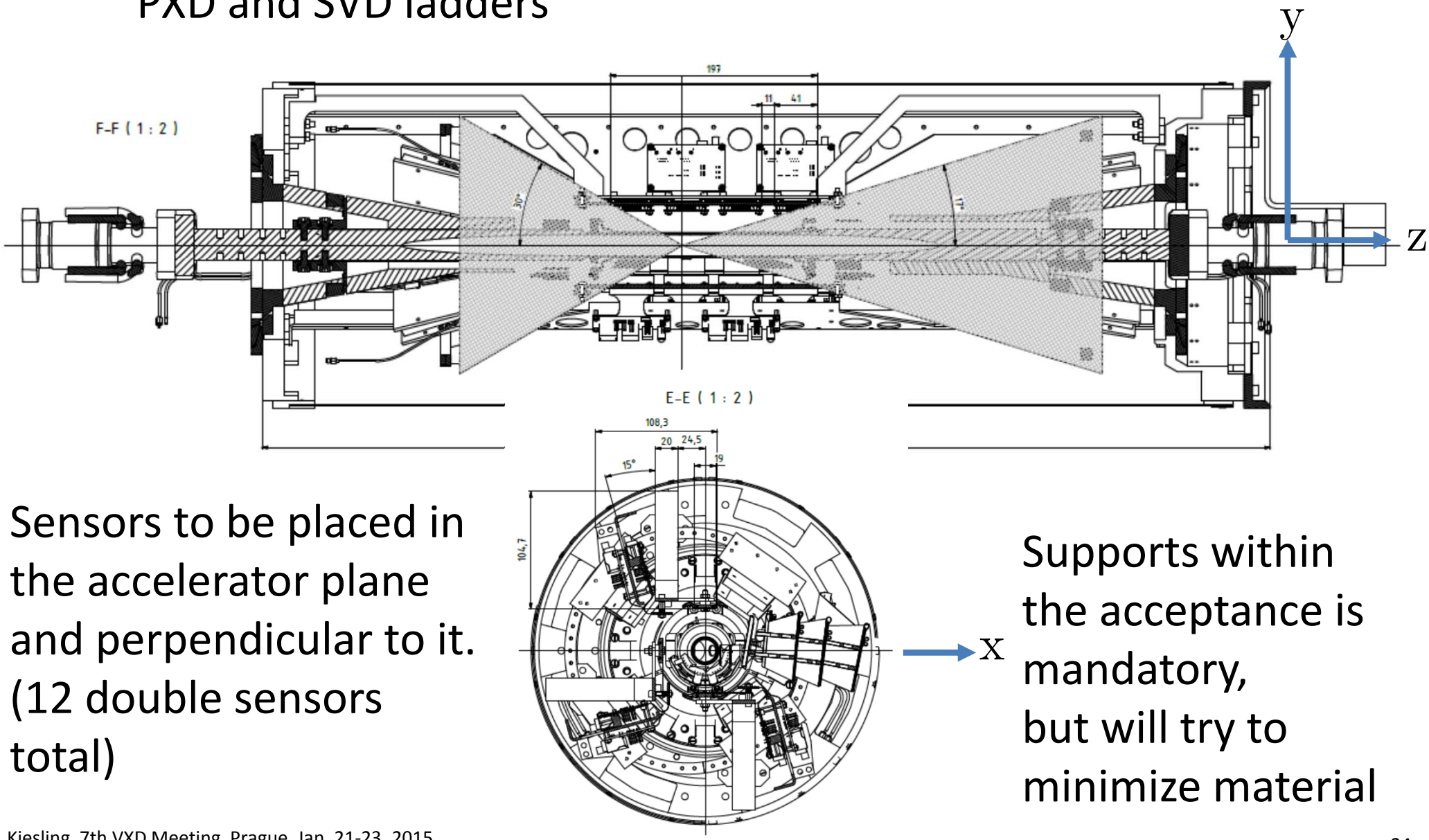
e.g. $\Delta E/E \sim 20\%$ @ 5 keV
$\Delta t \sim$ 1-20 ns

Strasbourg group wants to contribute (discussion)

NTU group wants to measure Bhabhas: install BGO crystals

VXD Equipment during Phase 2

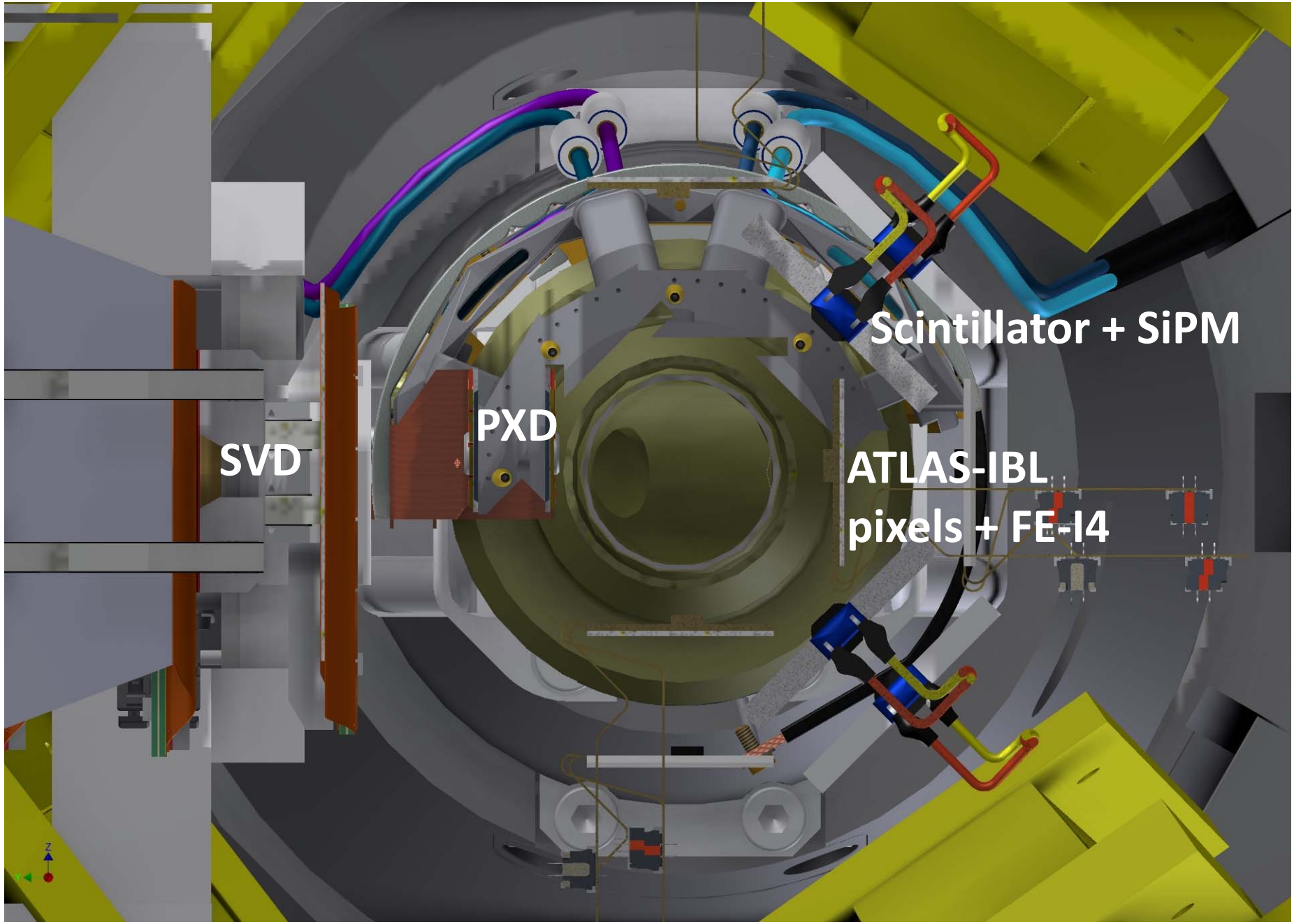
Plan: Cover large part of the area not instrumented by PXD and SVD ladders



Sensors to be placed in the accelerator plane and perpendicular to it. (12 double sensors total)

Supports within the acceptance is mandatory, but will try to minimize material

VXD Equipment during Phase 2



VXD Clean Room in B1

Should already be available
for BEAST Phase 2 assembly

Tscharlie Ackermann

Conclusion & Outlook

- DEPFET PXD9 Phase I production finished, 30 wafers, 180 matrices
- EMCM metallization program completed successfully
- Pilot Run with 3 “hot” wafers (10 %) + 5 “EMCM”-type wafers ongoing
- Present generation of ASICs suited for Gated Mode testing with PXD9, final submission by end of June 2015 (date somewhat critical)
- Switcher bumping to be defined, SMD procedure not yet established
- Identified Issue: mass testing of ASICs (especially DCDpl and SWG)
- DESY Thermal Test 2015 progressing, ladders built, SCBs in process
- Concrete planning for BEAST Phase 2 (“VXDP2”) has started, contributing groups are identified

Backup

Program for Spare / Upgraded PXD

- Construct spare PXD by the summer of 2019 (~ 5 years from now)
  Plan supported by Belle II management

- Need 2 years of production of sensors + < 2.5 years for construction, optional development of new ASICs, and commissioning

  -> continue production of new sensors when the present production is finished (sensors will be paid by MPI)

  -> Funding for electronics requested from BMBF for 2015-18

- Development of ASICs (+DAQ H/W) should wait for significant experience in beam operation (start development in 2017)

Pilot Assembly

- Start a pilot run with PXD9 3 wafers + 5 wafers “EMCM”-type (final metallization + thinning)

- Equip sensors with present ASICs (Gates Mode should work)

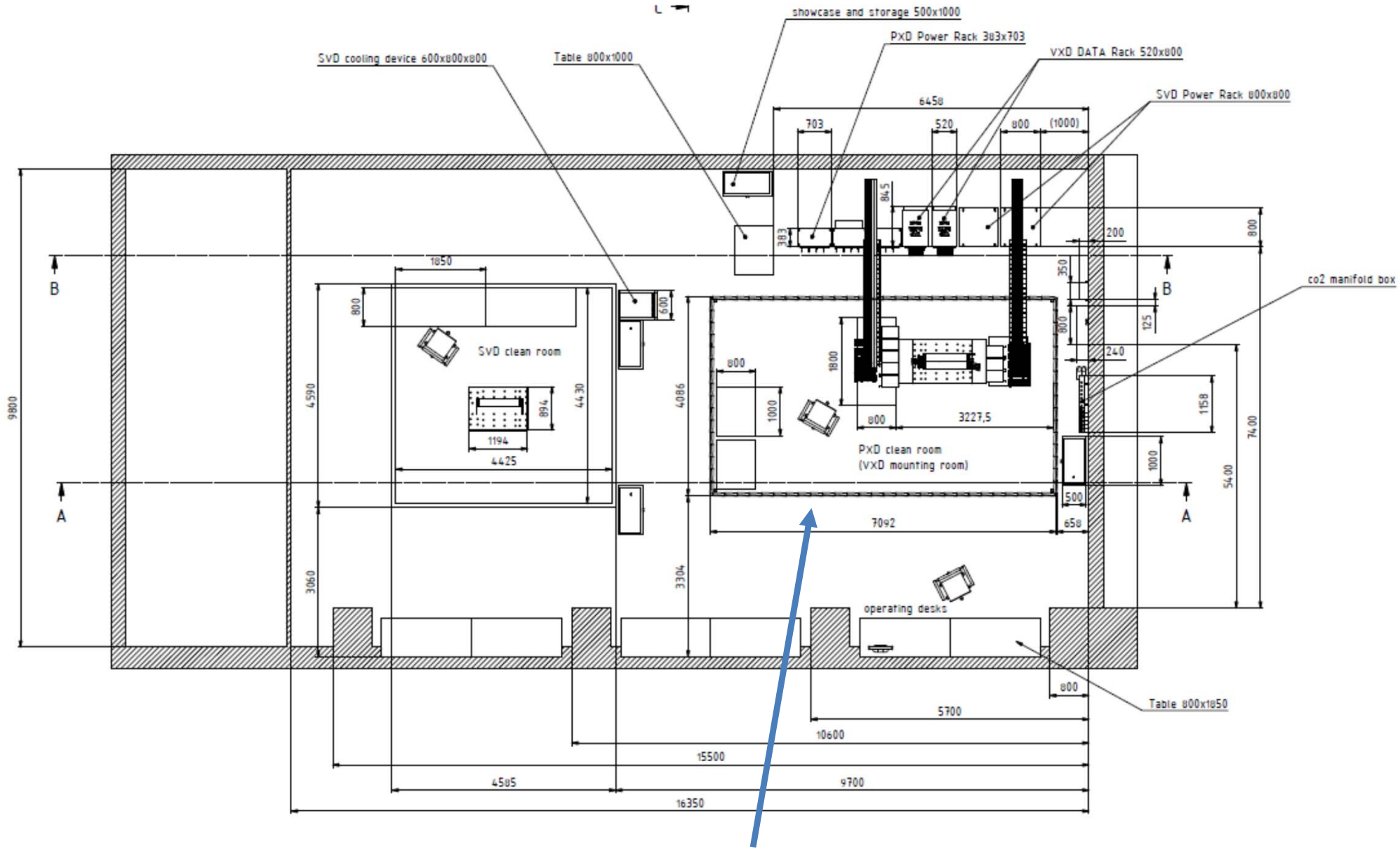
- Submit “final” Kapton design in Jan. 15 (back by March 2015)

- Do thorough tests with full modules assembly (+ gated mode) (flip chip @IZM Germany, SMD @ NTC Valencia

- Submit final ASICs by end of June 2015

- Prepare beam test (at DESY) with 2 sensors (ladders) together with final SVD ladders for the fall of 2015
(BEAST Phase 2 will have final ladders)

Phase 2 / PXD Integration



VXD Assembly clean room in B1