FADC Hardware + Firmware Status,
Noise Measurements

Richard Thalmeier (HEPHY Vienna)
• SVD Readout Hardware + Firmware Status: Progress since Pisa meeting / October 2014
SVD Readout System Overview

- DAQ: PC Farm
- COPPER: common readout platform
- FADC system with optical link to COPPER
- DOCK box with DC/DC
- Front-End

Data

Richard Thalmeier: FADC Hardware + Firmware Status
### SVD Readout System Overview

- **Main milestone**: CERN beam test in November 2014.
- **Goal from FADC development view**: Get as much components of the 2nd hardware iteration running stable, and learn what can be improved.
Junction Board V2 / DOCK Box

Richard Thalmeier: FADC Hardware + Firmware Status 2015-01-22
Junction Board V2 / DOCK Box

October 2014: Ready for beam test.
Junction Board V2 / DOCK Box

October 2014: Ready for beam test.

Now: Further tested, used at the beam test, still works fine.
FADC Mainboards V2

- ONSEN
- DATCON
- Copper Finesse
- Copper Finesse
- FTB
- Hybrid
- Hybrid
- FADC
- Junction Board
- HV + LV Power
- Buffer
- FADC Controller
- FADC
- FTB
- FTB

3 more FADC crates

PXD regime

SVD regime

Control_PC

DAQ regime

Richard Thalmeier: FADC Hardware + Firmware Status  2015-01-22
FADC Mainboards V2

- **October 2014:** PCBs ready, not equipped, not tested, Firmware not adapted yet.
FADC Mainboards V2

- **October 2014:** PCBs ready, not equipped, not tested, Firmware not adapted yet.
- **Now:** Equipped, programmed and tested successfully (including November beam test at CERN). Still missing in the firmware: Gigabit, Stratix-EEPROM-Flashing-via-VME, Hit-Time-Finding.
FADC Mainboards V2

- **October 2014:** PCBs ready, not equipped, not tested, Firmware not adapted yet.
- **Now:** Equipped, programmed and tested successfully (including November beam test at CERN). Still missing in the firmware: Gigabit, Stratix-EEPROM-Flash- via-VME, Hit-Time-Finding.

We had some **stability problems with VME access** at CERN beam test. I did lots of tests with my own VME test programs afterwards, and it seems to be **rock solid**. Probably Software or CAEN-VME-driver-problem: there was a program running on the DAQ-PC which read out some flags via VME from the FADC controller for the first time, in parallel to Hao's software, which did blockreads from the FADCs at the same time. In the final software this all will be done serially by the software, so the problem **should vanish anyway**. But of course this has to be investigated further.
FADC Stratix IV Daughterboards V2

Richard Thalmeier: FADC Hardware + Firmware Status
FADC Stratix IV Daughterboards V2

- **October 2014:** PCB development is in progress. FPGAs will be delivered in January 2015.
FADC Stratix IV Daughterboards V2

- **October 2014:** PCB development is in progress. FPGAs will be delivered in January 2015.

- **Now:** PCBs are ready and waiting to be equipped. FPGA delivery has been delayed by one month to mid-Feb.
Buffer Board

ONSEN

DATCON

PXD regime

SVD regime

Control_PC

3 more FADC crates

HV + LV Power

FTB

FADC Controller Buffer

Backplane Bus

Junction Board

FADC_

Copper Finesse

Copper Finesse

SVD regime

PXD regime

DAQ

Control_PC

SVD

Richard Thalmeier: FADC Hardware + Firmware Status

2015-01-22
Buffer Board

- **October 2014**: Tested and OK.
Buffer Board

- **October 2014:** Tested and OK. (That is what we thought back then...)
- **Now:** Further testing revealed that the source of some problems present since its existence (e.g. occasional data transmission problems between Cyclone and Stratix FPGA) was the Buffer Board. **Clock problems in the VME cards** were heavily dependent on their position in the VME crate. These problems now **have been finally solved** by optimizing the pre-emphasis of the buffer chips on the Buffer Board. Extensively tested then (e.g. at CERN beam test). So... Tested and OK (again) 😊.
FADC-Controller V2

- **ONSEN**
- **DATCON**

**PXD regime**

**SVD regime**

- **DATCON**
- **Control_PC**

- **HV + LV Power**
- **FADC Controller**
- **Buffer**
- **FTB**
- **Junction Board**

- **Copper Finesse**

- **3 more FADC crates**

- **Backplane Bus**

- **DAQ**
- **DOCK Box**
- **VME Crate**

*(Picture shows V1)*
FADC-Controller V2

- **October 2014**: PCBs are ready, not equipped, not tested, Firmware not adapted.
FADC-Controller V2

- **October 2014:** PCBs are ready, not equipped, not tested, Firmware not adapted.
- **Now:** PCB is equipped, firmware has been adapted by myself (mainly FPGA pinout changes; LED outputs added, FPGA-Self-Bootup), not fully tested yet.

At the CERN beam test we had V2 ready, but used V1. V2 was supposed to be tested also if we had some time left, but then was abused as organ donor (clock generator electronics) for V1...

Next week Katsuro will continue developing his FADC-Controller-Firmware at HEPHY; e.g. there are some trigger issues to be fixed.
HV and LV Power Supplies

FADC Controller
Buffer
FADC
Junction Board
HV + LV Power
FTB
Copper Finesse
Copper Finesse
FTB
3 more FADC crates
FADC VME Crate
DOCK Box
Copper VME Crate
DAQ

ONSEN
DATCON

PXD regime
SVD regime
Control_PC

Richard Thalmeier: FADC Hardware + Firmware Status
HV and LV Power Supplies

Detector

R.AC is finite only for pinholes

Sensor

Wire on Hybrid

Main ground, on detector

Hybrid connector

1.25_N

+1.25_HV_N

+2.50_HV_N

N_SIDE_HYBRID

APV25

GND_HV_N

HV_N_BIAS

HV_N_RET

HV_P_RET

HV_P_BIAS

+1.25_HV_P

+2.50_HV_P

P_SIDE_HYBRID

APV25

GND_HV_P

Power Supplies

10 V

LVPS_N

20 - 100 V

HV_N

NO GND connection here

20 - 100 V

HV_P

Extra separation voltage

on P SIDE

10 V

LVPS_P

No separation voltage

on N SIDE
HV and LV Power Supplies

- **October 2014:** Migration from Kenwood to CAEN was ongoing.
HV and LV Power Supplies

- **October 2014:** Migration from Kenwood to CAEN was ongoing.
- **Now:** At the CERN beam test we had *excessive noise problems* with the CAEN, so we switched back to the Kenwood, which worked fine. Will have to be investigated further.
Component Testing System

560 Analog Daughterboards

560 Digital Daughterboards

70 Stratix Daughterboards
Component Testing System

- **October 2014**: Testing process and first schematics were in development.
Component Testing System

- **October 2014**: Testing process and first schematics were in development.
- **Now**: Schematics and PCB layouts are ready; last verifications are done right now before ordering the PCBs.
SVD Readout Hardware V2 Prototypes + Firmware Status - Conclusion

- **Junction Boards**: Ready.
- **FADCs + analog and digital daughterboards**: Mostly ready, but still needs a lot of work.
- **Stratix-Daughterboards**: Waiting for the FPGAs.
- **Bufferboard**: Ready.
- **FADC Controller**: Mostly ready.
- **Component testing systems**: Hardware has been developed but not built yet; no firmware or software yet. Much work left.
- **HV and LV Supplies**: CAEN has to be debugged.
• DESY Noise Problem
DESY Noise Problems – Symptoms

- At the DESY beam test we installed and tested our setup; no PXD was present at first. We did **not** observe any noise problems at the output of the L3 sensor.
DESY Noise Problems - Symptoms

- The PXD was installed then and connected to its power supplies etc => since then the SVD software showed severe noise problems at L3.

Noise Map

- without PXD
- with PXD
DESY Noise Problems – Symptoms

- I tried to examine the source of the problems ghostbuster-style with an oscilloscope with a quickly-self-wounded coil connected to an active probe => there was a strong sine wave shaped disturbance of some fixed frequency all around the magnet. (Sorry, no one including myself seems to have noted or remember the frequency; but I have something around 1.5MHz in my mind..., which corresponds to a wavelength in the range of kilometers).

- With just two independent wires connected to the probe I did not observe this disturbance. So it must have been of electromagnetic nature, and not of electrostatic kind.
DESY Noise Problems – Symptoms

- The **PXD** then was disconnected from its external electronics and power supplies => the problems in the SVD data were still about the same. So the source of the problem cannot have been the PXD supplies, and also not the electronics on the PXD itself.
DESY Noise Problems – Symptoms

- Also the PXD group observed severe noise problems; mostly when the SVD was turned on...
DESY Noise Problems – Symptoms

- The PXD people tried lots of things: **Ground the PXD** directly to the magnet case, implement **cable shieldings** with aluminium foil connected to different points, etc... – some of them made it worse for them, some of them made it better. Unfortunately no one at the PXD and SVD side seems to have recorded the different activities and its impacts (**we have to in the future!!**); both sides tried lots of things not always coordinated and systematically, until both sides somehow had reasonably sufficient working systems...
DESY Noise Problems - Symptoms

- For the SVD, it was not easily possible to ground directly at the APVs, because that would have required the disassembly of the whole setup including the CO2 cooling system, so we did the best we could have been done from the outside: ground the SVD at the Dock box to the housing of the magnet using several wires. This diminished the problem: the noise was still present, but it was so low now that the SVD data at least was usable.
DESY Noise Problems – Educated Guess

- The wire bunches to the two sensor systems always are (more or less weakly) **capacitively coupled** to each other, to ground, or to something else. Not with 0 ohms, of course, but still – very simplified – with some (more or less high) impedance. (In reality it is some kind of distributed RLC network).
DESY Noise Problems – Educated Guess

- So for MHz frequencies they can be considered somewhat connected.
DESY Noise Problems – Educated Guess

- So for MHz frequencies they can be considered somewhat **connected**.
  Thus we have a **wire loop**.
DESY Noise Problems – Educated Guess

- We for sure had lots of electric and electronic devices in the area which could emit **magnetic fields** – and there must have been such, because I **did** measure an AC voltage at the coil connected to the oscilloscope probe.
DESY Noise Problems – Educated Guess

- We for sure had lots of electric and electronic devices in the area which could emit **magnetic fields** – and there must have been such, because I **did** measure an AC voltage at the coil connected to the oscilloscope probe.

So with the wire loop and the alternating magnetic field there is an alternating **voltage** between the PXD and the L3 Sensor induced.
DESY Noise Problems – Educated Guess

- If the PXD gets **grounded** to the magnet housing, the whole loop is still present; only the electrical potentials are shifted. So the SVD still has the same alternating voltage in respect to the PXD, because the SVD oscillates around ground with the full alternating voltage. The PXD now does not.
DESY Noise Problems – Educated Guess

- If the loop is **grounded additionally** at another point (e.g. at the PXD Supplies) connected outside the magnetic field to the grounded magnet housing, ...

![Diagram showing FADC, Power, DockBox, L3 Sensor, and connections]

```text
DESY Noise Problems – Educated Guess

- If the loop is **grounded additionally** at another point (e.g. at the PXD Supplies) connected outside the magnetic field to the grounded magnet housing, ...
```
DESY Noise Problems – Educated Guess

- If the loop is **grounded additionally** at another point (e.g. at the PXD Supplies) connected outside the magnetic field to the grounded magnet housing, the voltage at the PXD cables (induced by the magnetic field which gets around these cables) then **gets shorted** and lost in the impedance of this cable and the ground return (like a short circuited transformer). But the voltage on the SVD cables (induced by the field around the SVD cables) remains. So the total voltage between the sensors is less. For now.
DESY Noise Problems – Educated Guess

- Now lets ground the **SVD Dock box and the PXD**, as we also did at DESY.
DESY Noise Problems – Educated Guess

- Now let's ground the **SVD Dock box and the PXD**. The loop gets a **lot smaller**, and so the area, and so the $\Phi = \int B \times dA$. That's why we observed **much smaller noise** in the SVD then.
DESY Noise Problems – Educated Guess

- Now lets ground the **SVD Dock box and the PXD**. The loop gets a **lot smaller**, and so the area, and so the $\Phi= \int B \ast dA$. That’s why we observed **much smaller noise** in the SVD then. The impedance of the original loop is much, much higher, and so the voltage division of this loop into the new grounding wire is negligible; practically all its voltage drops at $Z$. 

**Diagram**

- FADC, Power
- Z
- DockBox
- PXD
- L3 Sensor
- $d\Phi/dt$
- $U$
DESY Noise Problems – Educated Guess

- So... if we would have grounded the L3 directly inside the magnet housing without including the 2m wires outside the magnet housing to the Dock box into our current loop, the problem **should have virtually disappeared.**
DESY Noise Problems – Educated Guess

- So... if we would have grounded the L3 directly inside the magnet housing without including the 2m wires outside the magnet housing to the Dock box into our current loop, the problem *should have virtually disappeared*.

**Groundings** or connections on any other **additional point(s)** now are **bad** because then we have a low impedance voltage divider of the voltage generated in the big loop between the impedance of the grounding lines and those of the external cabling. This causes to rise the voltage between PXD and L3 again.
DESY Noise Problems – Investigation

- Based on these educated guess, so if such a loop really was the cause of the noise, it should be possible to reproduce the DESY-noise by applying some material close to the L3-sensor which has alternating voltage respect to the sensor.

- If such a loop with a voltage between the PXD and SVD was not the cause, it should be unlikely that such an investigation brings comparable results.

So Hao and myself built and examined some electrical mockup last week.

We intended to build a setup which causes SVD noise behavior as close as possible to those at the DESY beam test.

The plan was to inject some noise (different shapes, amplitudes, ...) in different ways (capacitive, inductive, combinations of them) with different injectors into the L3, until the software shows similar noise behavior as at the DESY beam test, to conclude what can have caused the problems.
DESY Noise Problems – Investigation

- The very first attempt was: A simple metal sheet, insulated by a sheet of paper, connected to a frequency generator, and placed near the L3. Frequency: 1.5 MHz, amplitude 20 Volts.
DESY Noise Problems – Investigation

- Result: Noise behavior similar to DESY, but much worse.
- So we just lowered the amplitude to 5 volts – and we had very similar noise compared to the DESY beam test situation!
DESY Noise Problems – Conclusion

- So the **assumption** that the DESY SVD noise problem was **caused by bad grounding of the SVD**, and that a proper grounding of the SVD (as it has already been implemented since then) close to the sensor will **eliminate the problem**, seems **very plausible**. This assumption has been **hardened by our investigations**.
The End...

... for now.

A lot is done, but there is still a lot to do... fine! 😊
<table>
<thead>
<tr>
<th>MAXWELL</th>
<th>Global / Integral (ohne K, B)</th>
<th>Lokal / Sprung</th>
<th>Bewegt</th>
<th>Einheiten</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ind.-Gesetz innen orient</td>
<td>( U(\omega A) = -\hat{\Phi}(A) )</td>
<td>( \nabla \times \vec{E} = -\partial_t \vec{B} )</td>
<td>( \nabla \cdot \vec{B} = 0 )</td>
<td>([U] = V)</td>
</tr>
<tr>
<td>Magn. Hüll-Fluss innen orient</td>
<td>( \Phi(\omega \vec{V}) = 0 )</td>
<td>( \nabla \cdot \vec{B} = 0 )</td>
<td>( \nabla \times \vec{A} = 0 )</td>
<td>([E] = V/m)</td>
</tr>
<tr>
<td>Durchfl. AMS außen orient</td>
<td>( \vec{V}(\omega \vec{A}) = \vec{I}(A) + \vec{\psi}(A) )</td>
<td>( \nabla \times \vec{H} = \vec{J} + \partial_t \vec{D} )</td>
<td>( \nabla \cdot \vec{B} = 0 )</td>
<td>([\psi] = \text{V} \cdot \text{s})</td>
</tr>
<tr>
<td>Erhalt.-El.-lad. außen orient</td>
<td>( \psi(\omega \vec{V}) = \vec{Q}(\vec{V}) )</td>
<td>( \nabla \cdot \vec{D} = \sigma )</td>
<td>( \nabla \cdot \vec{B} = 0 )</td>
<td>([\vec{D}] = \frac{\text{V} \cdot \text{s}}{\text{m}^2})</td>
</tr>
<tr>
<td>Erhalt.-El.-lad. außen orient</td>
<td>( \vec{I}(\omega \vec{V}) = -\vec{\alpha}(\vec{V}) )</td>
<td>( \nabla \cdot \vec{J} = -\partial_t \sigma )</td>
<td>( \nabla \times \vec{A} = 0 )</td>
<td>([\vec{J}] = \frac{\text{A}}{\text{m}^2})</td>
</tr>
</tbody>
</table>

**Einheiten:**
- \([U] = V\)
- \([E] = V/m\)
- \([\psi] = \text{V} \cdot \text{s}\)
- \([\Phi] = \frac{\text{V} \cdot \text{s}}{\text{m}^2}\)
- \([\vec{D}] = \frac{\text{V} \cdot \text{s}}{\text{m}^2}\)
- \([J] = \frac{\text{A}}{\text{m}^2}\)
- \([K] = \frac{\text{A}}{\text{m}}\)
- \([\sigma] = \frac{\text{A} \cdot \text{s}}{\text{cm}^2}\)
- \([\vec{E}] = \frac{\text{V} \cdot \text{s}}{\text{m}^2}\)
- \([\vec{B}] = \frac{\text{V} \cdot \text{s}}{\text{m}^2}\)
- \([\vec{D}] = \frac{\text{V} \cdot \text{s}}{\text{m}^2}\)
- \([\vec{H}] = \frac{\text{V} \cdot \text{s}}{\text{m}^2}\)
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**Fiktiv:**
- \( E = F + W \)
- \( \vec{A} = \partial_t \vec{E} + \nabla \times \vec{B} \)
- \( \vec{B} = \vec{H} \times \vec{M} \)
- \( \vec{F} = -\nabla \cdot \vec{E} \)
- \( \vec{D} = -\nabla \cdot \vec{B} \)

**Bewegt:**
- \( E' = E + \partial_t \vec{E} \)
- \( B' = B \)
- \( \vec{M}' = \vec{H} \times \vec{M} \)
- \( \vec{F}' = \vec{E} \times \vec{B} \)