DEPFET IB-Meeting

Report of PL

- DEPFET Collaboration Matters
- Preparations of PXD9 sensors and ASICs
- Assembly Procedures
- Services, DAQ and Cooling
- Preparation for BEAST Phase 2

DEPFET Collaboration Matters

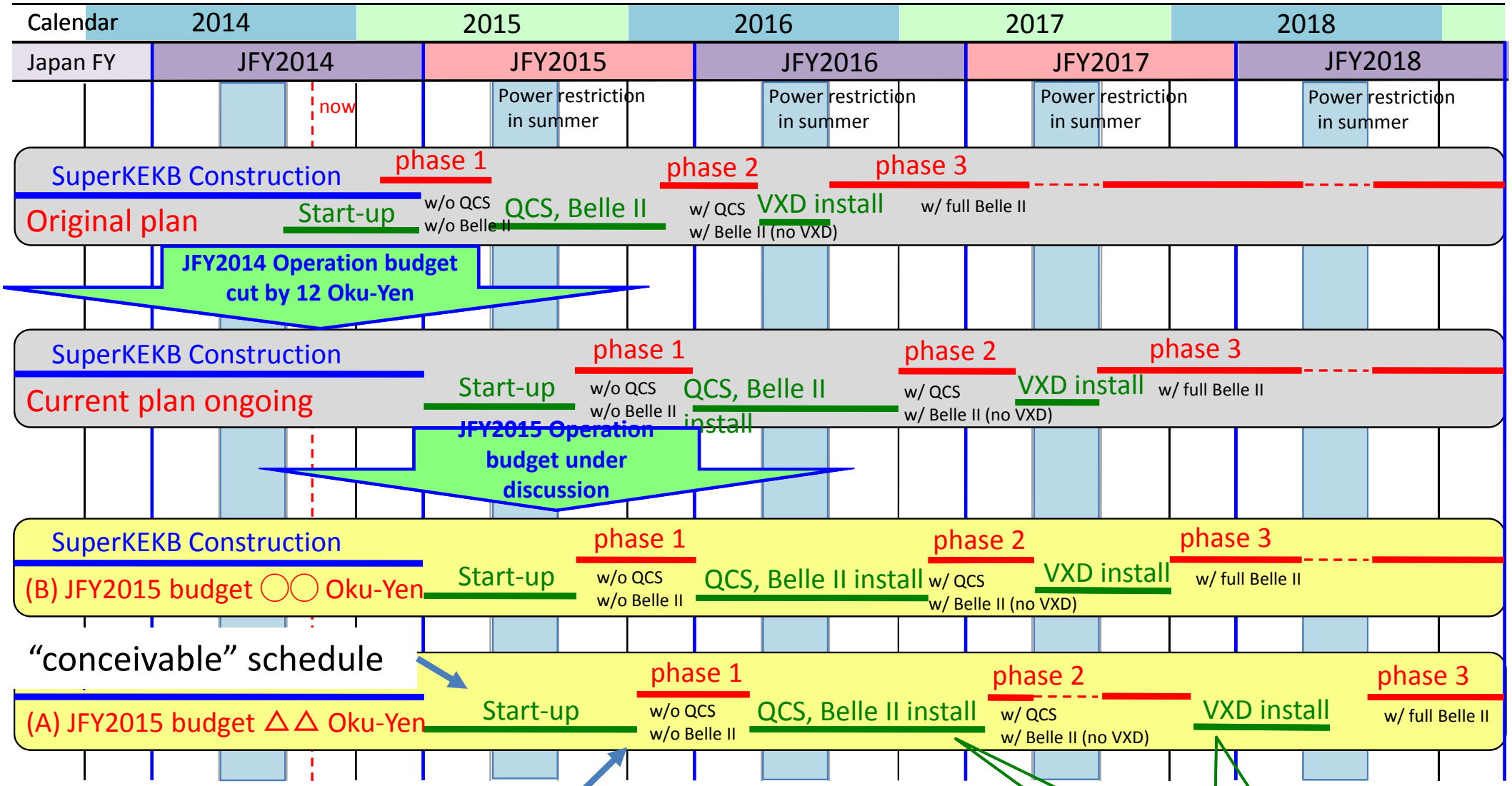
- Prof. Concettina Sfienti's group (University of Mainz, DEPFET has also joined Belle II during the last B2GM (Nov. 2014)
  - PXD Services: Slow Control
  - Presentation of plans during this meeting (M. Hoek)

- Prof. Ivan Peric left Heidelberg University, now at KIT (IPE)
  - will continue the ASIC development for the PXD (DCD, SWG)
  - (KIT is already member of DEPFET and Belle II Collaborations)

- Prof. Fischer's group (Heidelberg University) will stop ASIC development for the PXD, but
  - concentrate on Slow Control of the VXD and Belle II
  - (together with Mainz and TUM)

SuperKEKB/Belle II Schedule

shown during B2GM in Nov. 2014



“MEXT gives maximum consideration to SuperKEKB”
(“conceivable schedule” confirmed by M. Yamauchi)

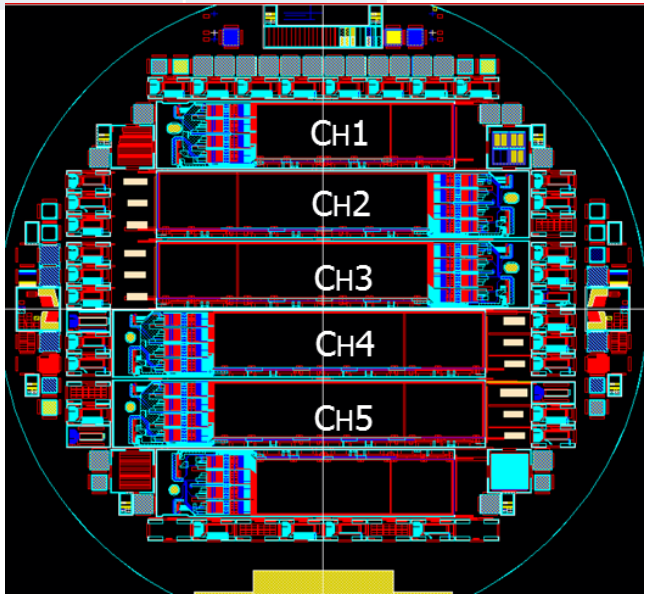
more discussions in Ushiroda-san's talk

Status of DEPFET Sensors (Phase I)

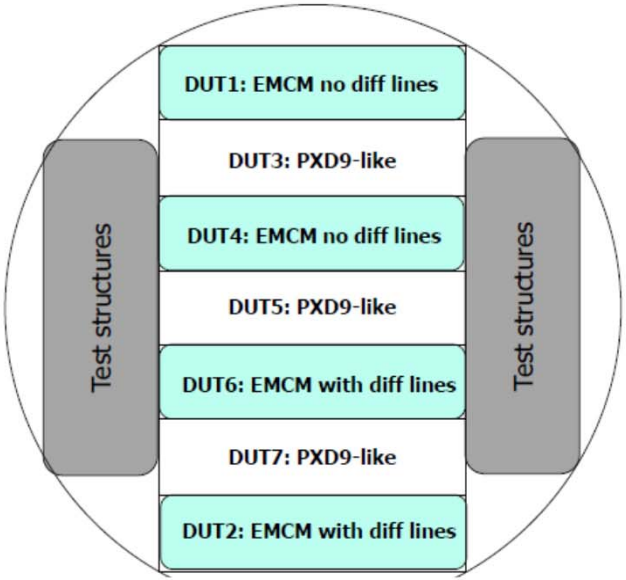
	0	1	2	3	4	5	sum
Chip1	10	9	2	2	1	6	30
Chip2	16	7	1	0	0	6	30
Chip3	16	4	3	2	0	5	30
Chip4	11	4	5	3	1	6	30
Chip5	12	4	4	2	2	6	30
Chip6	15	4	2	2	1	6	30

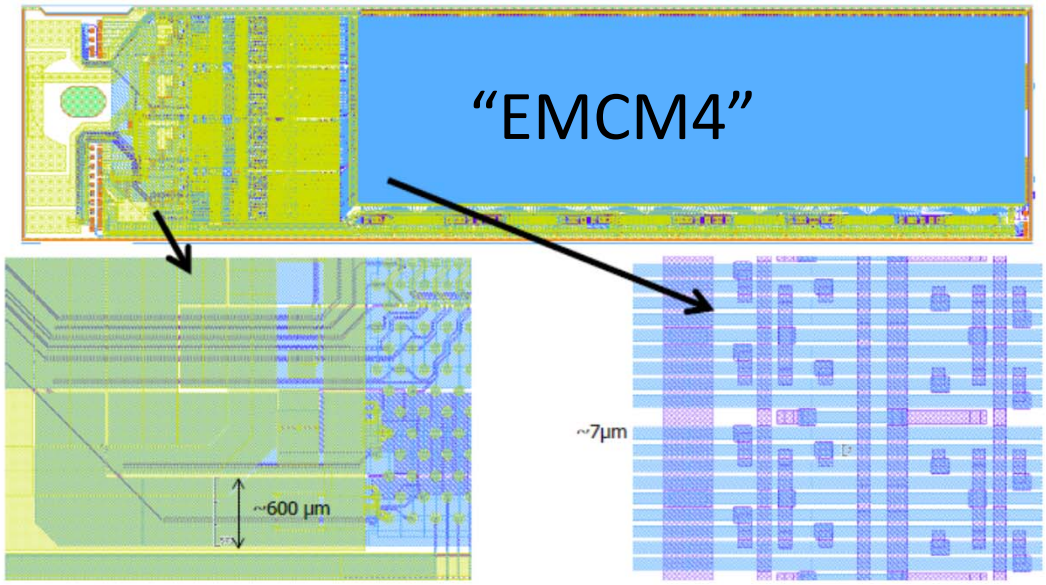
0 – no severe defects
1 – single pixel
2 –single rows and columns
3 – whole modul affected?
4 – whole module killed
5 –to be clarified

PXD9 wafer yield > 60 %



Status of Metallization (Phase II)





Wafer	DUT1	DUT2	DUT3	DUT4	DUT5	DUT6	DUT7
24	0	0	0	0	4	0	0
25	4	0	2	0	0	0	0
26	0	0	0	0	0	0	0
27	0	0	0	0	4	0	0
28	0	2	0	0	0	0	0

2 = small defects, module operational

4 = lethal defects, module probably "dead"

Yield 91%

Sensor Count: Safety Factors

Yield estimate after metallization (Phase II): = 0.55

- Need a safety factor of **1.8** for the rest of the production steps

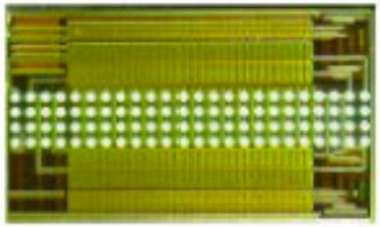
	Class 0/1	Class 2-5	Sum	PXD	Safety factor
inner	36	20	56	16	2.3
outer	70	43	113	24	2.9
Sum	106	63	169	40	2.7

Taking into account class 0 and 1 only

Pilot run with 3 “hot” wafers (10% of total wafers)

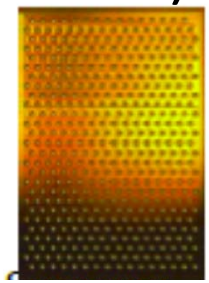
Status of ASICs

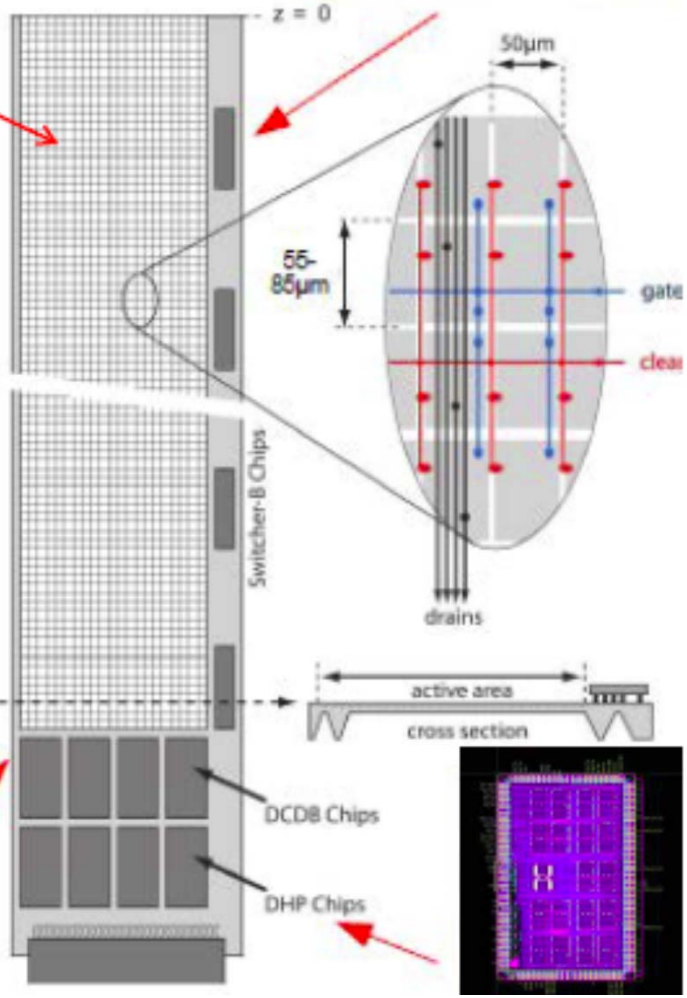
Switcher (Gated)



DEPFET Sensor

DCD (pipe -line)





DHP (1.0)

- 2nd generation ASICs
- used in electrical tests
- some smaller issues found
- will be used also for the **pilot run production**

Some concerns:

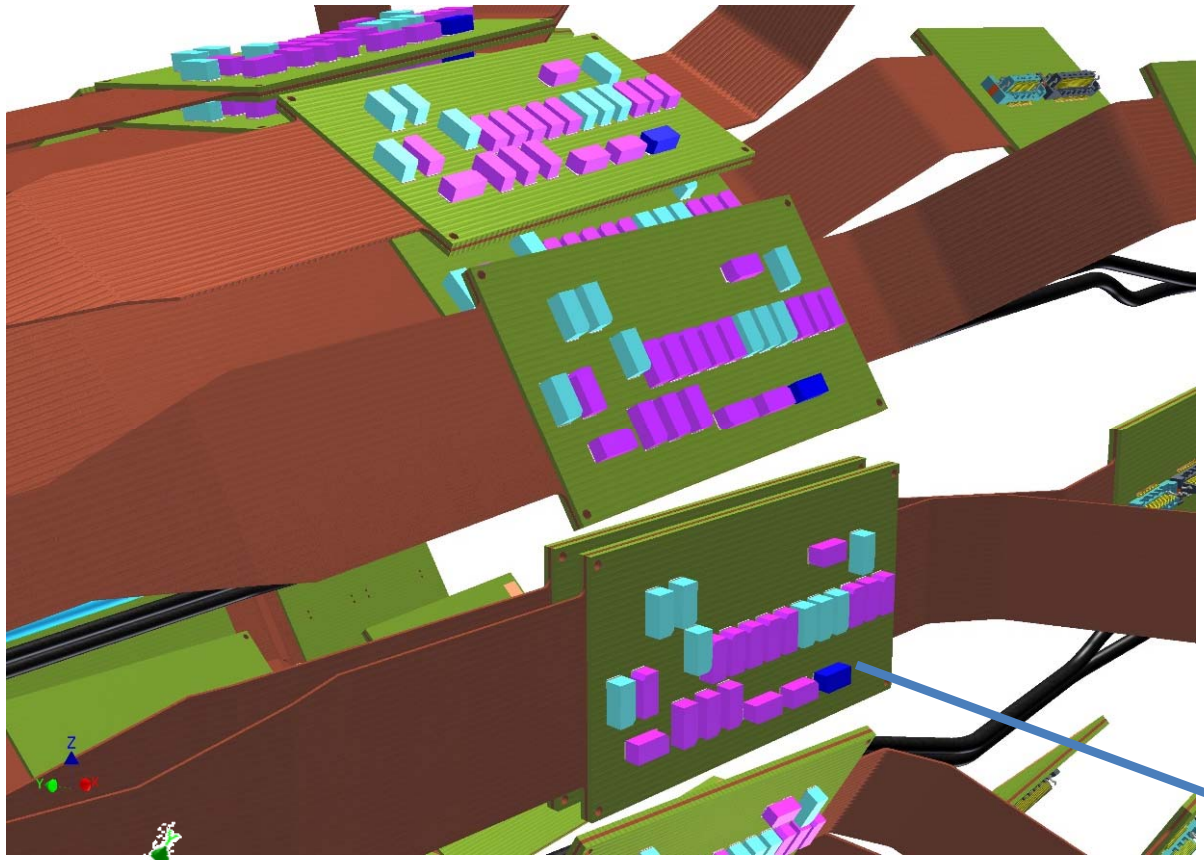
- bumping of DCDpl
- testing of ASICs before flip-chipping

Needed for final production:

- 1080 SWG
- 720 DCDpl
- 720 DHPT

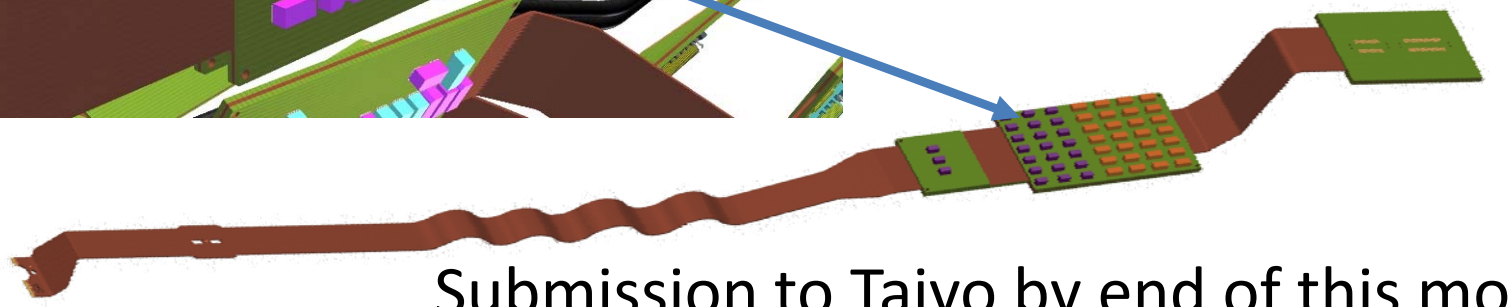
Status of Kapton Cable

Final design of Kapton cable ("outer BWD"), including passive elements, is nearing completion (4 types: FWD, BWD, inner, outer)



FWD and BWD sides different geometry (shown here is the FWD side)

Passive elements (capacitors) necessary for Gated Mode operation

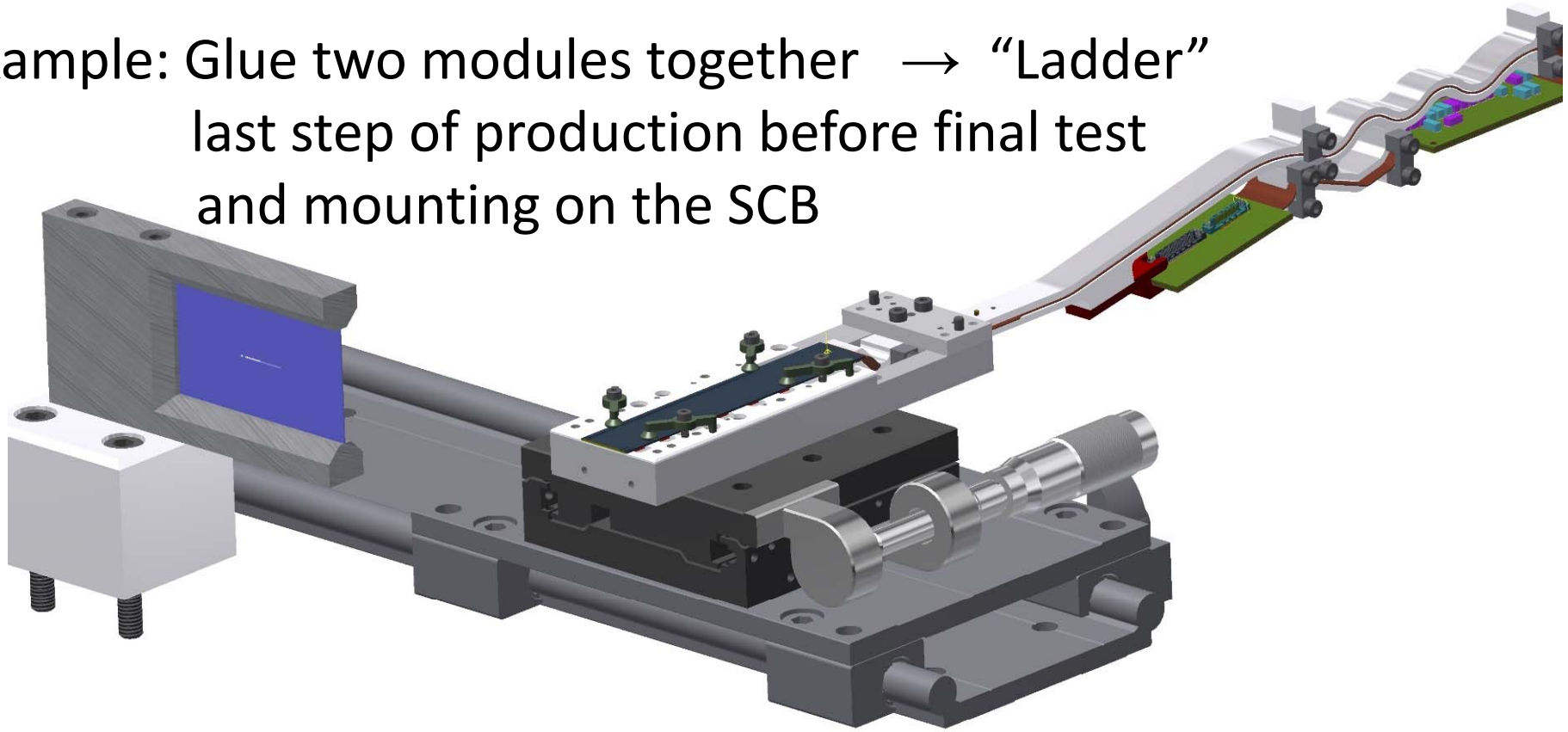


Submission to Taiyo by end of this month

Asssembly Procedures

Complicated set of jigs necessary for the various production steps (see next page)

Example: Glue two modules together → "Ladder"
last step of production before final test
and mounting on the SCB



Highest priority in the mechanics design right now

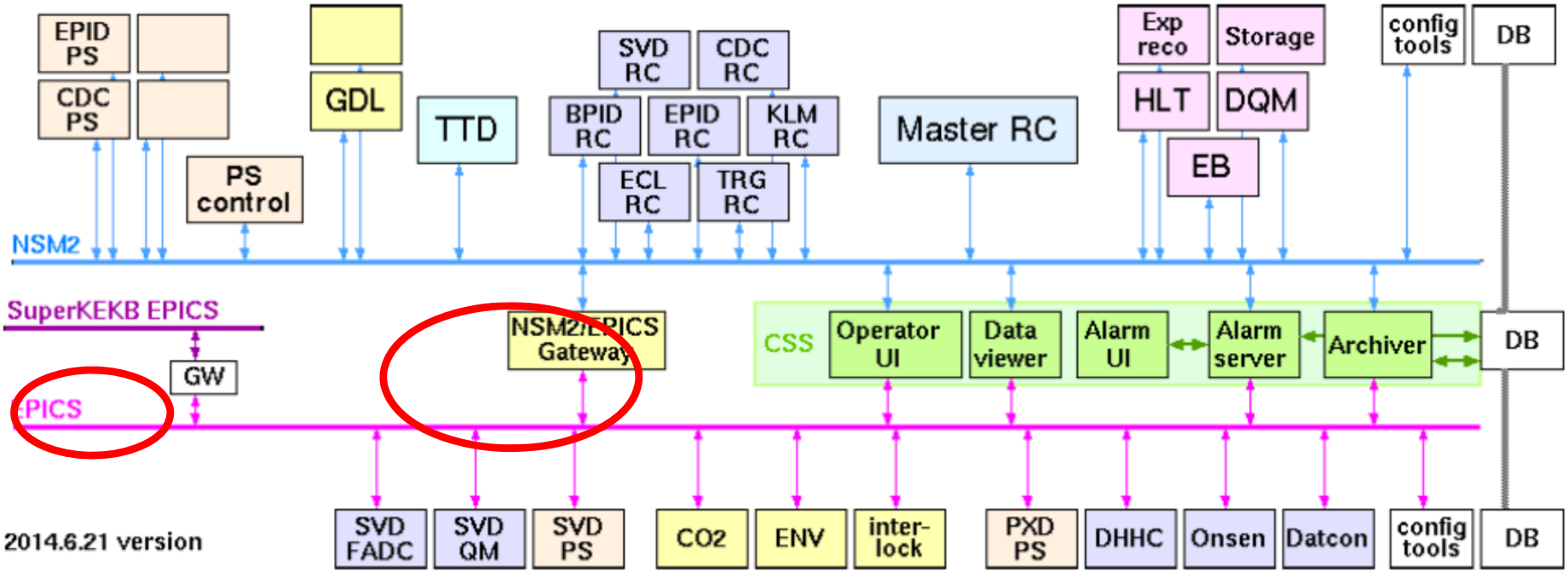
Steps During PXD Production

Item	Where
DEPFET Sensor (Phases I, II and III)	Semiconductor Lab (HLL)
Flip chipping of ASICs	IZM Berlin
mount SMDs (classify, no immediate rework)	NTC Valencia & IFIC V.
Add Kapton cable, wire bonding	MPI Munich
Gluing of two modules (= „ladder“)	MPI / HLL
Assembly of PXD half shells	MPI Munich
Commissioning PXD	MPI Munich
Assembly of PXD and Beam pipe	KEK clean room (B1)
Completion of assembly with SVD (= „VXD“)	KEK clean room (B1)
Commissioning of VXD	KEK clean room (B1)
Installation of VXD into Belle II	on SuperKEKB beam line

Services for the PXD

- DHH System: series production started
  option considered to go optical from docks to the DHH/DHE/DHC crates on top of Belle
- P/S System: series production started
- PXD-DAQ system: new carrier boards, data reduction system (DATCON and HLT ROI finders) development ongoing
- CO2 System (“IBBelle”) in phase of parts purchasing
  Cryo parts: 64 k€, Electronics: 116 k€ (180 k€ of 500 k€)

Slow Control, Data Quality



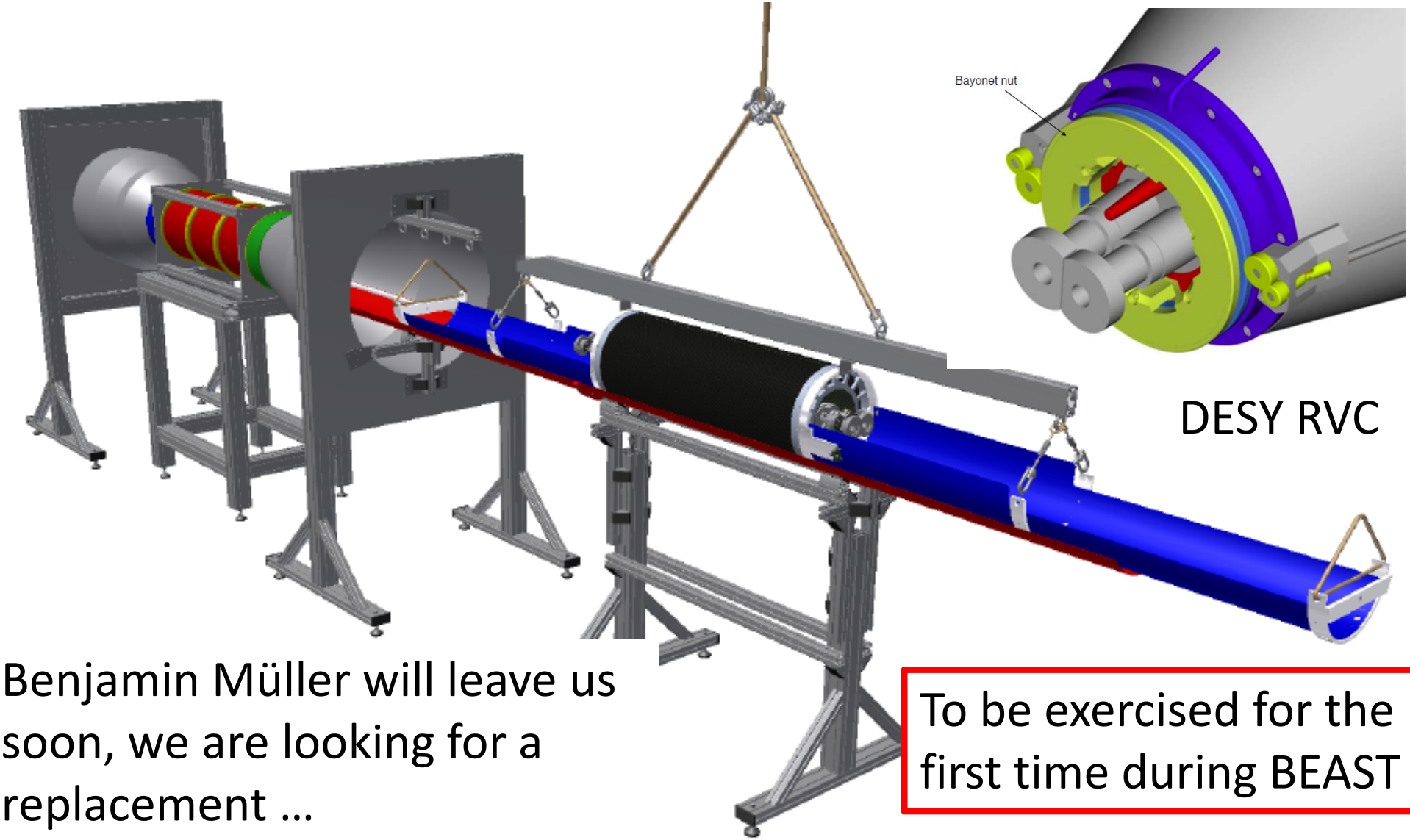
Common GUI for Belle II: CSS, NSM2 (Run Ctrl) and EPICS (Slow Contr.)

Michael Ritzert & Thorsten Röder @ KEK (September 2014):
Major Milestones achieved:

- Gateway between NSM2 and EPICS
- Present NSM2 data within CSS
- Strong support by Mainz group

VXD Installation: AIM

AIM ("Alternative Installation Method") is baseline installation
"Mockup" now has to become a fully engineered procedure

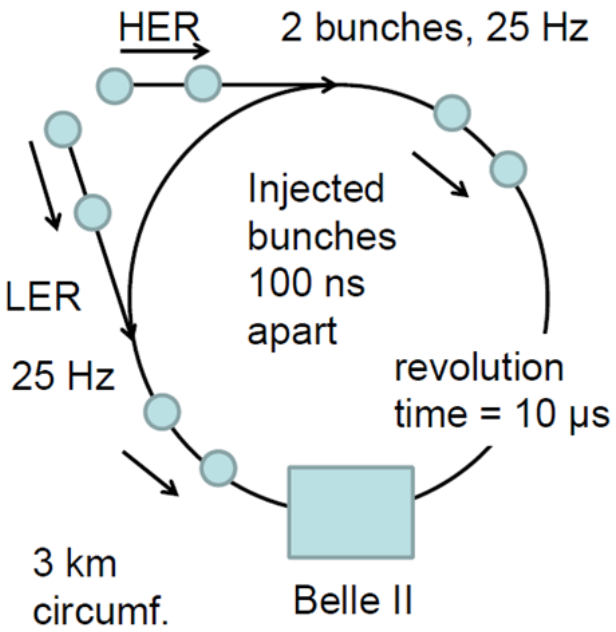


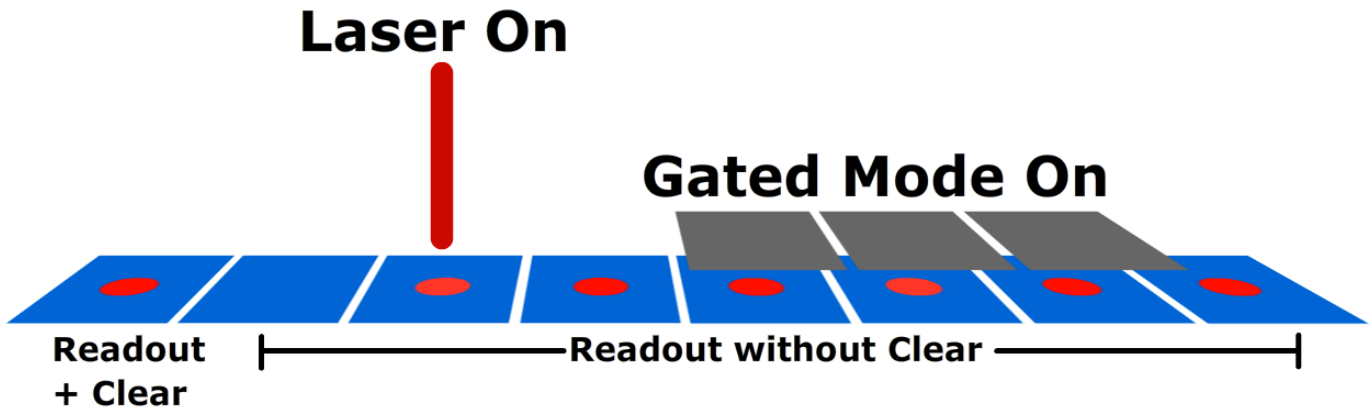
DESY RVC

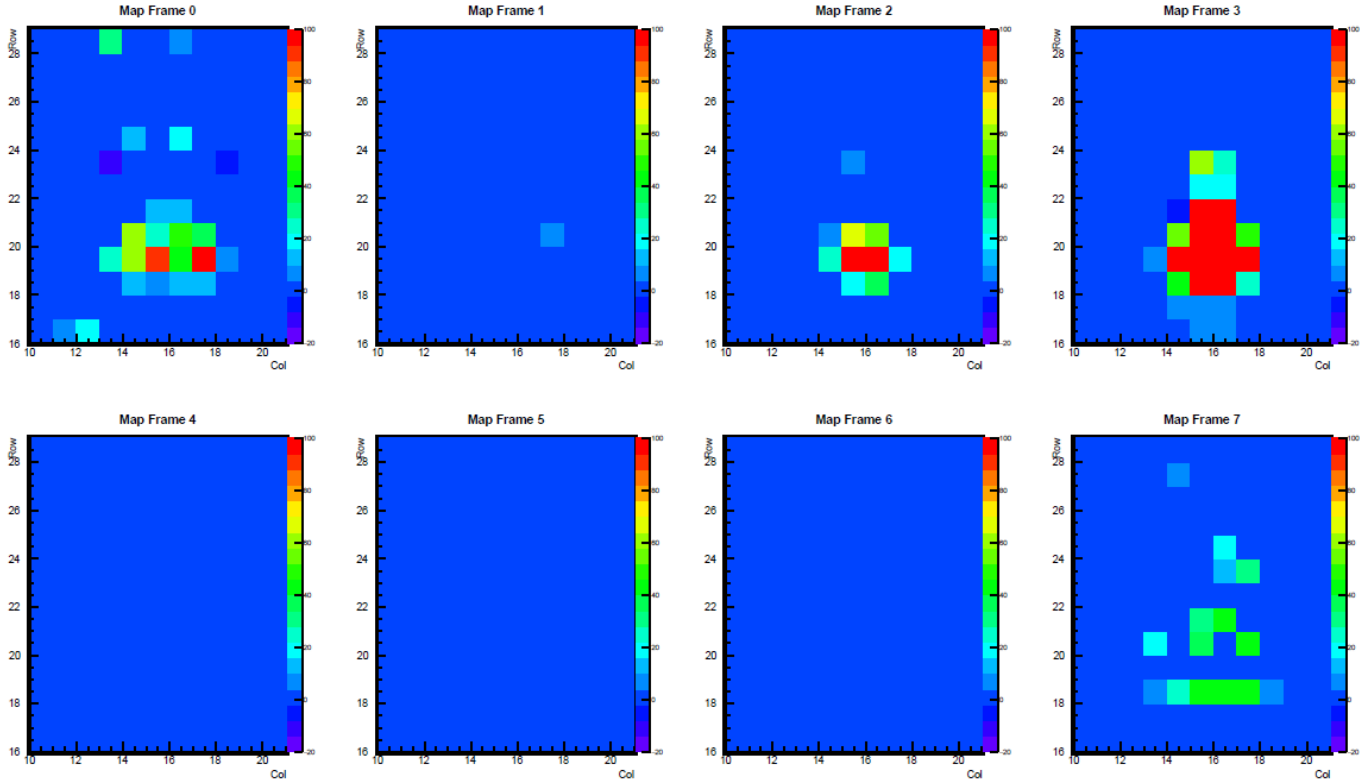
Benjamin Müller will leave us soon, we are looking for a replacement …

To be exercised for the first time during BEAST 2

Injection “Noise”





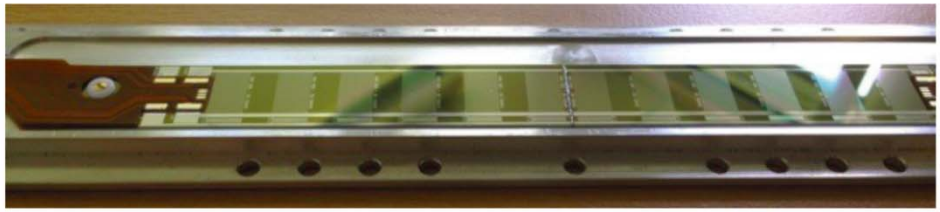


“Continuous”
injection
(ΔI/I very small)

Gating is essential

VXD Thermal Mockup

Produced at
MPI / HLL



Thermal dummy sensors

Tscharlie
Ackermann
MPI

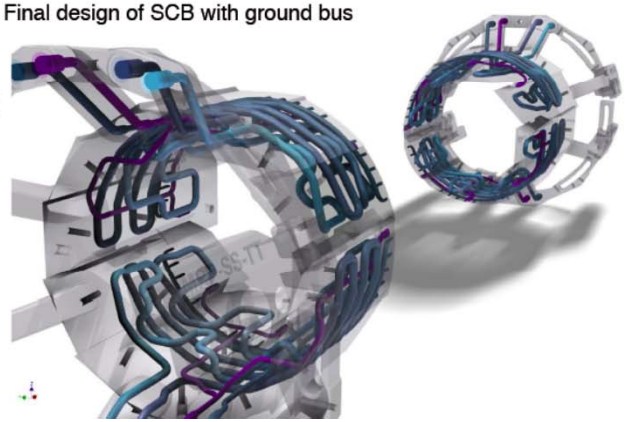
Full dummies produced,
now under measurement to
study gluing process

Kapton heating

Kapton flex

Support

Final design of SCB with ground bus



Production had some
delay, now preparing for
pressure tests at MPI

BEAST Phase 2: The "VXDP2"

- Phase 2:
  - Belle II on beamline, fully installed **except VXD**
  - Final Focus System (QCS) installed for the first time.
  - Final beampipe and HM masks around IP
  - First attempt to collide beams and achieve $1x10^{34}$ /cm s

- Determine particle/photon fluxes for the individual background contributions (syn.rad., Touschek, rad. Bhabha, 2γ)

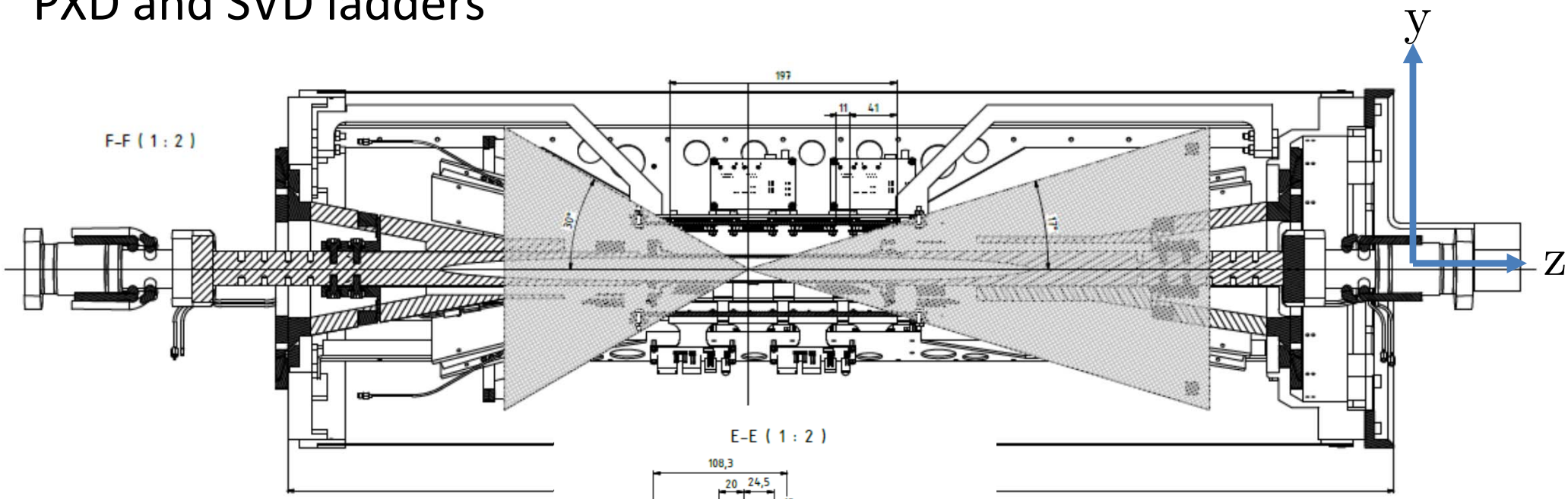
- Study injection bg and exercise gated mode operation of VXD

- Determine bg status safe for PXD/SVD, exercise H/W interlock, radiation & environmental monitoring (!)

- Install one sector (=6 ladders) of PXD and SVD in accel. plane

VXD Equipment during Phase 2

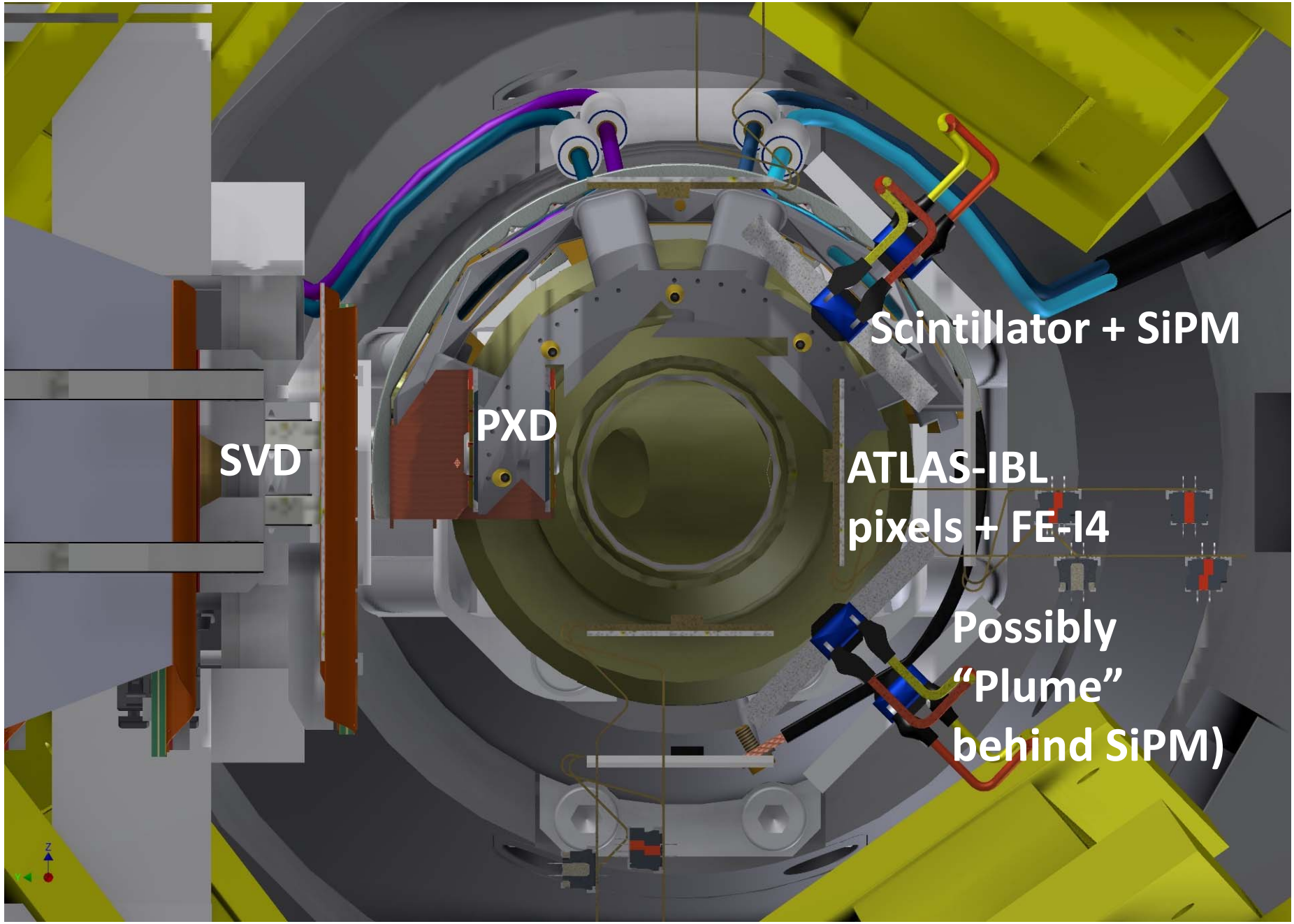
Plan: Cover large part of the area not instrumented by PXD and SVD ladders



Additional sensors to be placed in the accelerator plane and perpendicular to it
(+ envir. & rad. monitors)

Requirement:
ΔE/E ~ 20% @ 5 keV
Δt ~ 1-20 ns
-> ATLAS IBL pixels
"ILC" sciniillators
+ SiPM readout

VXD Equipment during Phase 2



Conclusion & Outlook

- DEPFET PXD9 Phase I production finished, 30 wafers, 180 matrices
- Pilot Run with 3 “hot” wafers (10 %) + 5 PXD9 dummy wafers ongoing
- Present generation of ASICs suited for Gated Mode testing with PXD9, final submission optimally by end of June 2015 (hopeless?)
- DCD production including bumping mandatory, SWB bumping at PacTech
- SMD procedure MUST BE established **until end of February 2015, NOW need to think of “Plan B”**
- DESY Thermal Test 2015 progressing, ladders built, SCBs in process
- Concrete planning for BEAST Phase 2 (“VXDP2”) has started, contributing groups are identified

Major Milestones for the Coming 2 Years

- Pilot Run with first “hot wafers” (test by summer of 2015)
  (need tested ASICs and established SMD mount procedure)
- DESY Thermal Test (includes PXD and SVD dummies) in 2015
- Build IBBelle by fall of 2015, complete commissioning by 3/2016
- Build 2 ladders (from Pilot Run) for DESY VXD Beam test
  (Jan, 2016), prepare Slow Control for VXD
- Final ASICs by spring 2016 (test with Pilot run sensors)
- Build BEAST 2 sensor systems (FE-I4 and Scint/SiPM) by end 2016
- Finish PXD module / ladder production by spring 2017

Backup

Program for Spare / Upgraded PXD

- Construct spare PXD by the summer of 2019 (~ 5 years from now)
  Plan supported by Belle II management

- Need 2 years of production of sensors + < 2.5 years for construction, optional development of new ASICs, and commissioning

  -> continue production of new sensors when the present production is finished (sensors will be paid by MPI)

  -> Funding for electronics requested from BMBF for 2015-18

- Development of ASICs (+DAQ H/W) should wait for significant experience in beam operation (start development in 2017)

Pilot Assembly

- Start a pilot run with PXD9 3 wafers + 5 wafers “EMCM”-type (final metallization + thinning)

- Equip sensors with present ASICs (Gates Mode should work)

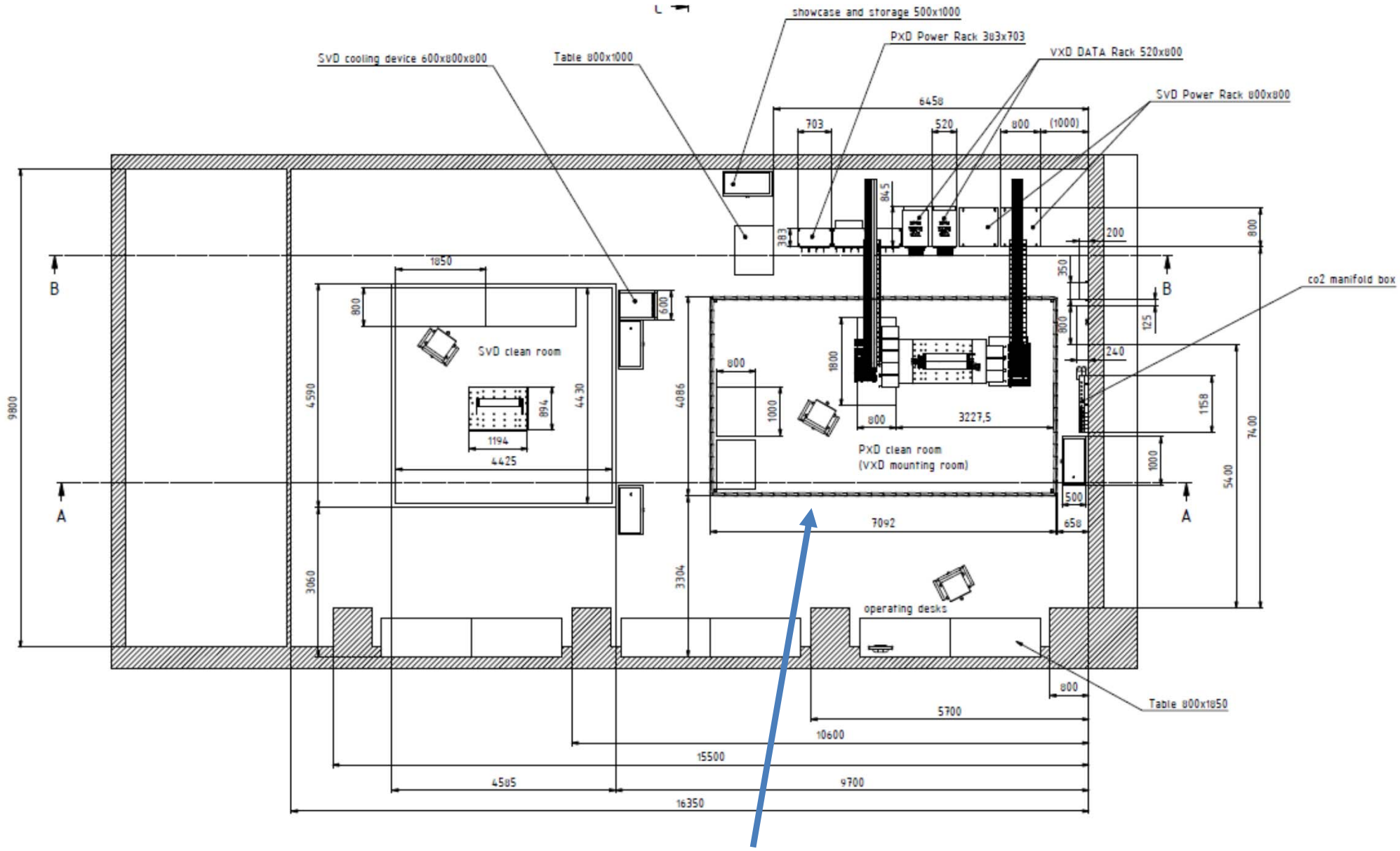
- Submit “final” Kapton design in Jan. 15 (back by March 2015)

- Do thorough tests with full modules assembly (+ gated mode) (flip chip @IZM Germany, SMD @ NTC Valencia

- Submit final ASICs by end of June 2015

- Prepare beam test (at DESY) with 2 sensors (ladders) together with final SVD ladders for the fall of 2015
(BEAST Phase 2 will have final ladders)

Phase 2 / PXD Integration



VXD Assembly clean room in B1