Belle II Note
Number 0010

The vertex detector numbering scheme

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Abstract

This note describes the numbering scheme for both the Pixel Vertex Detector (PXD) and the Silicon Strip Detector (SVD) of Belle II. These vertex detectors share a similar geometrical structure of their constituents and can therefore be described using the same numbering scheme. This note also introduces the Belle II coordinate system and the detailed numbering scheme for individual pixels and strips for the PXD and SVD respectively.

1 Introduction

The physics program of Belle II demands very high precision for the reconstruction of decay vertices. In order to satisfy this demand, the Belle II detector is equipped with two highly granular vertex detectors. The first of the two detectors is the Pixel Vertex Detector (**PXD**, see figure 1). It is the innermost detector, with its first sensitive layer being located only 14 mm in radial direction from the interaction point (**IP**). The PXD consists of two layers, with 8×2 active sensors for the first layer, and 12×2 active sensors for the second. Each active sensor is a matrix of 768×250 pixel cells using the DEPFET technology.

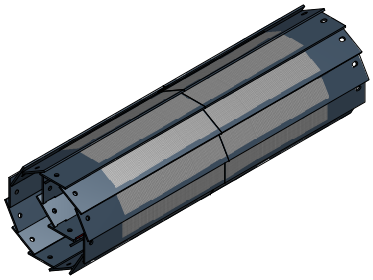


Figure 1: The Pixel Vertex Detector (PXD).

The second detector is the Silicon Strip Vertex Detector (**SVD**) which consists of 4 layers of double sided strip detectors. Like the PXD, the layers of the SVD are arranged cylindrically around the IP. However, the outer 3 layers of the SVD have slanted parts in the forward region of the detector. This optimizes the material budget for particles flying into the forward direction and saves costs due to the reduced sensor area.

Though each detector uses different technologies to measure the passage of particles through their active areas, they share a very similar geometrical hierarchy. Therefore, the PXD and SVD detector groups agreed upon a common naming scheme for their respective detectors.

This note describes this naming scheme. Section 2 is an introduction to the coordinate system of Belle II, followed by an in-depth description of the numbering scheme in section 3 and its notation in section 4. The note closes with the definition of the numbering for individual pixels in section 5.1 and strips in section 5.2.

2 Coordinate system of Belle II

The Belle II detector is described using a **Cartesian, right-handed** coordinate system. The **origin** of the coordinate system is located at the nominal interaction point, with the axes described as follows: the z **axis** pointing along the direction of the magnetic field of the solenoid; the y **axis** pointing upwards, in the direction of the detector hall roof; and the x **axis** pointing along the radial direction towards the outside of the accelerator ring. This definition is shown in figure 2.

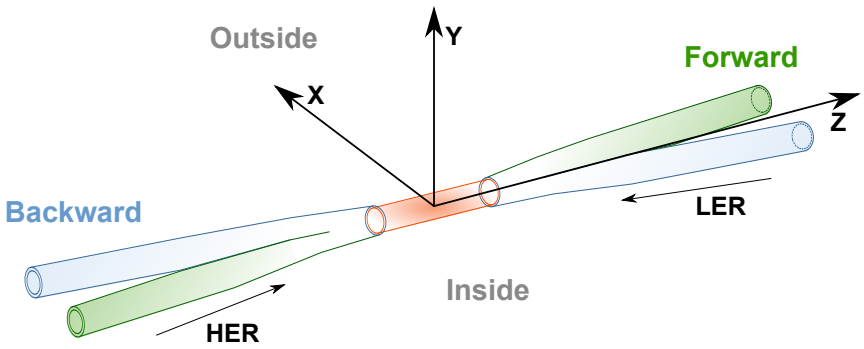


Figure 2: The Belle II coordinate system.

Due to the boost, a **forward** $(+z)$ and **backward** $(-z)$ region can be clearly defined. The coordinate system's positive z axis points towards the forward direction, and the negative axis towards the backward direction.

If not otherwise specified, all xy projections showing any part of the Belle II detector should be drawn such that the projected detector is seen from the forward to the backward direction. This means that the z axis should point out of the page, the x axis to the right and the y axis upwards.

3 Numbering scheme

The numbering scheme for the PXD and SVD detectors and their constituents relies on their common geometric hierarchy. The hierarchy is given as follows: each detector can be subdivided into two or more **layers**; each layer consists of several **ladders**; each ladder hosts two or more **sensors**. Those sensors are the active areas of the detector and measure the position of a traversing charged particle. Table 1 gives the numbers of ladders and sensors for each layer.

	Layer ID	Number Ladders	Number Sensors	Radius [mm]
PXD	1	8	2	14
PXD	2	12	2	22
SVD	3	7	2	38
SVD	4	10	3	80
SVD	5	14	4	104
SVD	6	17	5	135

Table 1: Ladder and sensor numbers for the PXD and SVD

3.1 Layer numbering

The innermost layer is given the ID **1**. The layer ID is then increased by one for each layer, stepping outwards along the radial direction as shown in table 1 and figure 3. The complete vertex detector consists of 6 layers, where layer IDs **1**and **2** describe the layers of the PXD and layer IDs **3** to **6** those of the SVD.

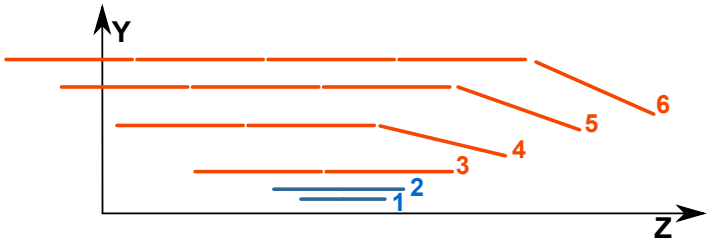


Figure 3: The layer numbering of the PXD (blue) and the SVD (orange).

3.2 Ladder numbering

With a xy projection of the PXD and SVD in mind, the numbering of the ladders starts at the right side of the detector ($+x$). In particular, the innermost ladder intersecting the positive x axis is specified to carry the ID **1**. The ladder ID is increased by one, following the ladders in a counter-clockwise direction. Figure 4 shows the ladder numbering for the PXD and figure 5 the numbering for the SVD.

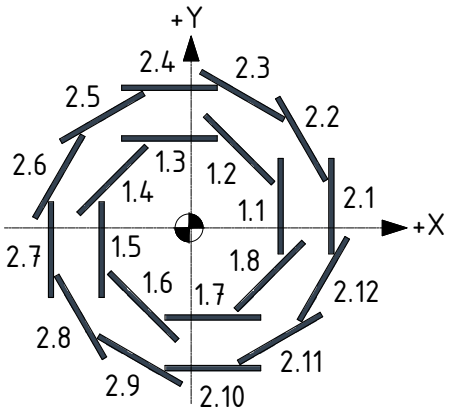


Figure 4: The ladder numbering for the PXD

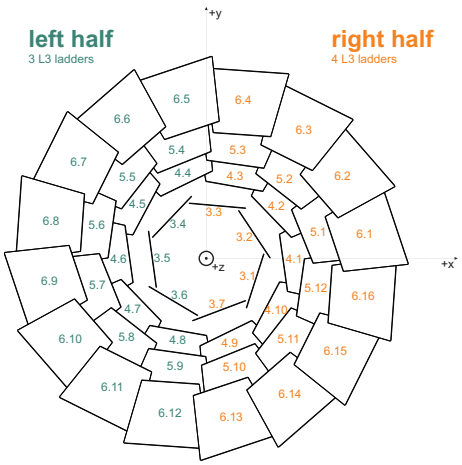


Figure 5: The ladder numbering for the SVD

3.3 Sensor numbering

Each ladder hosts two or more sensors, labeled in the following way: the first sensor starting from the forward part of a ladder (the part which is most positive in the z axis) is given the ID **1**. The ID is increased by one for each sensor, following the ladder along the backward direction (along the z axis). Figure 6 shows the sensor numbering for the PXD and figure 7 the numbering for the SVD.

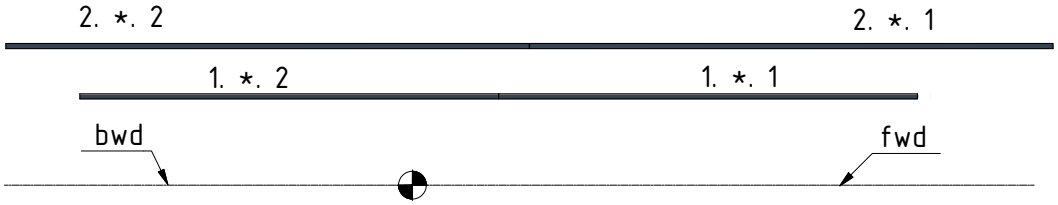


Figure 6: The sensor numbering for the PXD

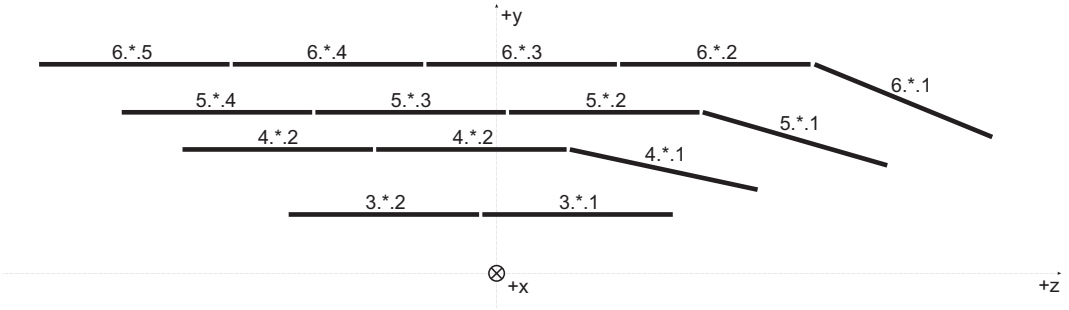


Figure 7: The sensor numbering for the SVD

4 Notation

Addressing a given sensor requires the three IDs for layer, ladder and sensor. The notation agreed upon is for the IDs to be listed in the order of layer, ladder and sensor using a point character (" . ") as the delimiter. For example: "**1.4.2**" specifies the first layer, fourth ladder and second sensor. In this example this would be the backward sensor, which is located on the fourth ladder of the first (innermost) layer of the PXD.

An asterisk can be used to address all layers, ladders or sensors. For example: "**1.*.2**" specifies all backward sensors of the first layer. To keep the notation short, trailing asterisks can be omitted: the notation "**1.*.***" is equivalent to "**1**" and describes all ladders and sensors of the first layer. Please see figure 6 for an example of the use of this notation.

This notation is also supported by the Belle II software framework and can be used to send a string query for a specific sensor to the geometry system.

5 Numbering of Pixels and Strips

5.1 The PXD pixel numbering scheme

5.1.1 How to address the pixels

The pixels of the PXD half ladders are addressed by their row and column numbers. However, there are two different definitions of rows and columns:

Geometrical row: A geometrical row is defined as a set of neighboring pixels parallel to the short edge of the sensor. For all half ladder types the geometrical rows are numbered from 1 to 768.

Geometrical column: A geometrical column is defined as a set of neighboring pixels parallel to the long edge of the sensor. For all ladder types the geometrical columns are numbered from 1 to 250.

Electrical row: An electrical row (or gate row) is defined as a set of pixels which is switched on and off simultaneously by a single Switcher channel. Each electrical row consists of four geometrical rows. This is the famous "four-fold readout" of the PXD sensors. For all half ladder types the electrical rows are numbered from 1 to 192.

Electrical column: An electrical column (or drain line) is defined as a set of pixels which is read out by the same channel of the Drain Current Digitiser (DCD) chip. This pixel set contains every fourth pixel of a geometrical column. For all half ladder types the electrical rows are numbered from 1 to 1000.

Figure 8 illustrates the fourfold readout and the pixel addressing. It is custom to display a pixel matrix in portrait mode with rows oriented horizontally. Following the mathematical convention, pixels are addressed by specifying their *geometrical* row number first, followed by their *geometrical* column number.

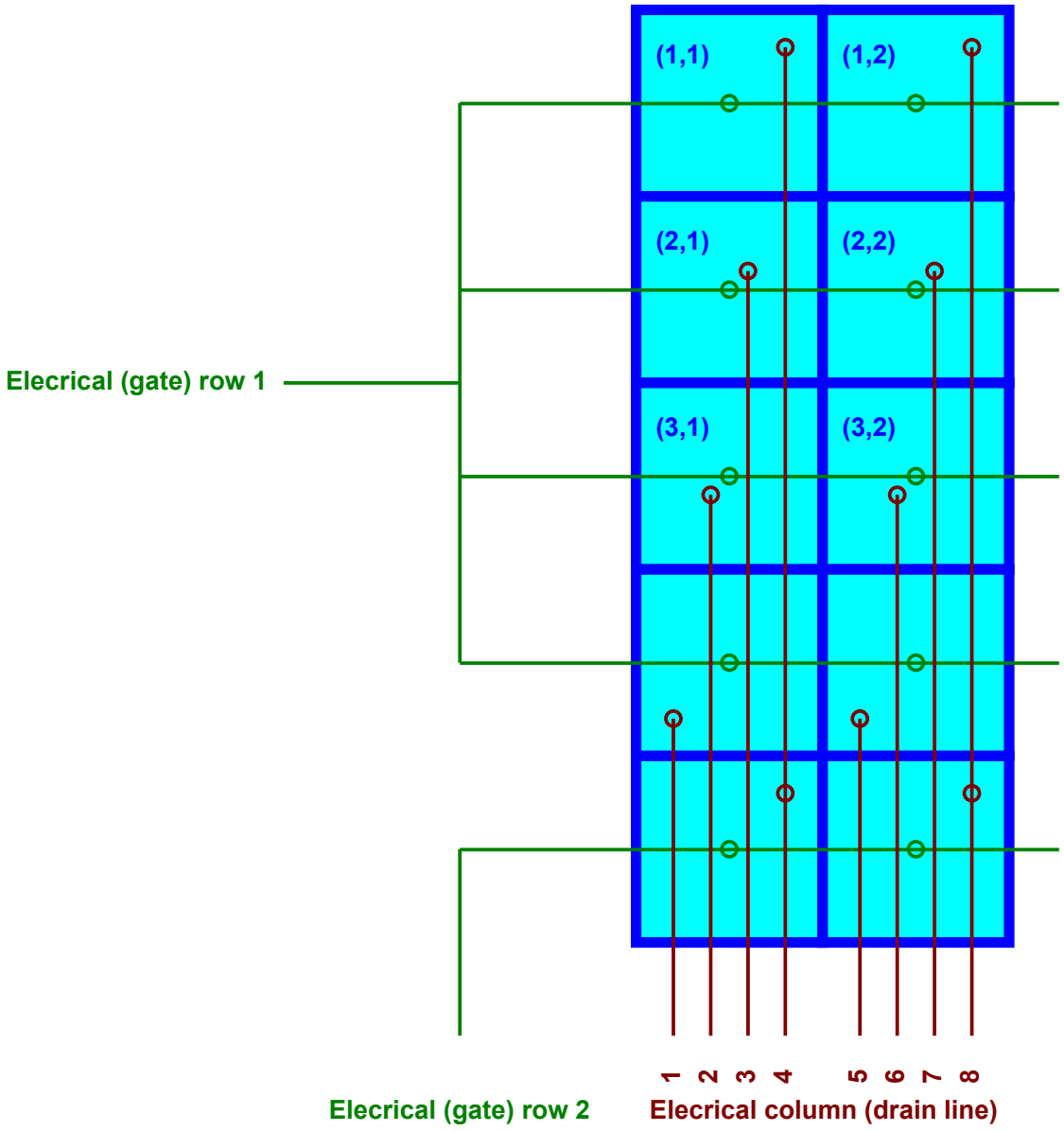


Figure 8: The fourfold readout of the PXD pixel matrices. Green: The electrical (gate) rows connect to four geometrical rows simultaneously. Red: The electrical columns (drain lines) connect to every fourth pixel of a geometrical column. Blue: The pixels are addressed by (r,c), where r is the *geometrical* row number and c is the *geometrical* column number, following the mathematical convention. This assumes that the rows are displayed horizontally.

5.1.2 ASIC numbering and local coordinate system

The readout ASICs are numbered according to their position in the JTAG chain, i.e. the sequence in which they are addressed by the readout electronics. The resulting numbering is displayed in figure 9.

Rule of thumb: Look at the half ladder from top (i.e. you see the ASICs), and turn it so that the ASICs you are interested in are close to you. Then the ASICs are numbered ascending from left to right. This works for all ASIC types and all half ladder types.

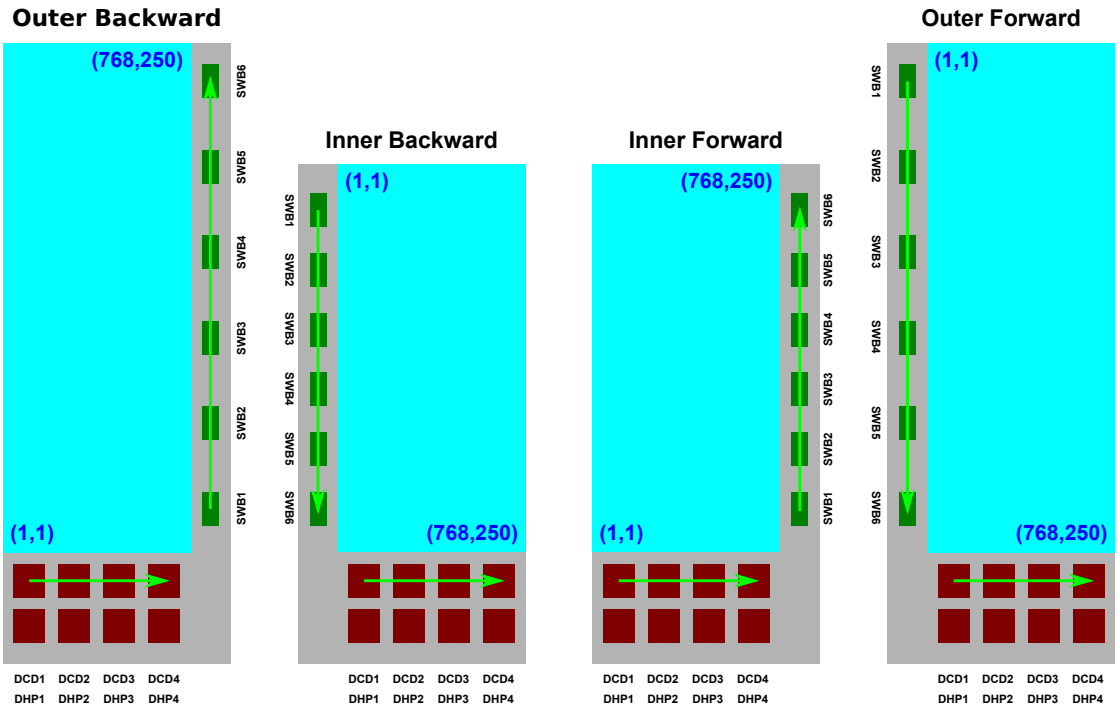


Figure 9: The numbering of the readout chips is dictated by their position in the JTAG chain, i.e. the sequence in which they are addressed by the readout electronics. Rule of thumb: Look at the half ladder from top (i.e. you see the ASICs), and turn it so that the ASICs you are interested in are close to you. Then the ASICs are numbered ascending from left to right. The green arrows show the natural coordinate directions, which are given by the channel numbering of the readout chips. This translates to a numbering scheme of the geometrical pixel rows r and columns c, displayed as blue coordinate pairs (r,c).

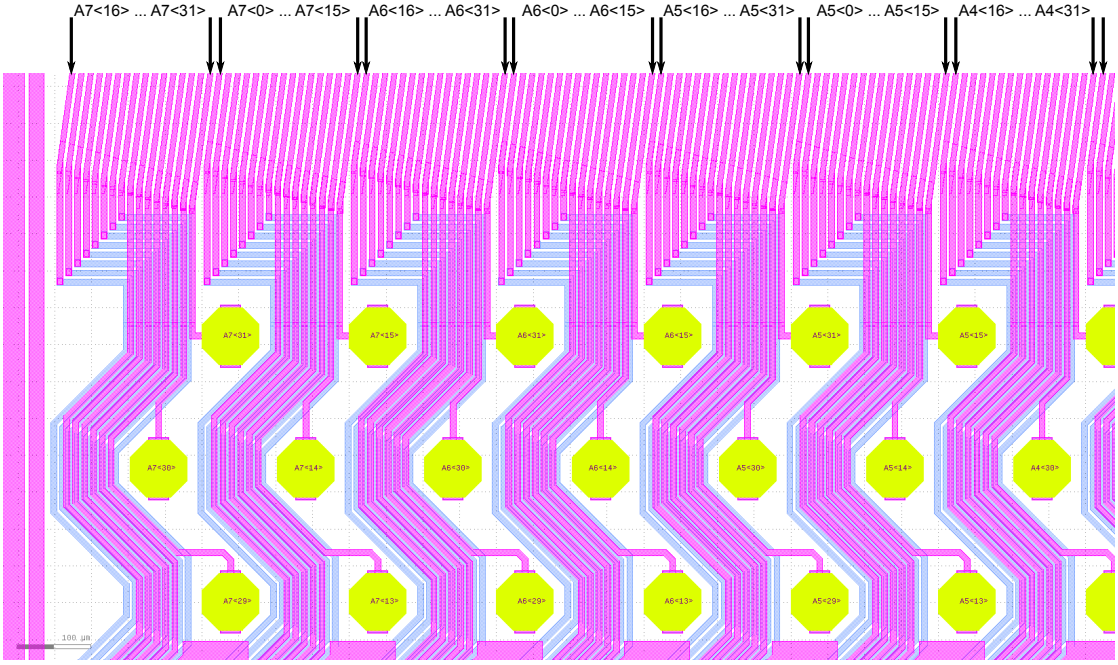
The channel numbering of the ASICs defines the row and column numbering direction, and therefore also the coordinate directions in the local coordinate system of the half ladder. The relevant ASICs define their channel numbering as follows:

- Drain Current Digitiser (DCD): The output of the DCD is multiplexed and uses eight parallel lines. Therefore, also the input pads are grouped into eight so-called "DCD columns" (not to be confused with the columns of the matrix). Each DCD column consists of two sets of 16 input pads (DCD half-columns). Figure 10a shows the footprint of a DCD in the following orientation: Assume the DCD to be flip-chipped onto the half ladder, and you look at the side of the half ladder where you see the ASICs. The sensitive part of the sensor is facing away from the observer, the end-of-stave (holding the DCDs and DHPs) is near the observer. The DCD column A0 is on the right edge of the chip, column A7 is on the left. The channels of the first DCD half-column are numbered from Ai<0> to Ai<15> counting towards the sensitive part. The next 16 channels are located to the left, numbered from Ai<16> to Ai<31> counting towards the sensitive part. In contrast, the drain lines (electrical columns) routed to the DCD input pads are numbered ascending from left to right, inside a DCD half-column. So, while there is no monotonic behavior of overall DCD channel numbering, it is advisable to follow the numbering inside a DCD half-column and define the coordinate direction from left to right. That way, we slice the matrix into 16 parts, inside each of which neighboring drain lines are counted ascending from left to right.
- Switcher: Figure 10b shows the footprint of a Switcher in the following orientation: Assume the Switcher to be flip-chipped onto the half ladder, and you look at the side of the half ladder where you see the ASICs. The sensitive part of the sensor is facing away from the observer, the balcony holding the Switcher is near the observer. The Switcher channels (both the Clear rows and the Gate rows) are numbered ascending from left to right. The Switcher channels are enabled one after the other, in ascending direction. Only the four geometrical rows corresponding to the currently enabled electrical row are read out at a time. This is the rolling shutter readout.

The counting directions of the readout chips translate to directions of the natural coordinates as shown in figure 9. Note that the balcony holding the Switchers changes position depending on the half ladder type. This leads to a different direction of the rolling shutter readout and a different natural coordinate direction.

Rule of thumb: Look at the half ladder from top (i.e. you see the ASICs), and turn it so that the ASICs you are interested in are close to you. Then the coordinate direction ($R\Phi$ for the DCDs, z for the Switchers) point from left to right. This works for all ASIC types and all half ladder types.

When the half ladders of figure 9 are mounted in the PXD, they are turned and rotated in space and end up in the positions shown in figure 11. This translates to the natural coordinate system $(R\Phi, z)$ of the PXD shown in figure 12.



(a) DCD footprint on the substrate of the half ladder. While the DCD columns are numbered from right to left, the channels inside each DCD half-column correspond to a drain line numbering which is ascending from left to right.

(b) Switcher footprint on the substrate of the half ladder. Both Clear and Gate lines are numbered ascending from left to right.

Figure 10: Footprints of the readout ASICs

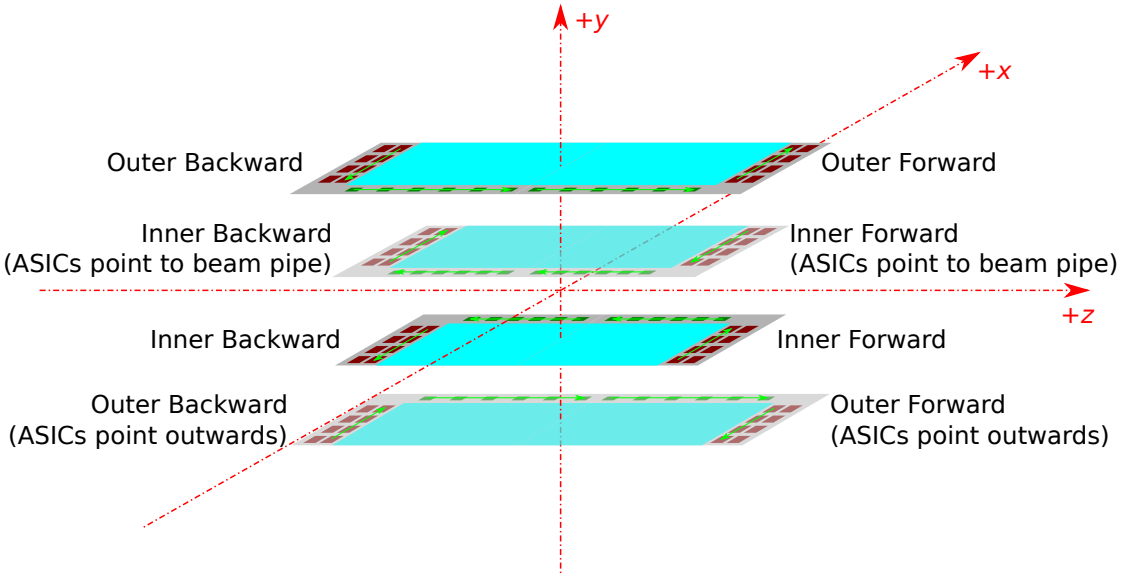


Figure 11: Natural coordinate directions of the ladders 1.3 and 1.7 (inner layer 1), and 2.4 and 2.10 (outer layer 2). The PXD half ladders of the inner layer 1 are mounted with the ASICs facing towards the beam pipe, while those of the outer layer face away from the beam pipe.

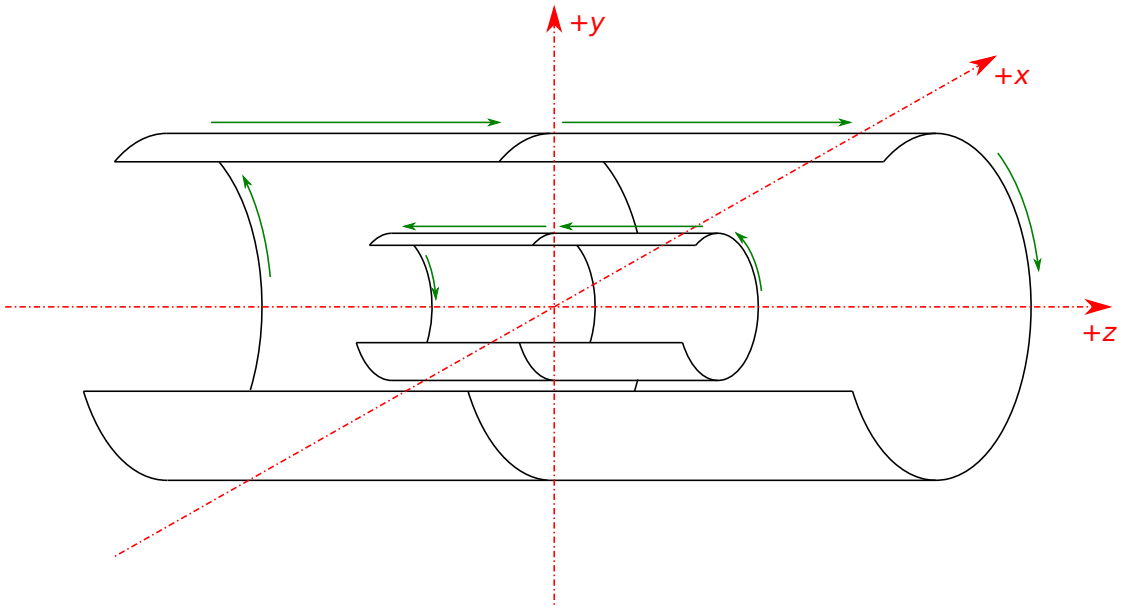


Figure 12: The natural coordinate system of the PXD, as derived from figure 11. The z coordinates of forward and backward half ladders point in the same direction within the same layer, but are different for layer 1 and 2. The $R\Phi$ coordinate changes direction even within the same layer.

5.2 The SVD strip numbering scheme

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