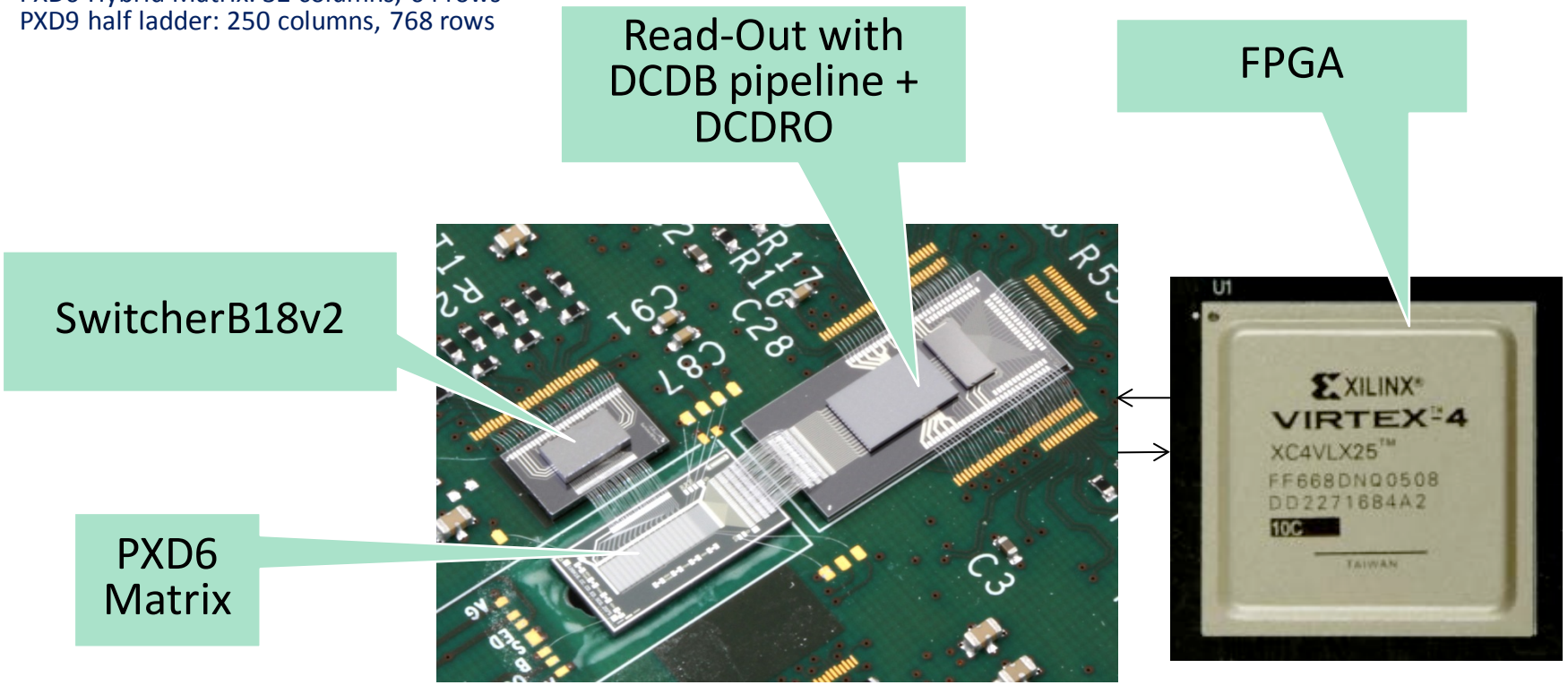
Gated Mode Pedestal Analysis

Hybrid Board H4.1.07

PXD6 Hybrid Matrix: 32 columns, 64 rows
PXD9 half ladder: 250 columns, 768 rows



Switch the DEPFET into gated mode:

- change the clear voltage to high and keep the gate in off state
- Laser pulse is controlled by a Trigger (TLU plus Pulse Generator)

Test Program

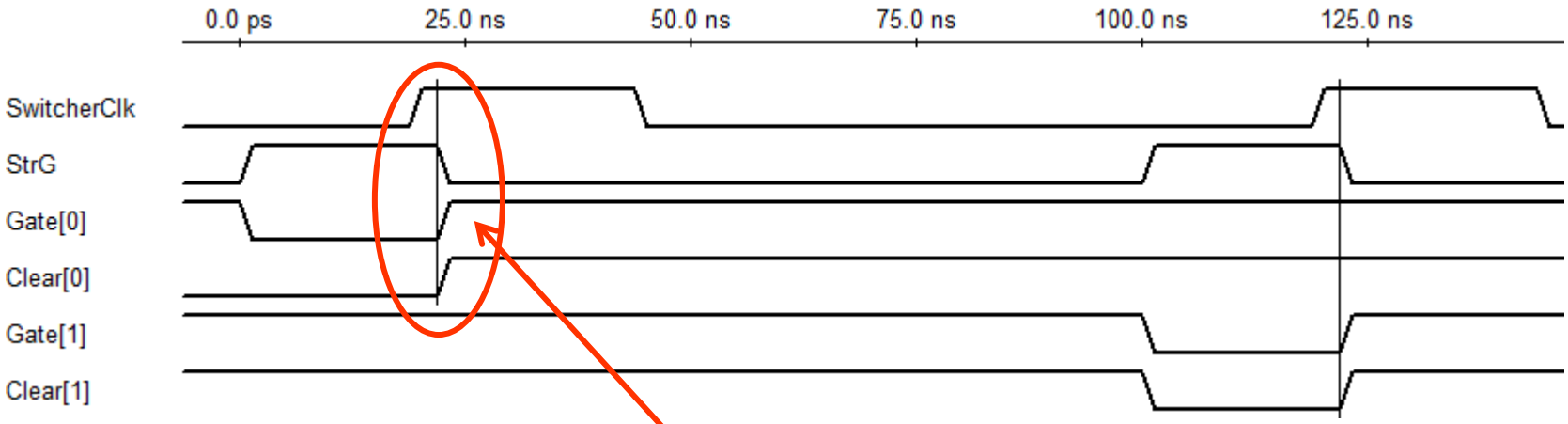
- To evaluate if the gated-mode works, readout of 8 consecutive DEPFET frames for each trigger

- Experiment A: “Signal Charge Storage”
  - Laser impinges on DEPFET pixels in sensitive mode → hit pixel collects charge
  - Enter gated mode, measuring charge in reference frame
  - → Goal: no charge loss from internal gate to clear

- Experiment B: “Junk Charge Generation”
  - Laser impinges on DEPFET pixels in blind mode → internal Gate is shielded
  - Exit blind mode in consecutive frames

  → Goal: hit pixel collects **no** charge from laser into internal gate

Gated mode with read-out

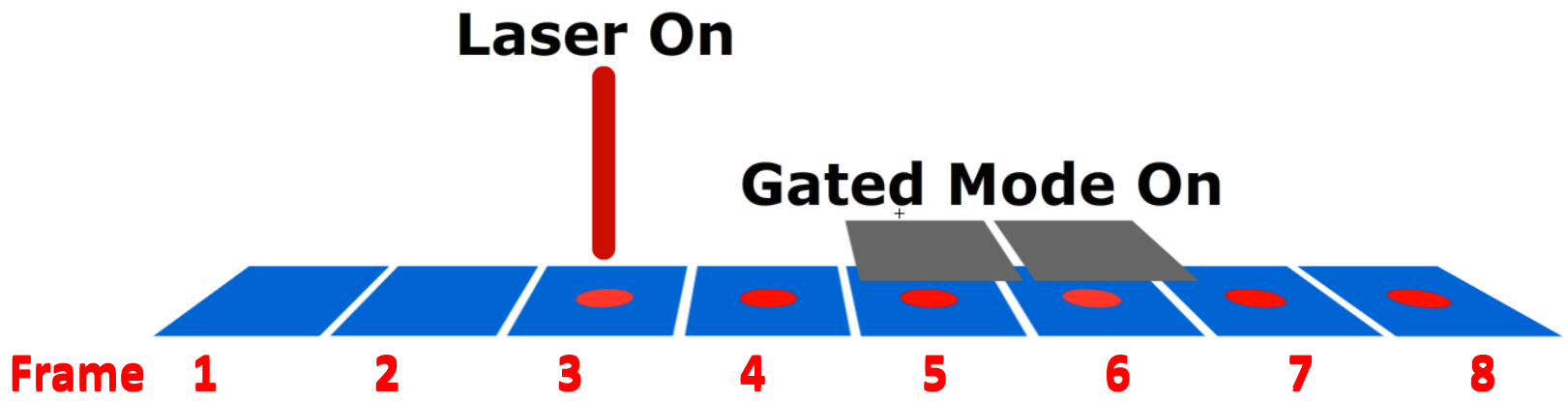


Enabling Gated Mode with read-out:

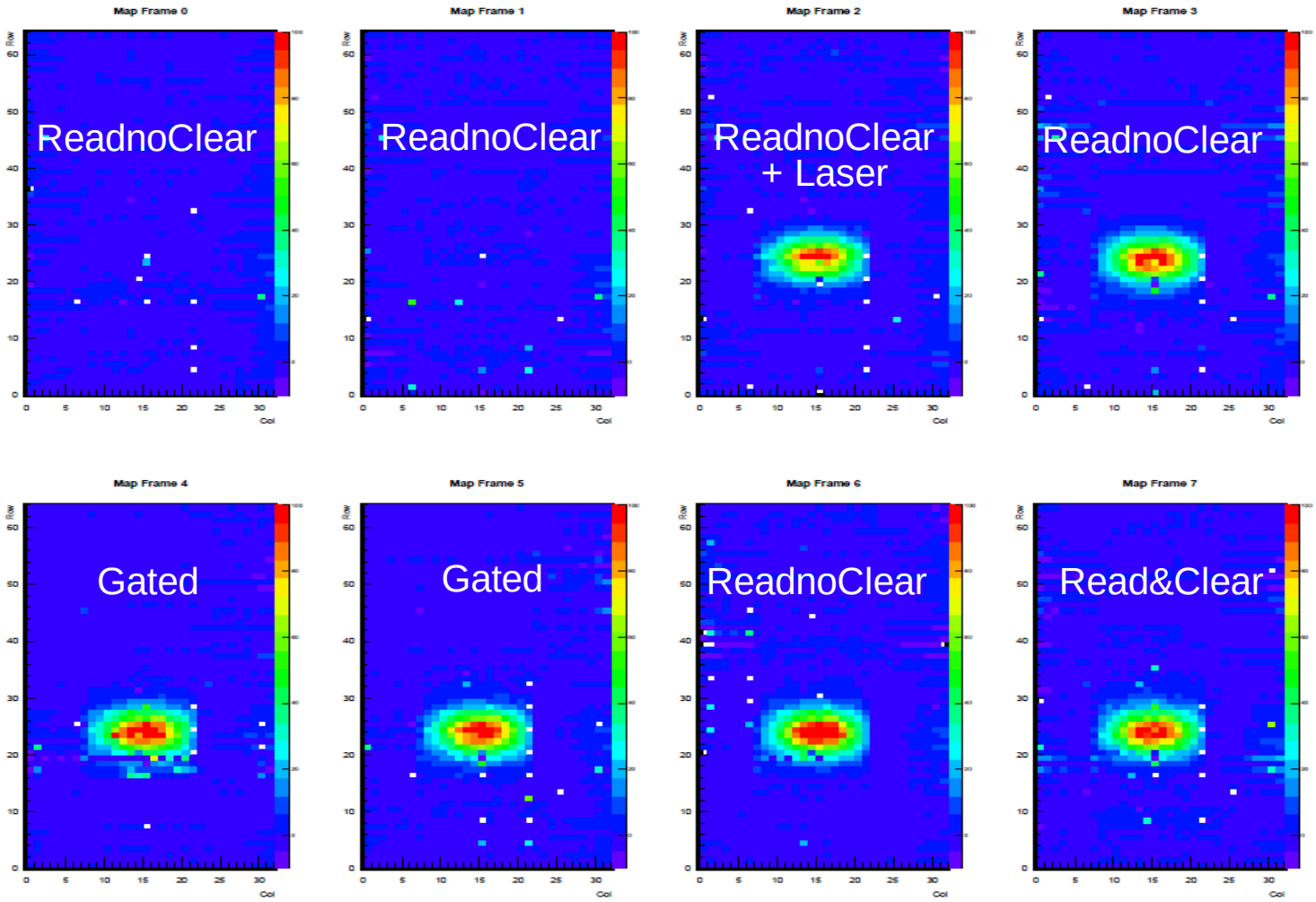
- SwitcherClk on high level & continues running, falling edge of StrG
- Clear changes to high level immediately on non-active channels
- Rolling shutter mode continued, no clear on activated channels

Experiment A: *Signal Charge Storage*

Frame n	Frame 0	Frame 1	Frame 2	Frame 3	Frame 4	Frame 5	Frame 6	Frame 7
Normal sequence	ReadnoClear	ReadnoClear	ReadnoClear + Laser	ReadnoClear	Gated Mode	Gated Mode	ReadnoClear	Read & Clear



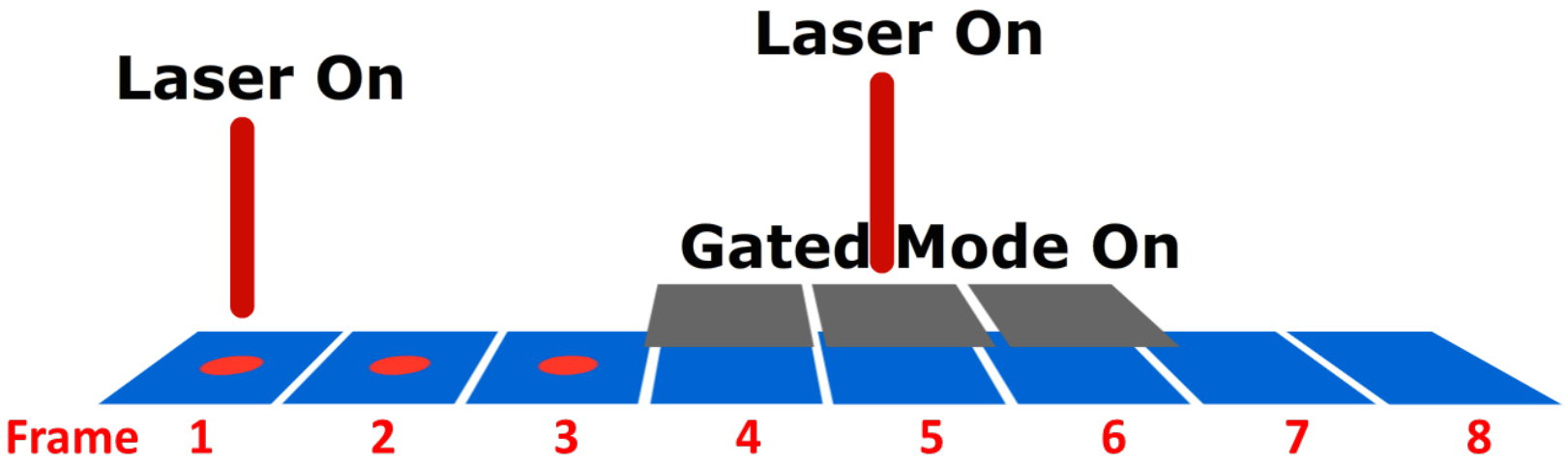
Gated Mode with RO – *Signal Charge Restore*



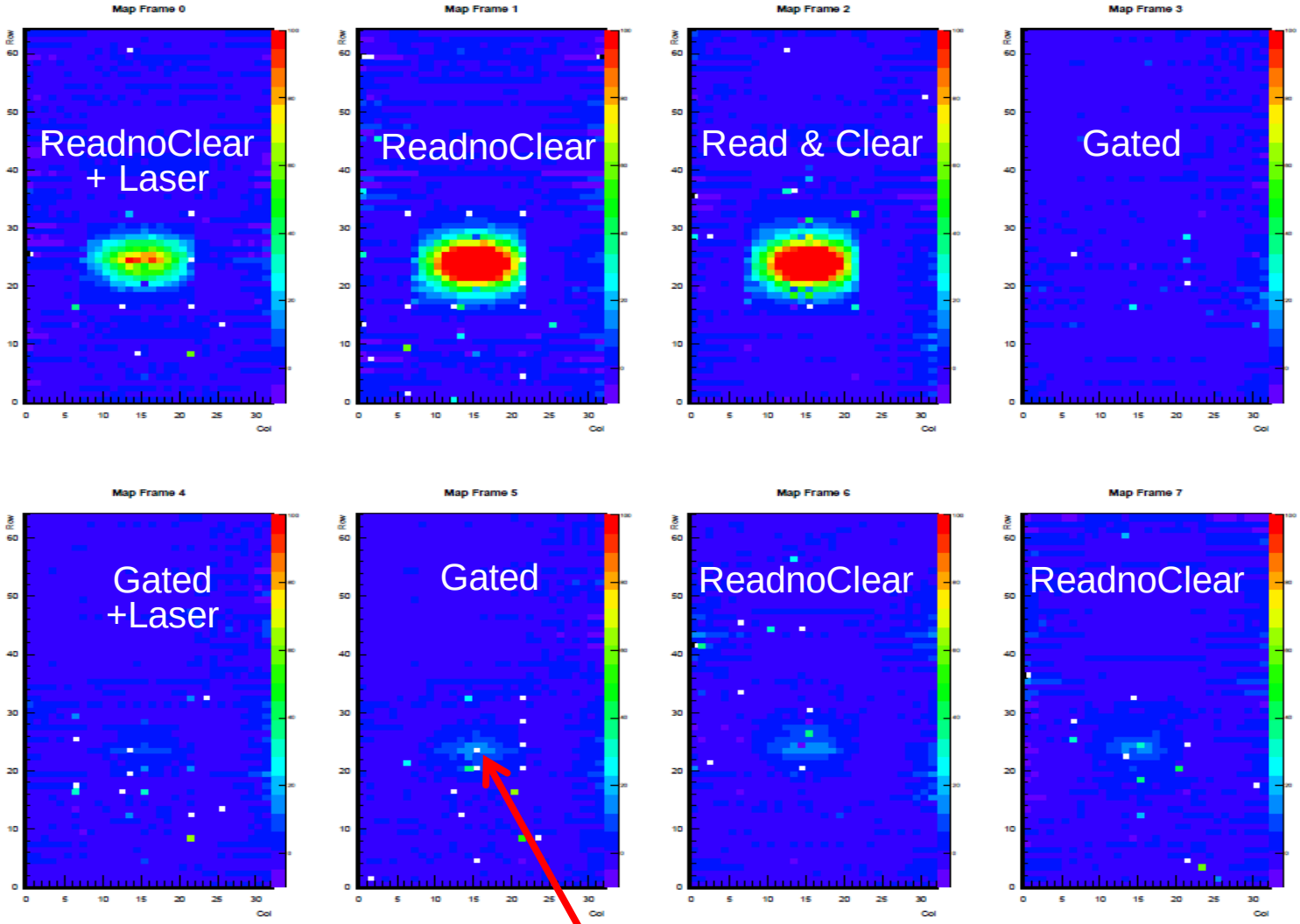
- Laser 400ns, 1V
- GateOff = 8V, Clear On = 18V

Experiment B: *Junk Charge Generation*

Frame n	Frame 0	Frame 1	Frame 2	Frame 3	Frame 4	Frame 5	Frame 6	Frame 7
Normal sequence	ReadnoClear + Laser	ReadnoClear	Read & Clear	Gated Mode	Gated Mode + Laser	Gated Mode	ReadnoClear	ReadnoClear



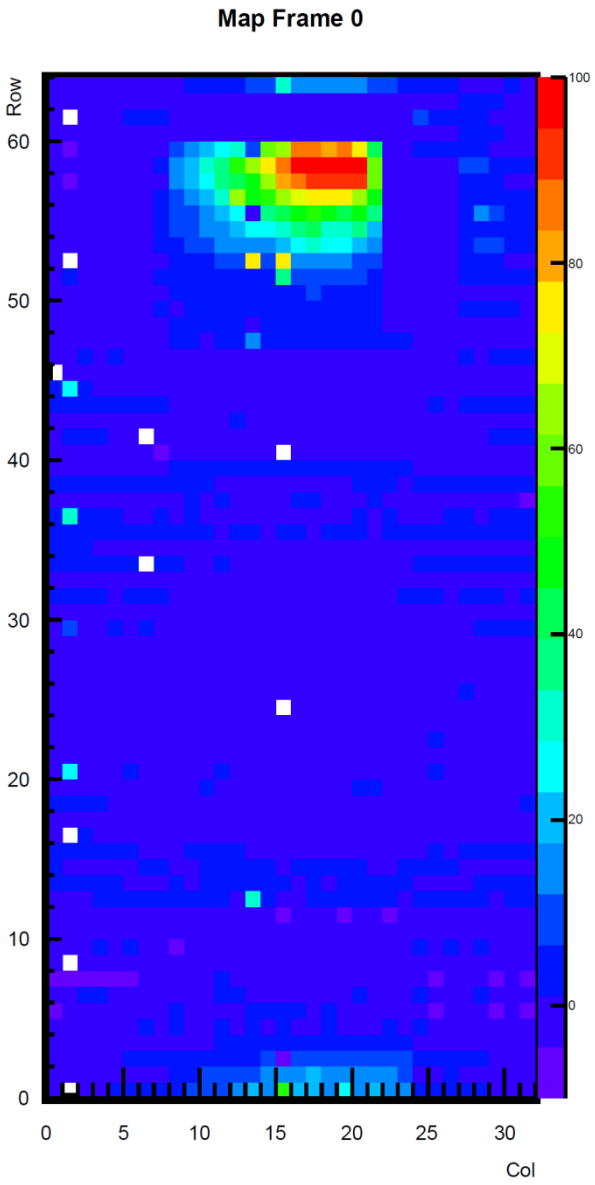
Gated Mode with RO – *Junk Charge Generation*

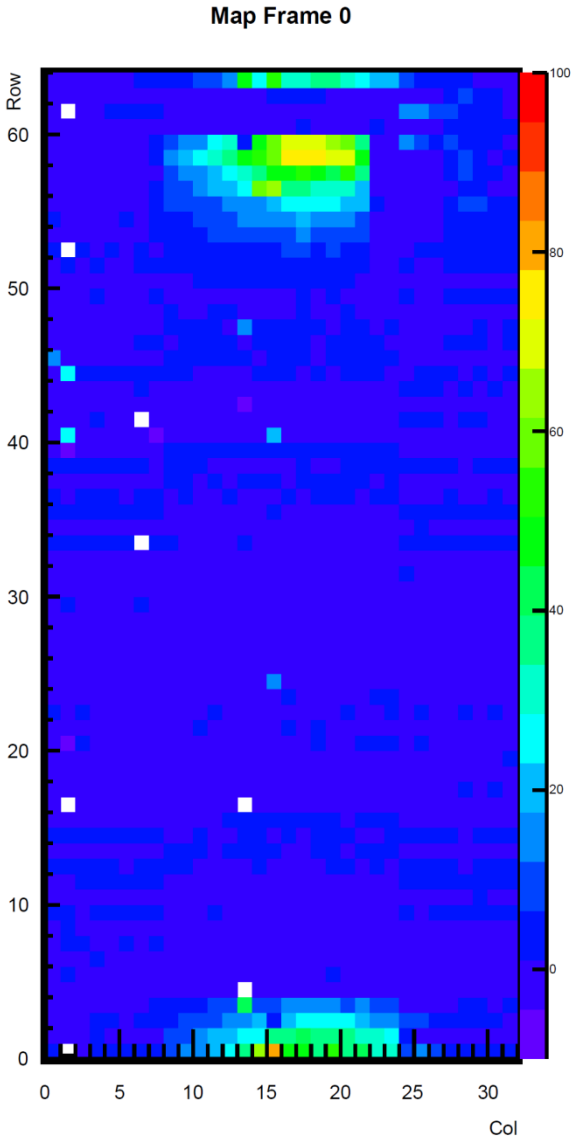


- Laser 1µs, 800mV

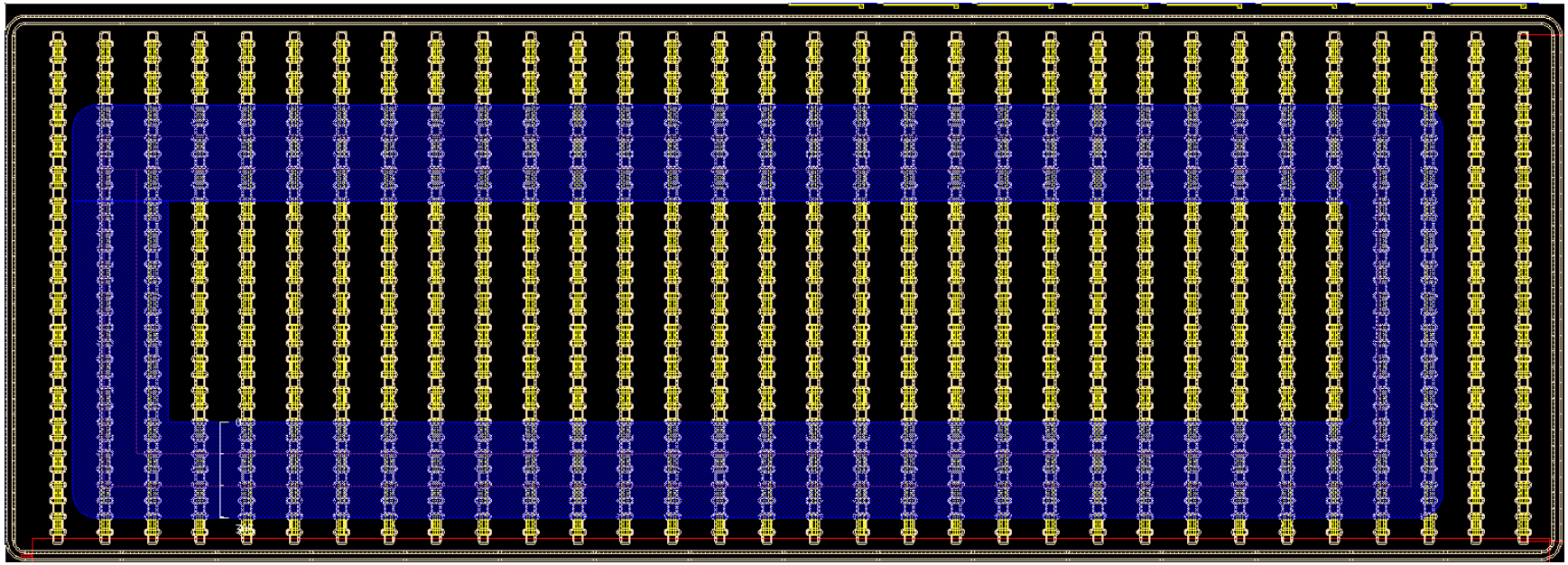
spot contours since rows sensitive for 100ns

Trouble in paradise…





Known Culprit – the Aluminium Ring ☑



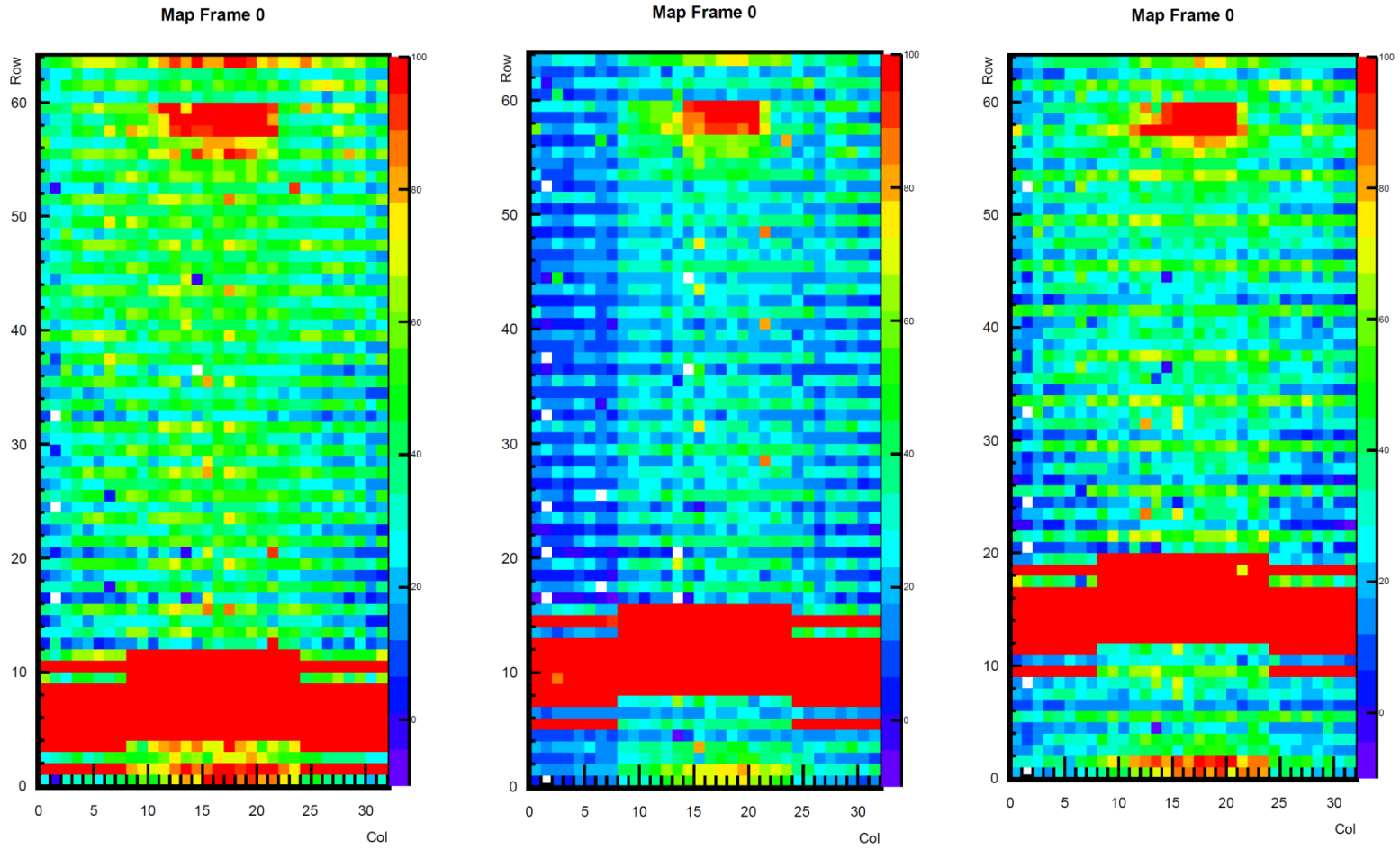
Maybe it‘s this one… but not implemented yet!

Extract from the DCD-Bv4-Pipeline Reference Manual:

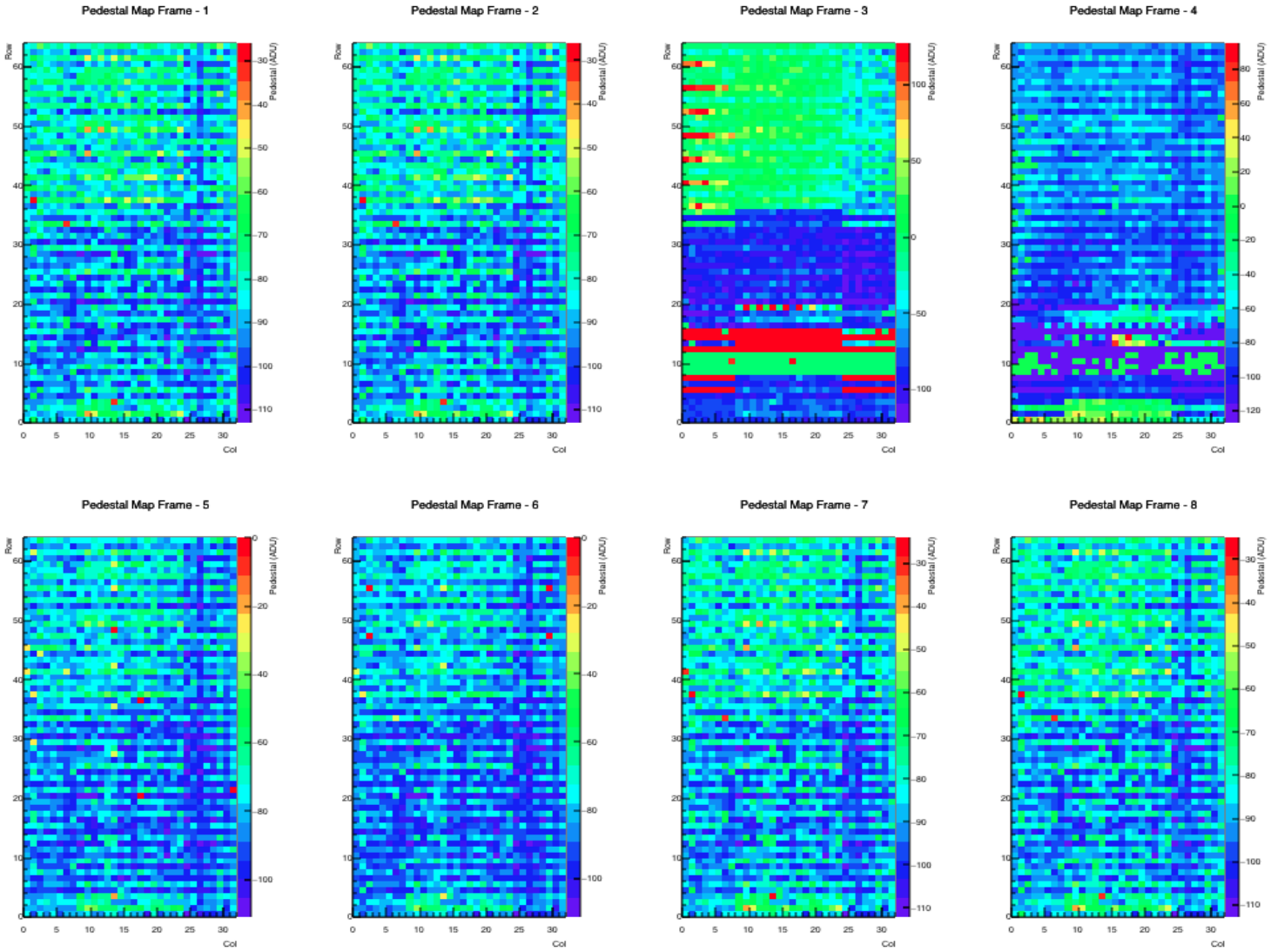
> “*Internally, the algorithmic ADCs start converting the input currents and the digital processing pipeline are filled with their output values.* ***191*** *clock cycles later (DCDv2:* ***171****), the first valid byte of data can be read at the DOX[7:0] bus.”*

…the difference translates to a delay of exact 80 columns

Are there some shorts between matrix rows?



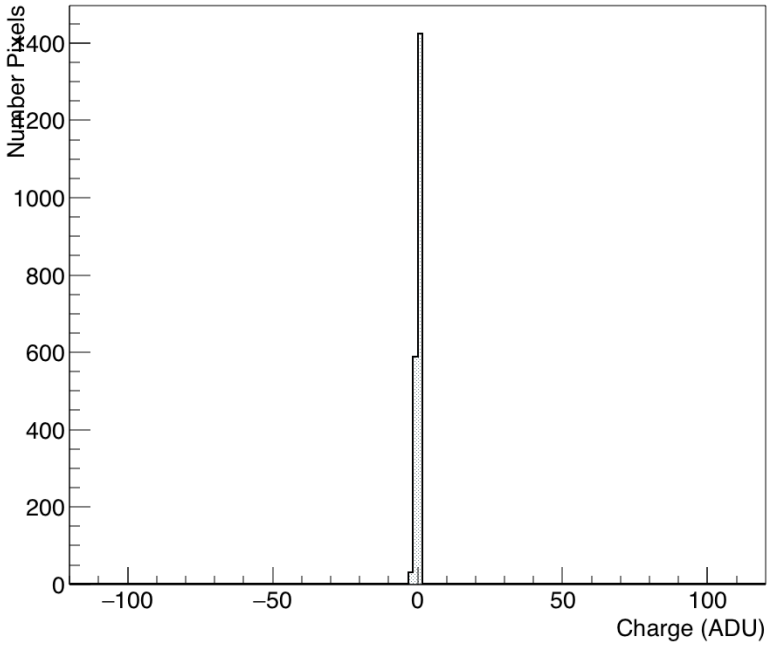
Gated Mode with Read Out – all Frames



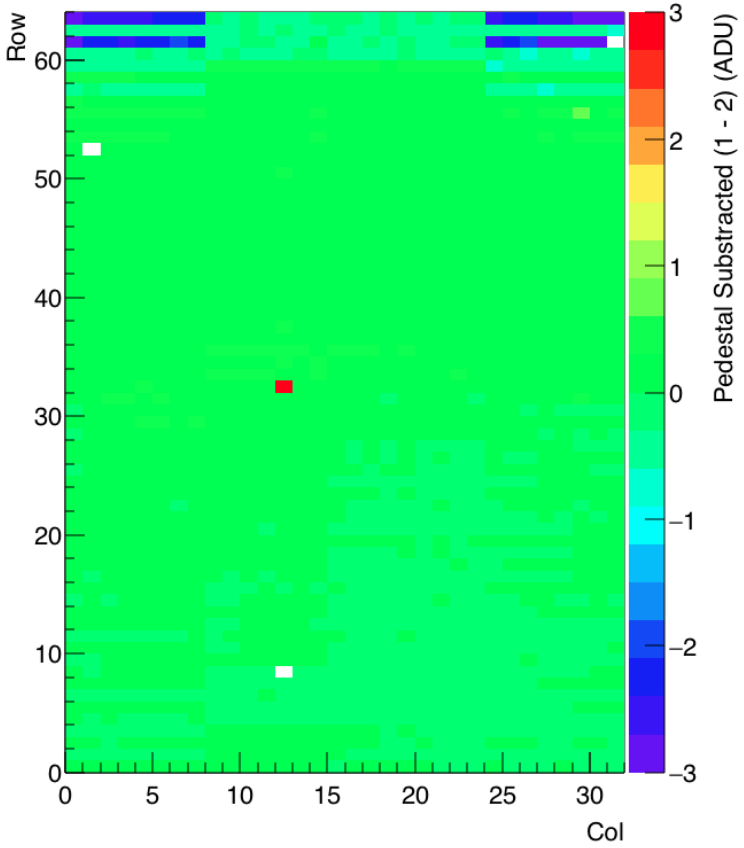
Gate Mode with RO 1600ns during frame 3, Gate Off = 3V, Clear On =18V

Subtraction Map Frame 1 – Frame 2

Subtracted Charge Distribution (1 – 2)

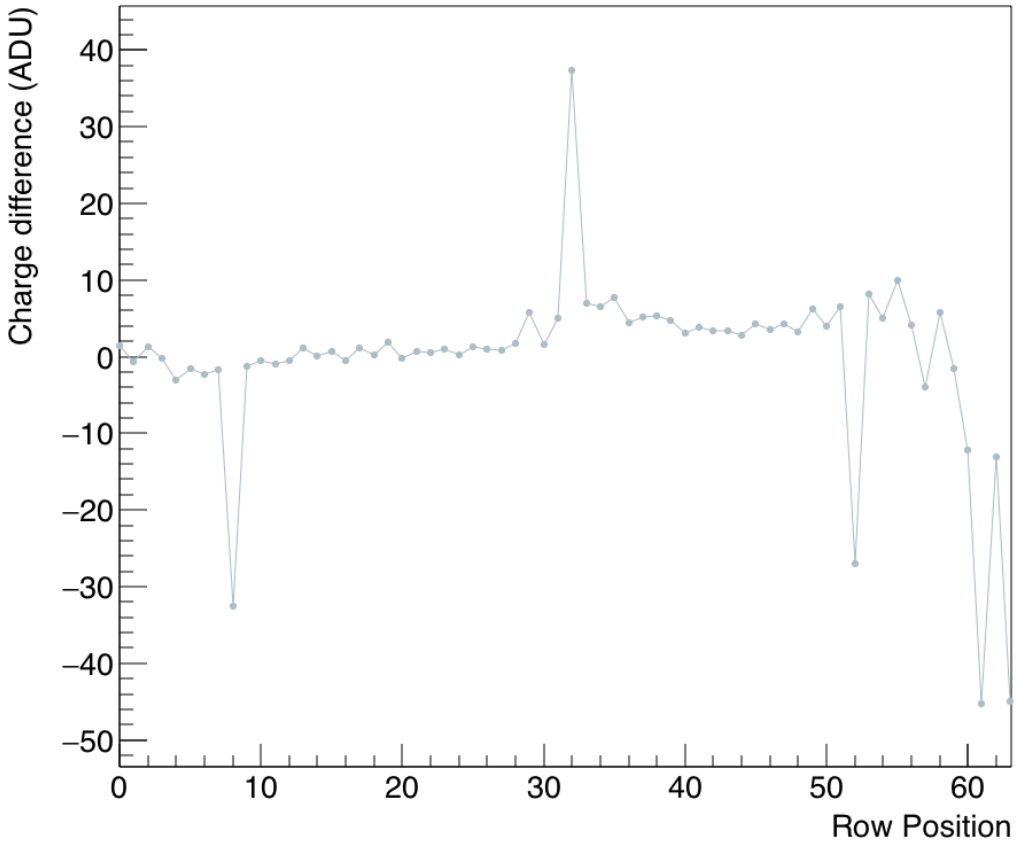


Pedestal subtraction Map (1 – 2)



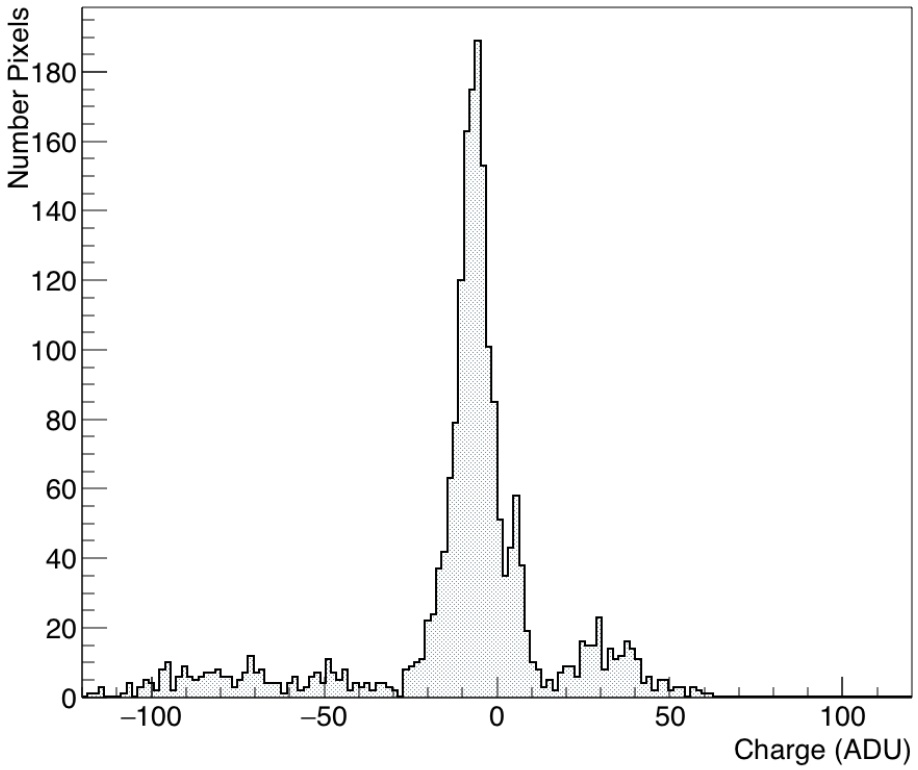
Subtract sum of rows of Frame 1 – Frame 2

Subtraction of charge in a full row (1 – 2)

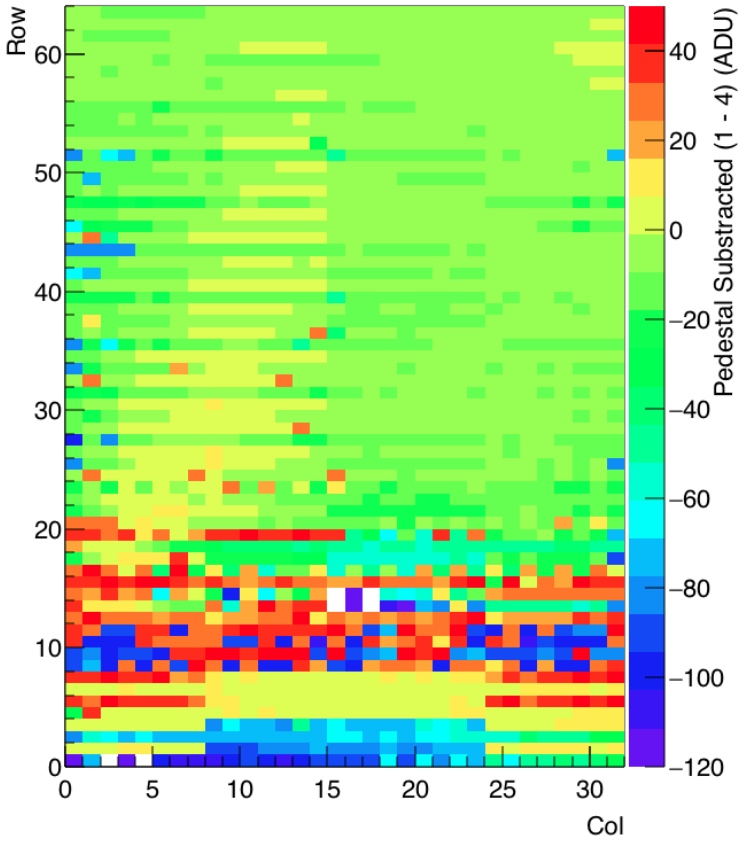


Subtracting Distribution Frame 1 – Frame 4

Pedestal subtraction Map (1 – 4)

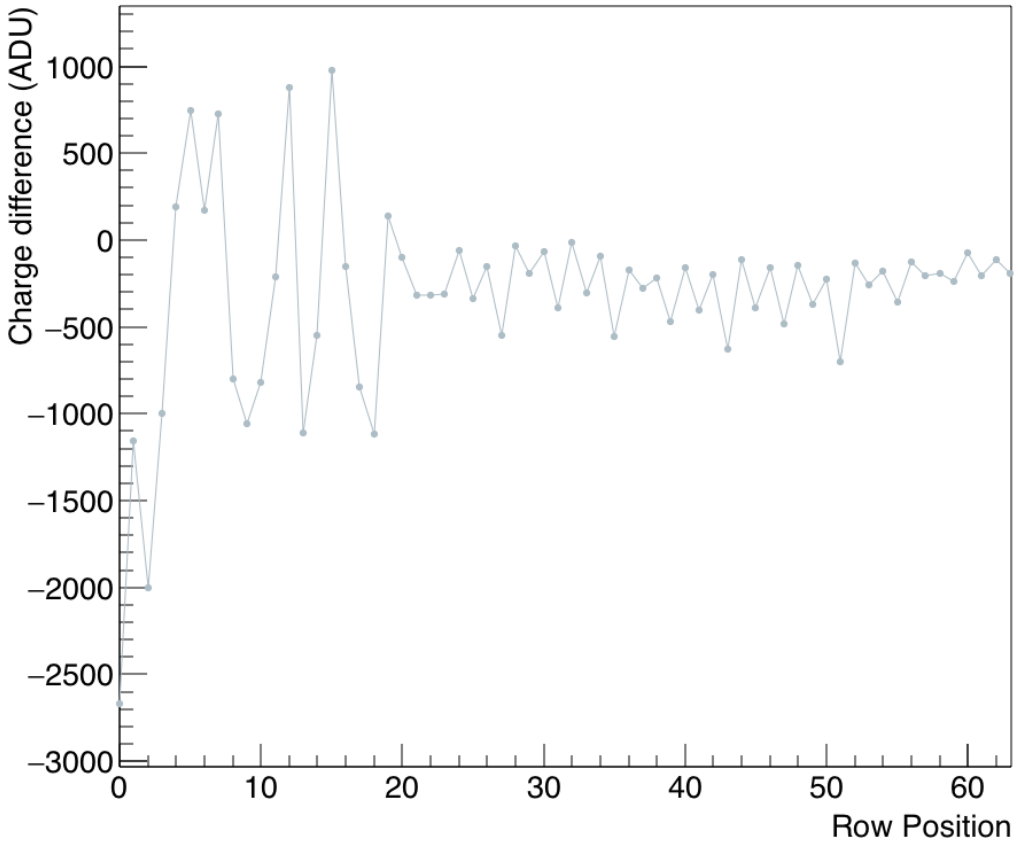


Pedestal subtraction Map (1 – 4)



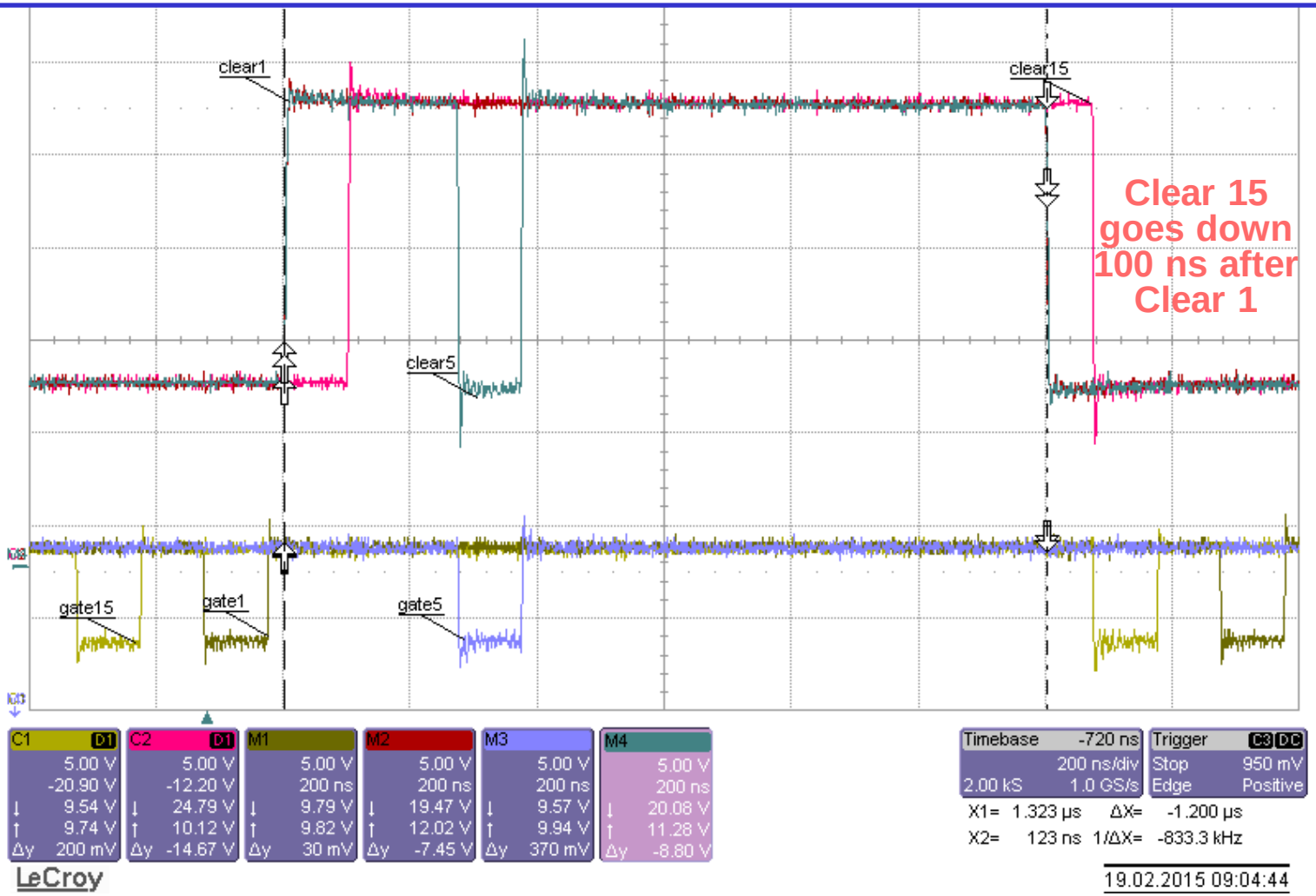
Subtract sum of rows of Frame 1 – Frame 4

Subtraction of charge in a full row (1 – 4)

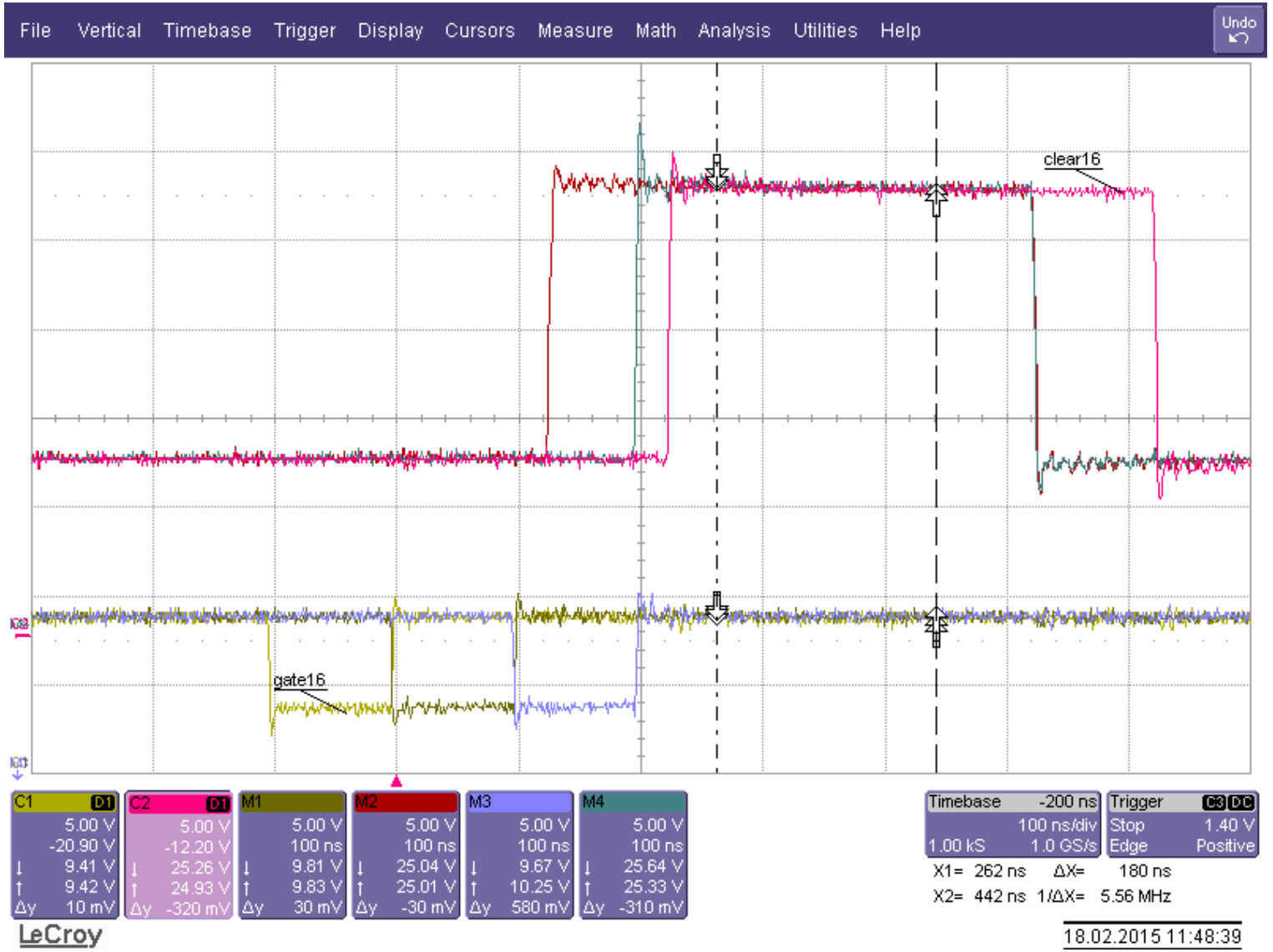


Gated Mode with RO – 1200ns

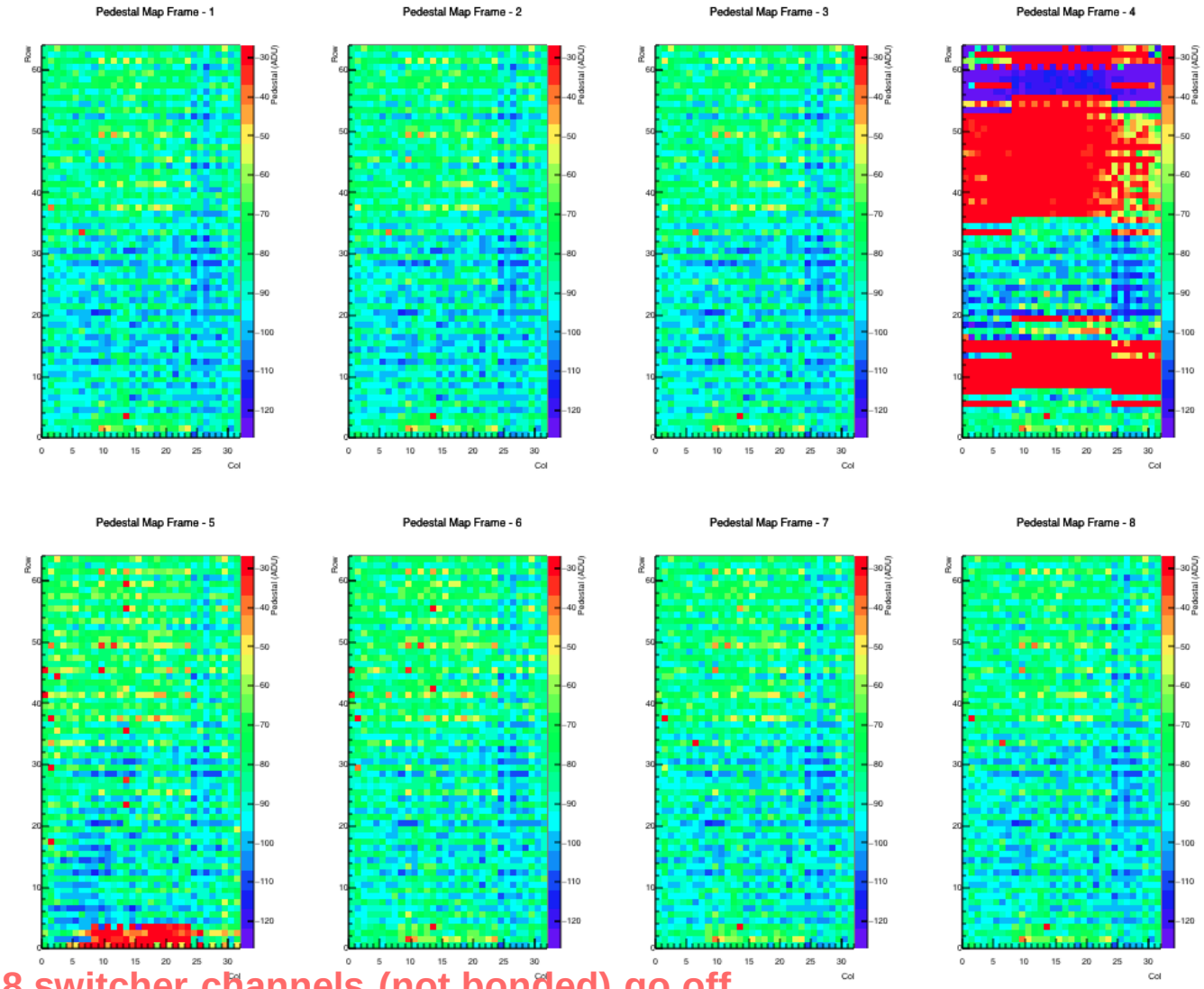
Gating of the first 8 switcher channels starts about 125ns after frame starts
FF0 → switches on BoostGated at falling edge of StrG (25ns)
FF1 → Gated Mode after next StrG (100ns)



Gated Mode with RO – 400ns



Gated Mode with RO 1200ns – all Frames



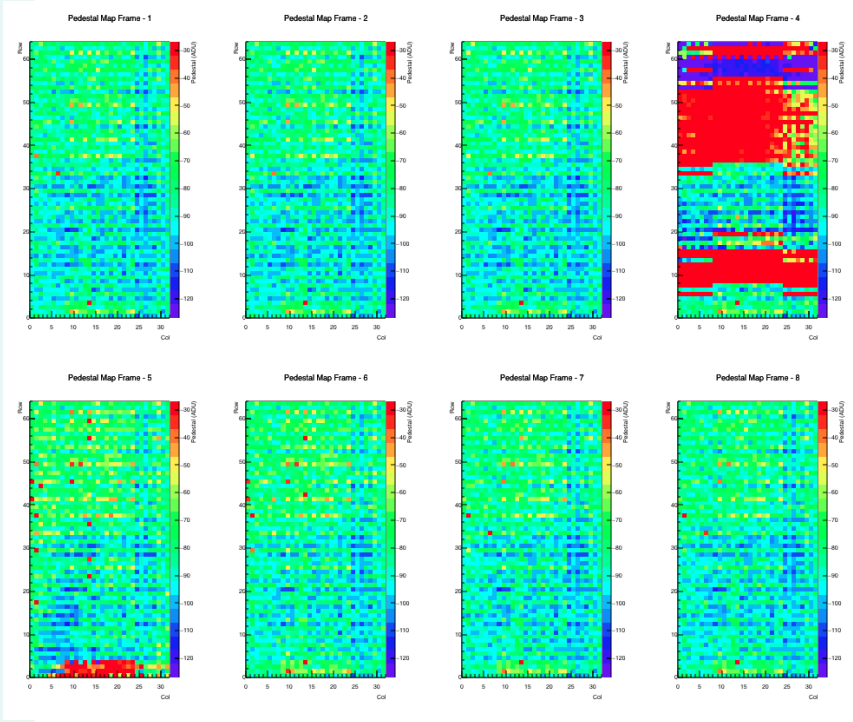
Last 8 switcher channels (not bonded) go off after 1625ns potentially distorting next frame?

Pedestals and Common Mode Correction

Three methods of pedestal and common mode correction:

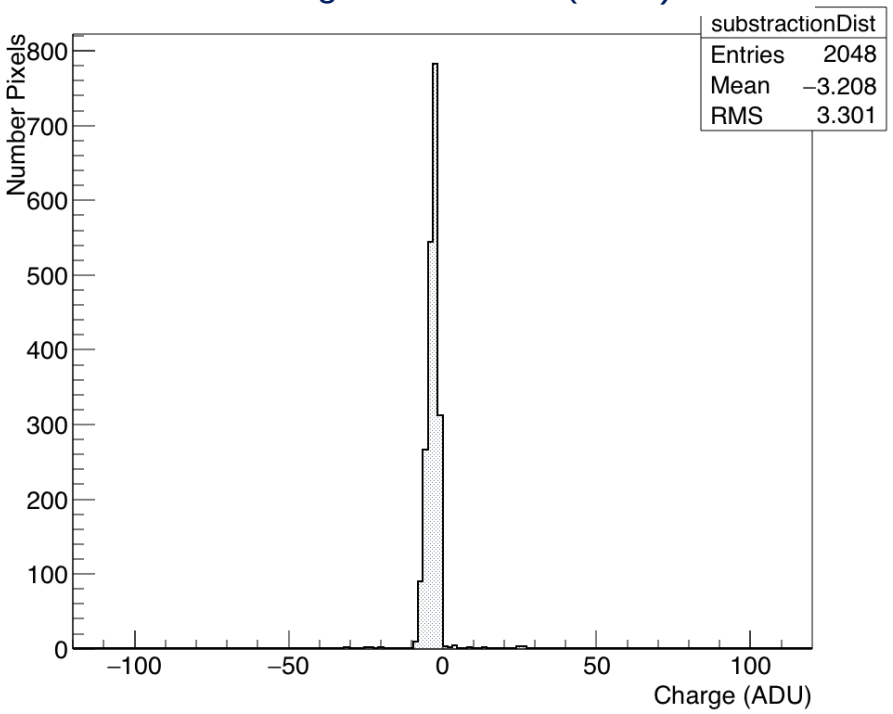
- Pedestal → offline CMC
- Offline CMC → Pedestal
- Analog CMC → Pedestal → offline CMC

Pedestal → offline CMC

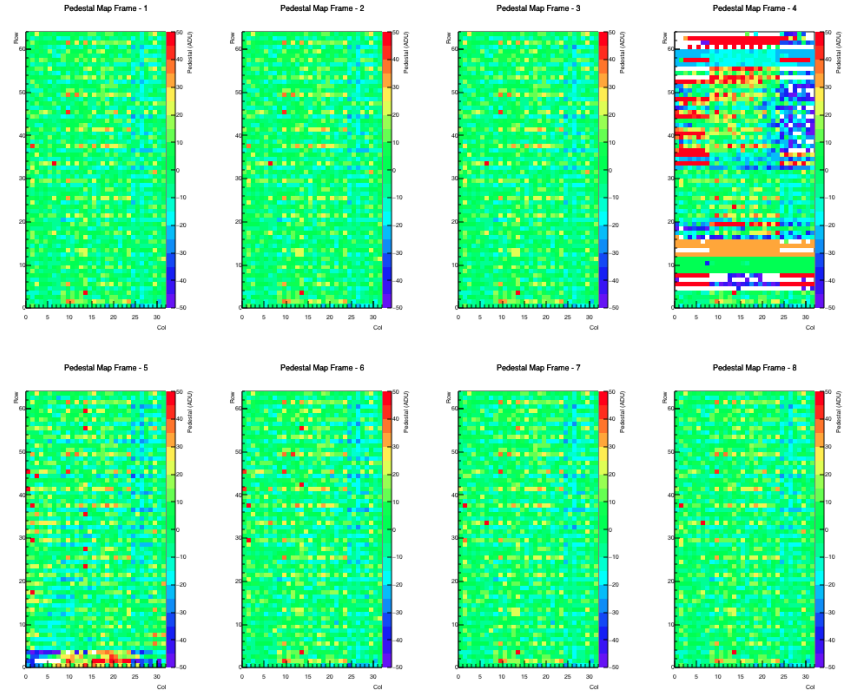


Gated Mode with RO – 1200ns

Subtracted Charge Distribution (1 – 6)

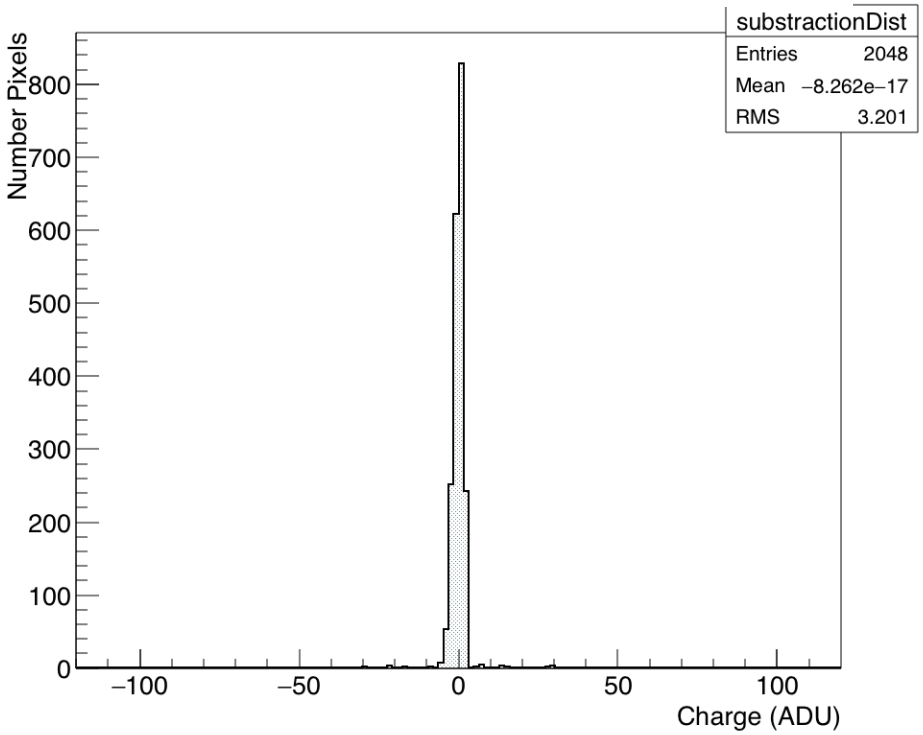


Offline CMC → Pedestals

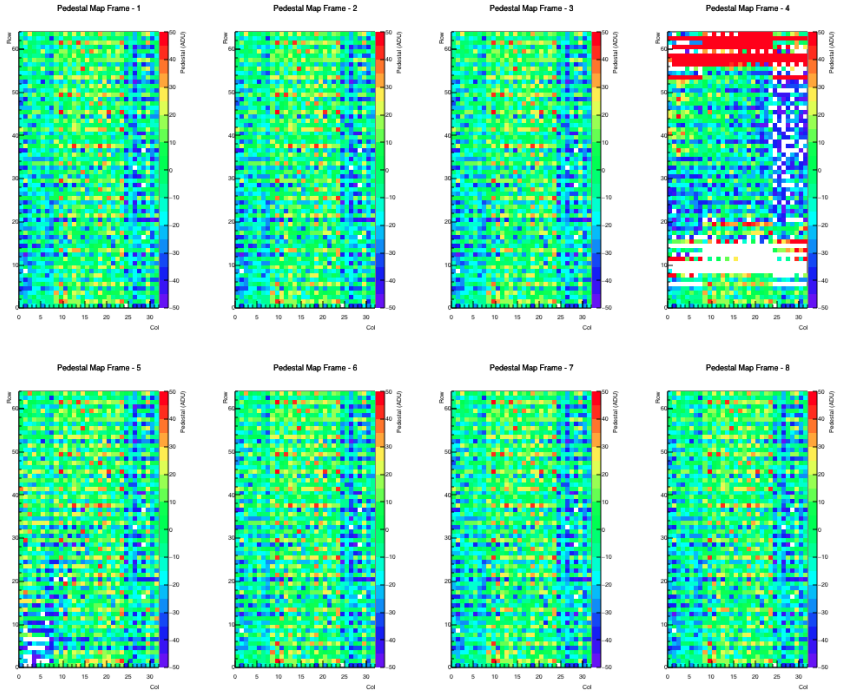


Gated Mode with RO – 1200ns

Subtracted Charge Distribution (1 – 6)

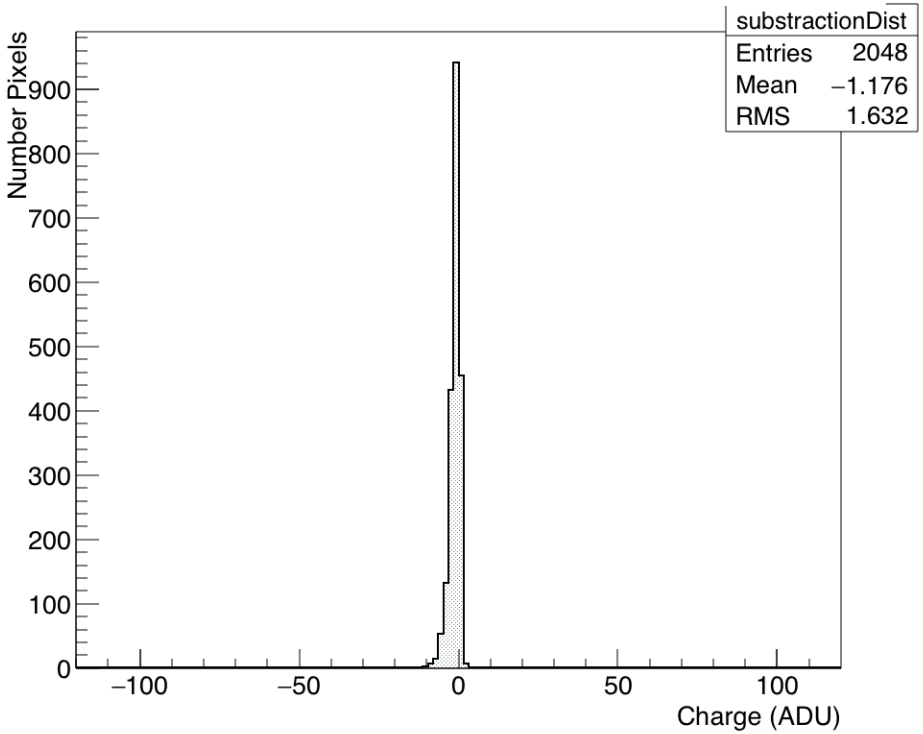


Analog CMC → Pedestal → offline CMC



Gated Mode with RO – 1200ns

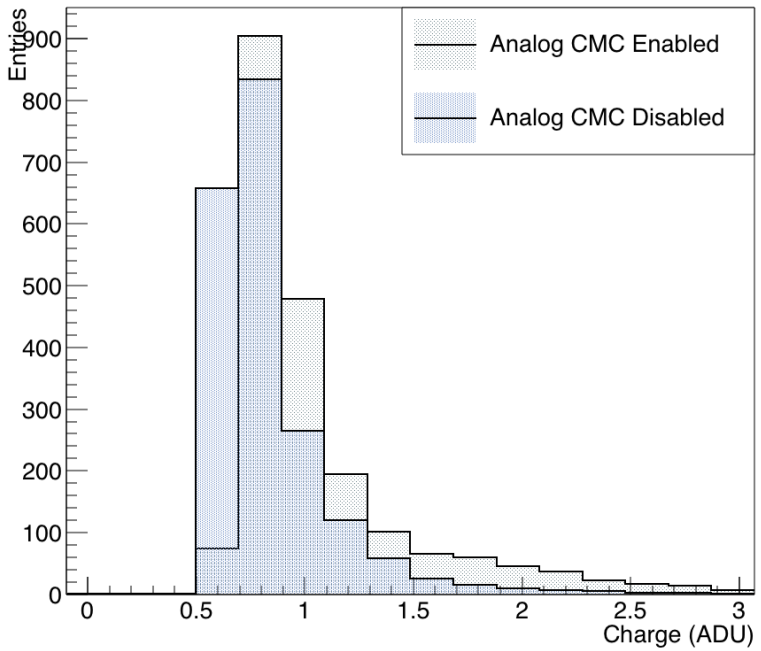
Subtracted Charge Distribution (1 – 6)



Analog Common Mode Correction in the DCDPP

- DCDPP provides an analog CMC which can be switched on and off by software
- Noise increases when analog CMC is on

Noise Distribution Comparison



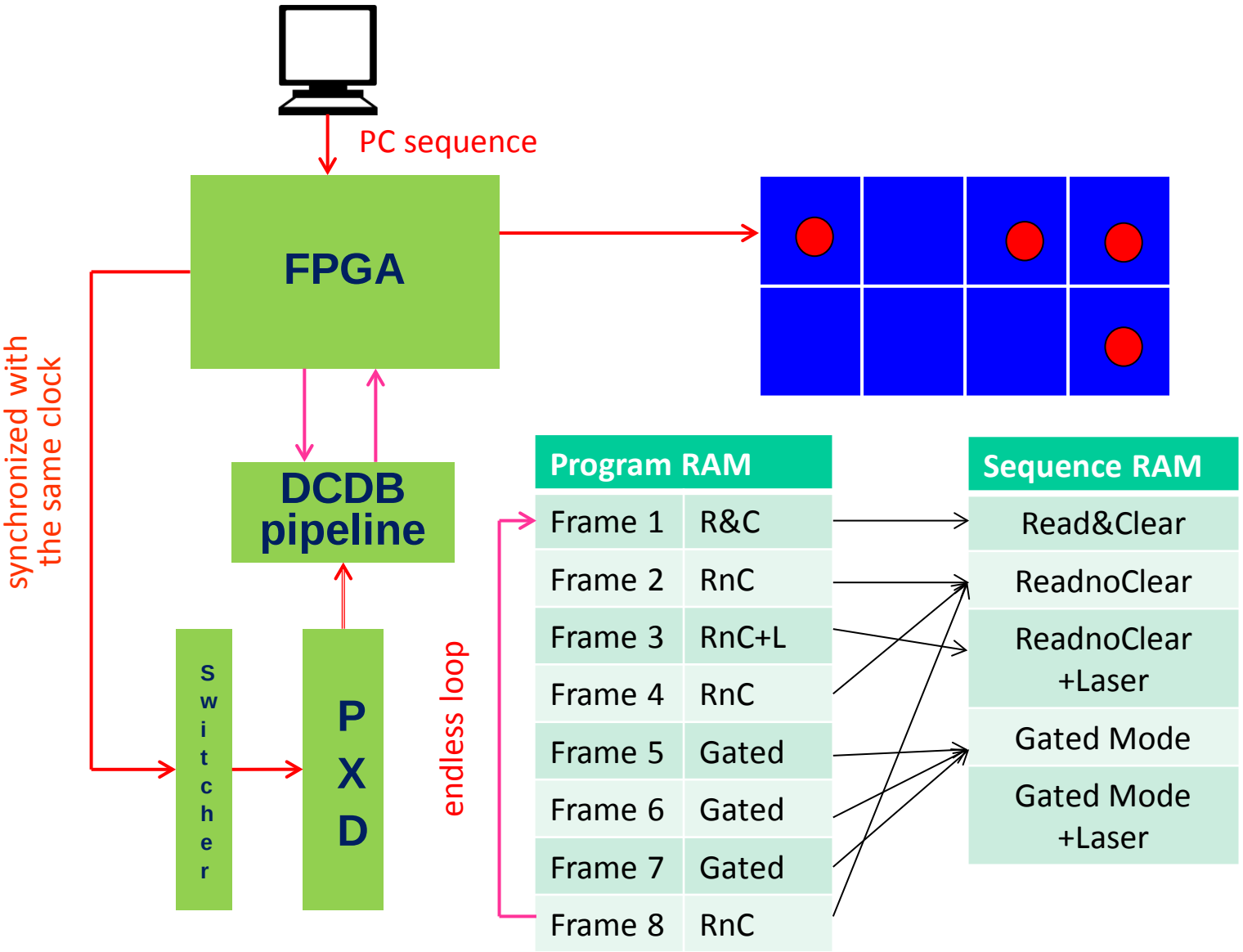
SUMMARY

- Gated mode can be applied with SWBv2 in a fast way (has to be confirmed for the capacitive load of a large matrix)
- Significant change of pedestals during the gated mode
  - For the gated mode with RO: how to handle data in DHPT?
- Analog CMC seems to improve the pedestal variation (on a small increase of noise)
  - Analog CMC is also important to correct for inhomogeneous irradiation along z

Thank you for your attention

Back-up Slides

Test Sequence



Test Sequences

Program RAM:
contains all information in which order different sequences have to be run through

→endless loop until stop

16-bit program code	Address	Sequence
0000000010000000	128	Read & Clear
0000000100000000	256	Read no Clear
0000000110000000	384	Read no Clear + Laser
0000000100000000	256	Read no Clear
0000001000000000	512	Gated Mode
0000001000000000	512	Gated Mode
0000001000000000	512	Gated Mode
0000000100000000	256	Read no Clear

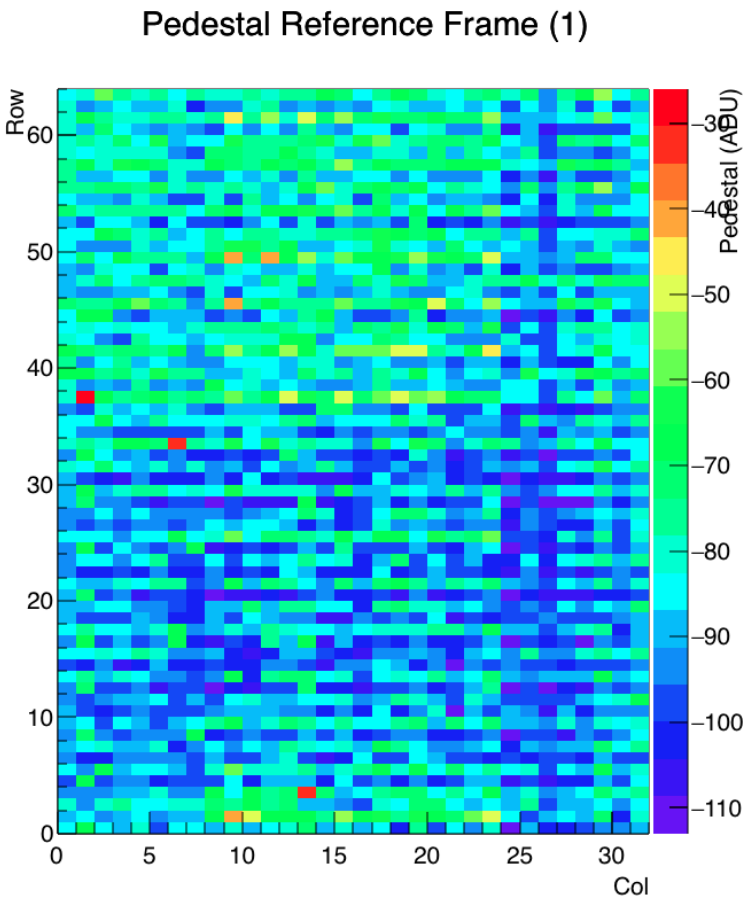
#4:trigger,#3:StrC,
#2: StrG,#1:Clk

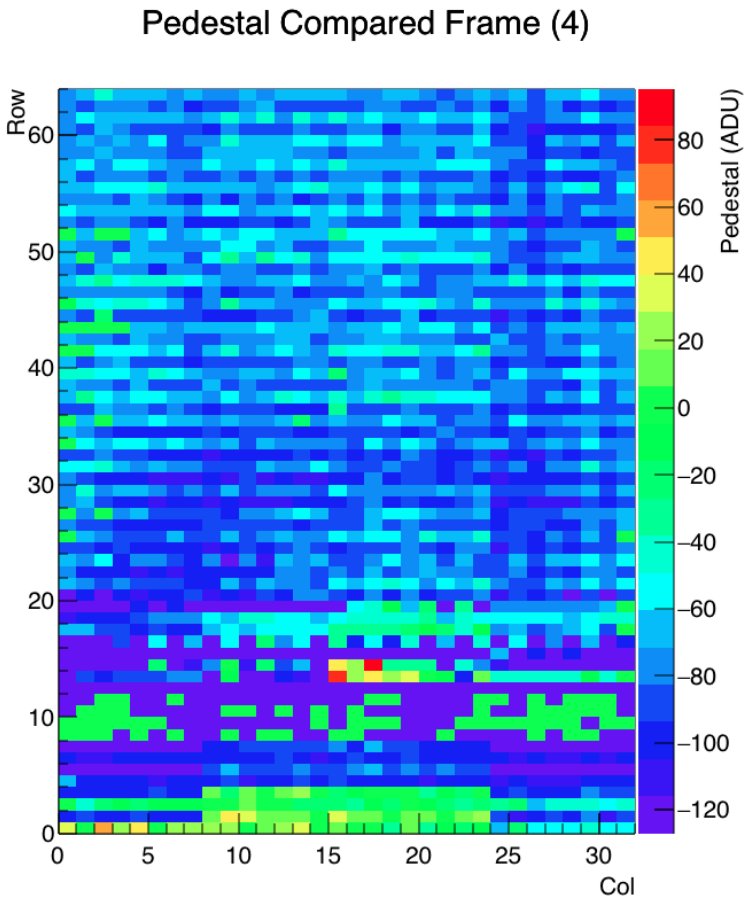
0,0,1,0
0,0,1,0
0,0,1,0
0,0,1,0
0,0,1,0
0,0,1,0
0,0,0,0
0,0,0,0
0,0,0,0
0,0,0,0
0,0,0,0
0,0,0,0
⋮

Sequence RAM:
contains all Trigger, Clk, StrG & StrC information for the whole sequence in binary format

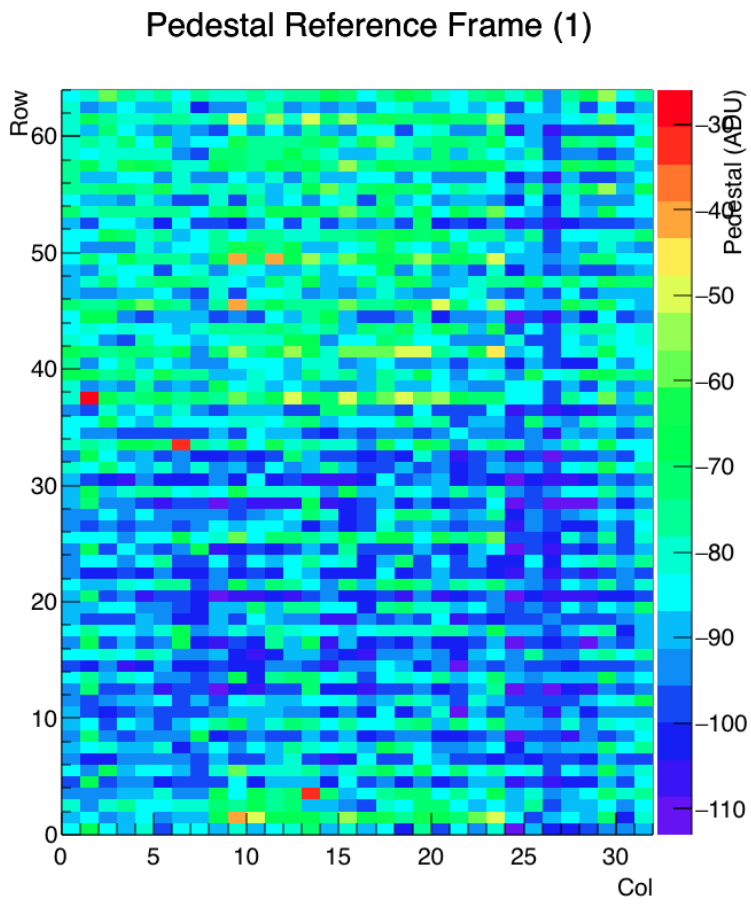
- FPGA sequentially reads binary code and translates it into microcode
- same clock as for DCDB pipeline
- extra start-up sequence resets SwitcherB & prohibits DCDB RO during this time

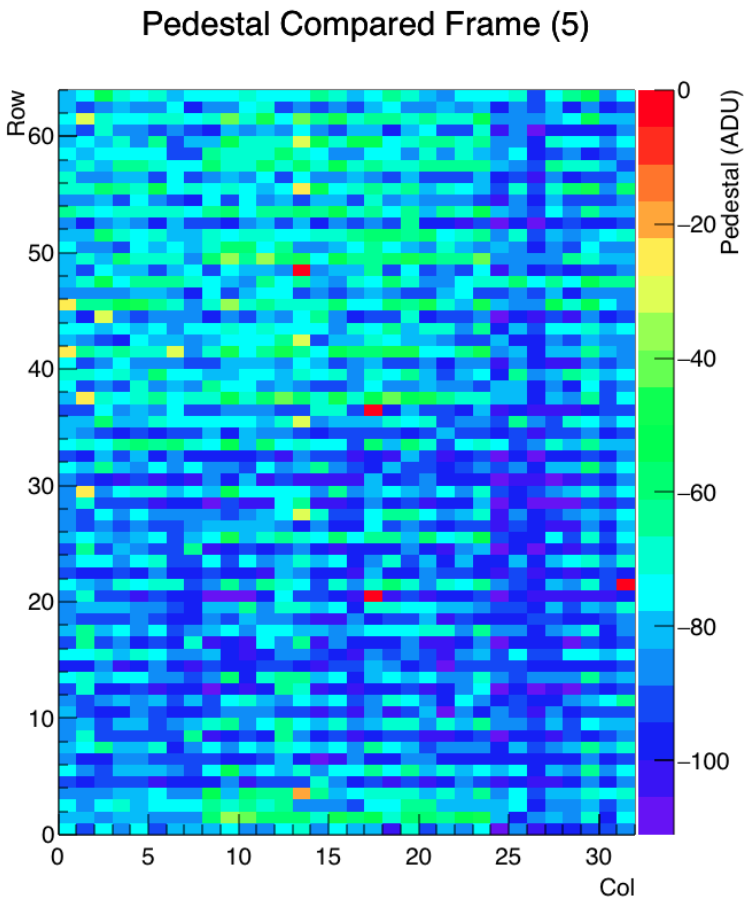
Comparison Pedestal Map R&C - Gated





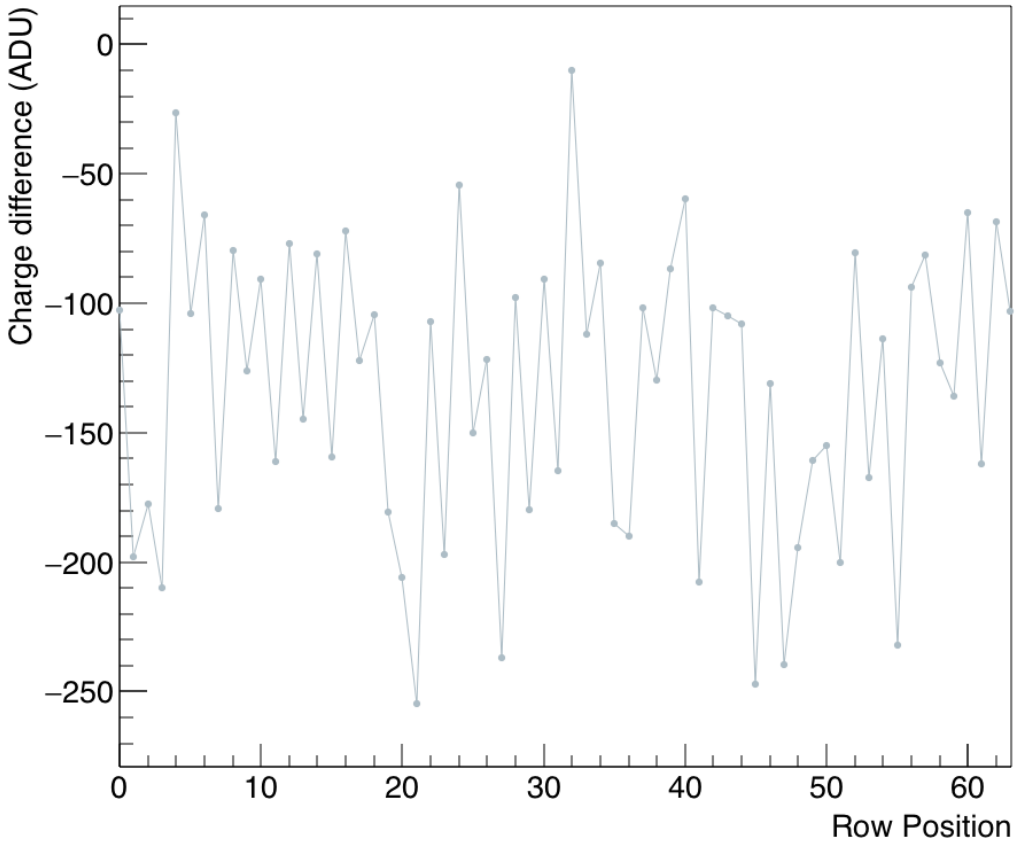
Comparison of Pedestal Map with normal mode after Gating (Frame 1 vs Frame 5)





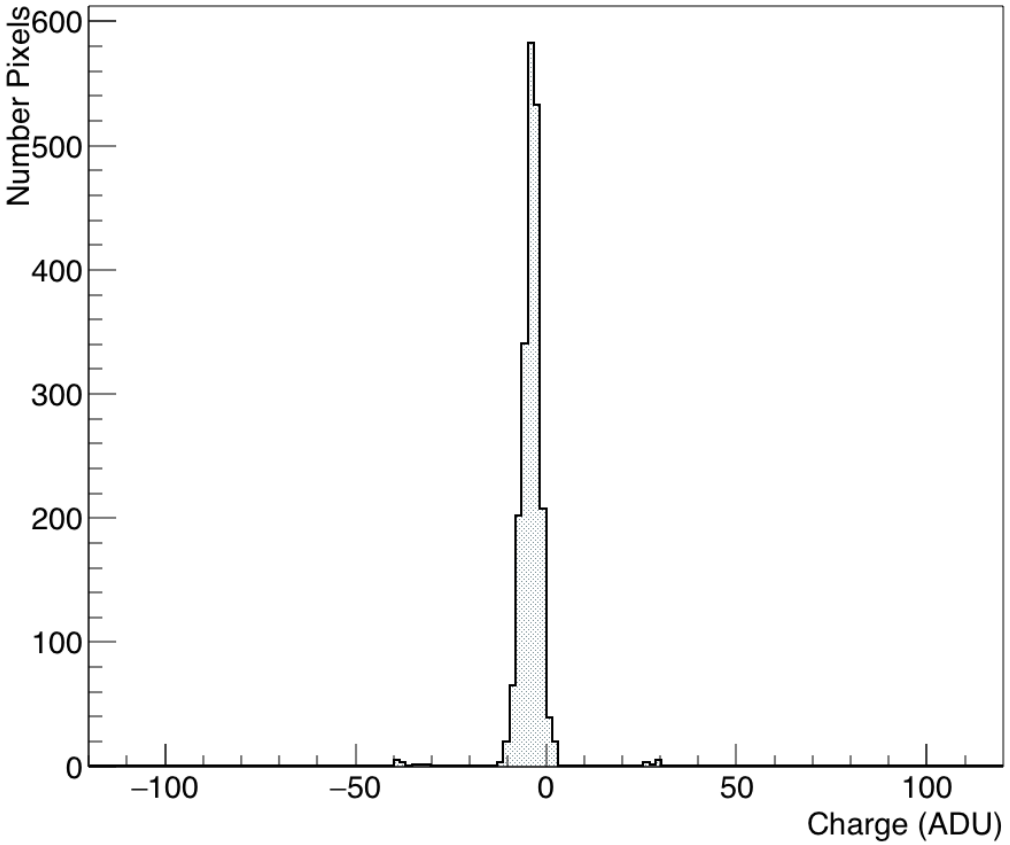
Subtract sum of rows of Frame 1 – Frame 5

Subtraction of charge in a full row (1 – 5)

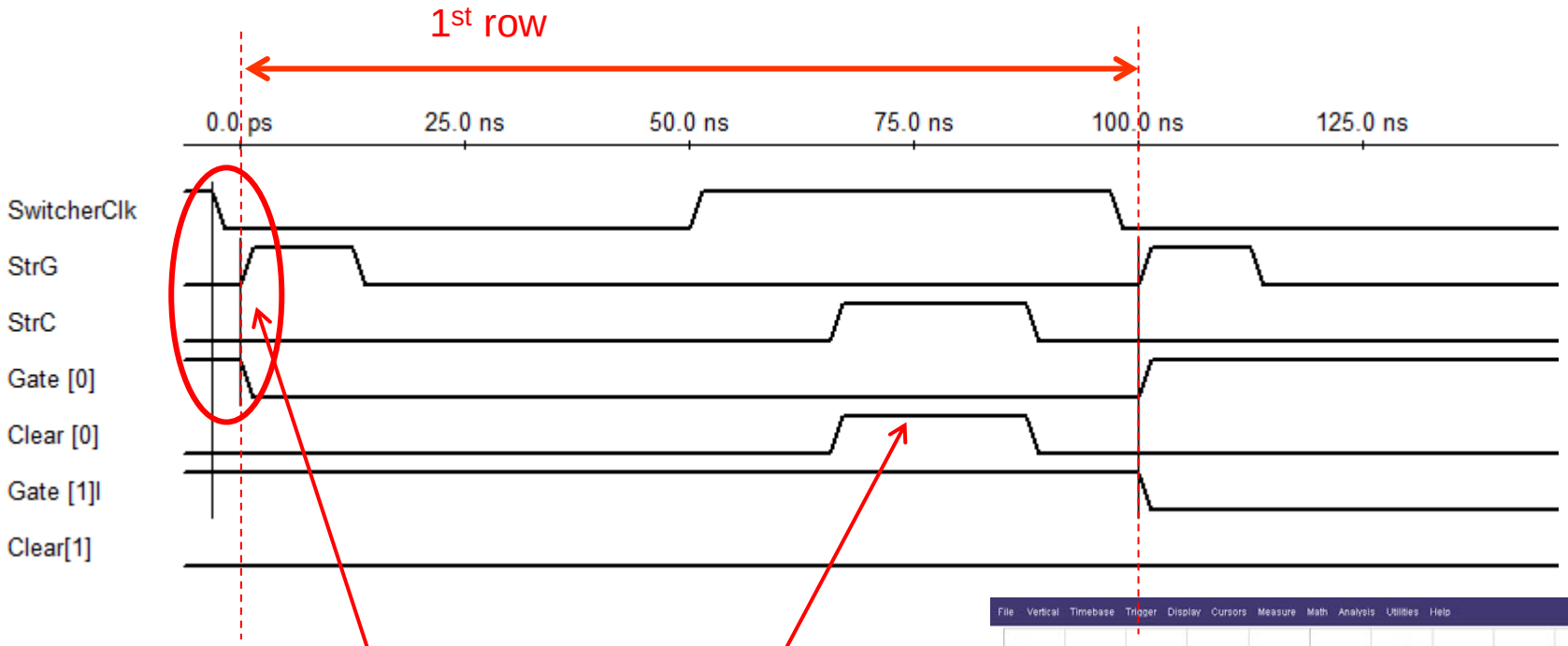


Subtracting Distribution Frame 1 – Frame 5

Pedestal subtraction Map (1-5)



Normal Operation

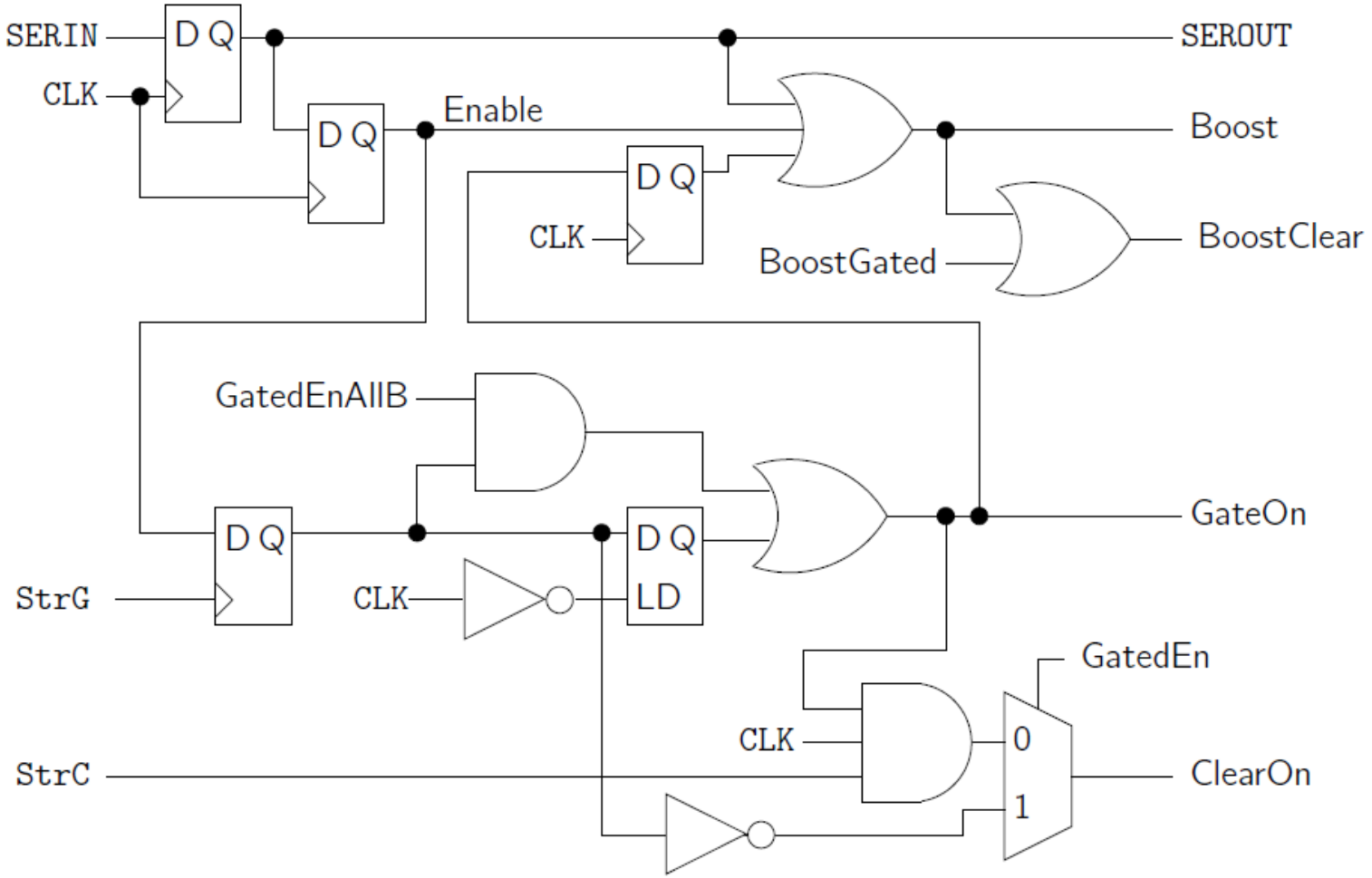


for gate activation rising edge of StrG has to be after falling edge of SwitcherClk

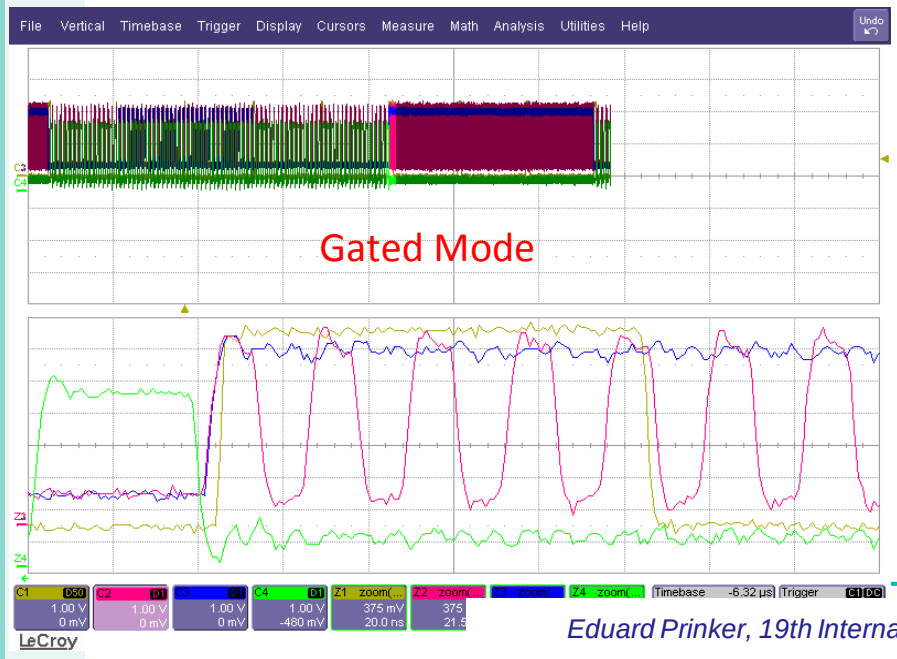
clear pulse is only working when gate is switched on

PMOS-gate on low = active

SwitcherB strobe logic of one channel

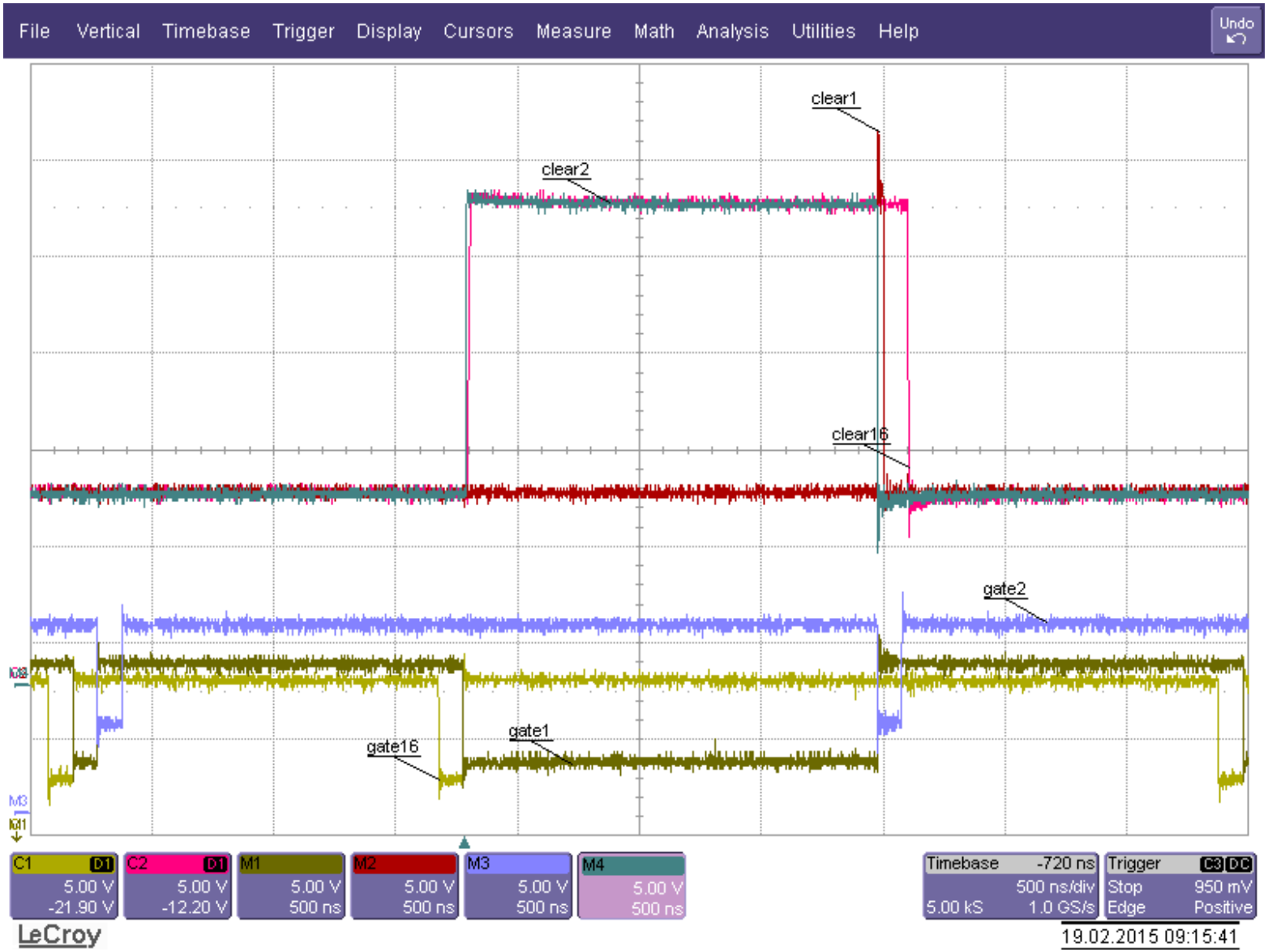


Gated mode without read-out: Switcher input

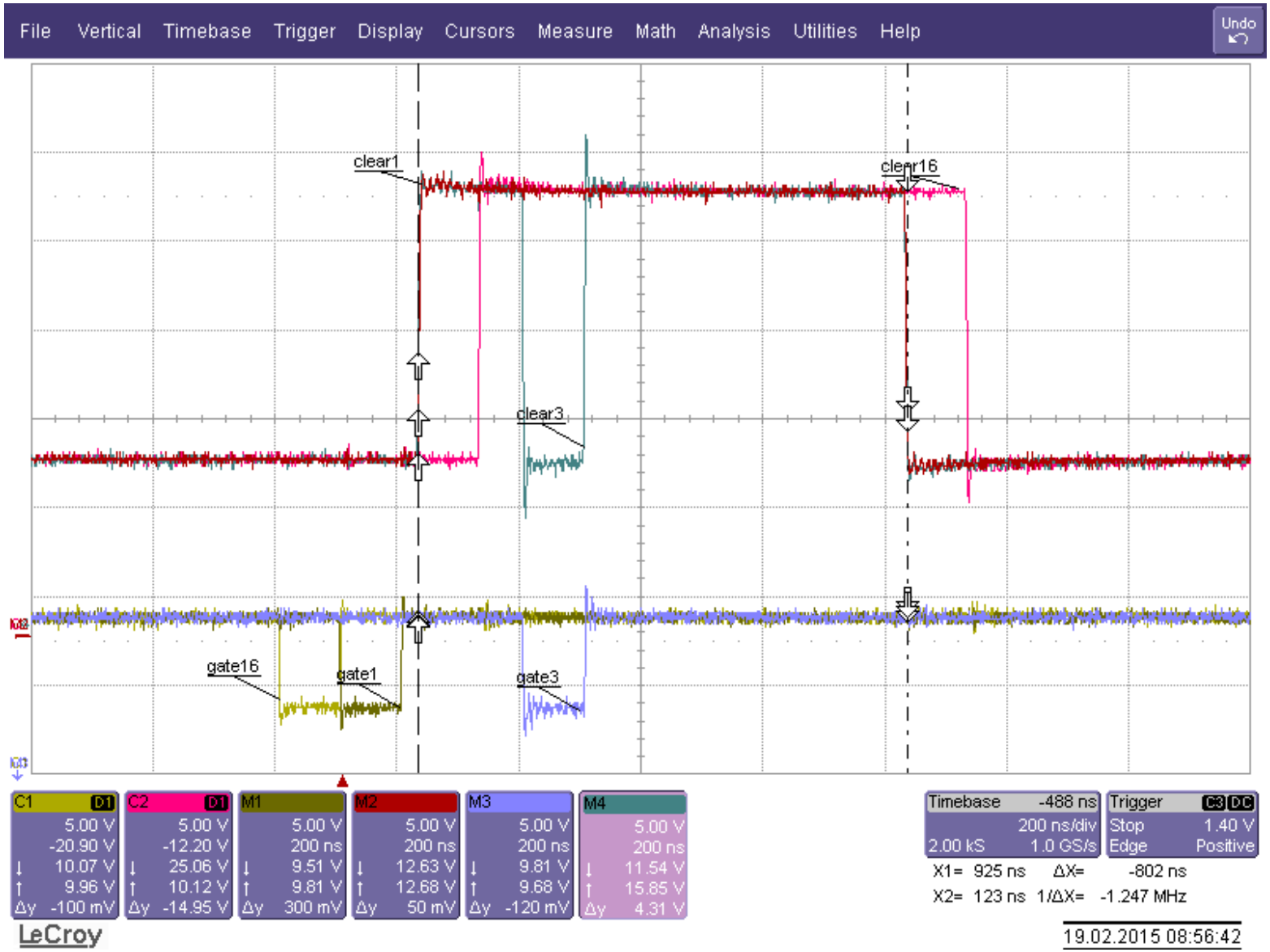


clk
StrC
StrG
Trigger

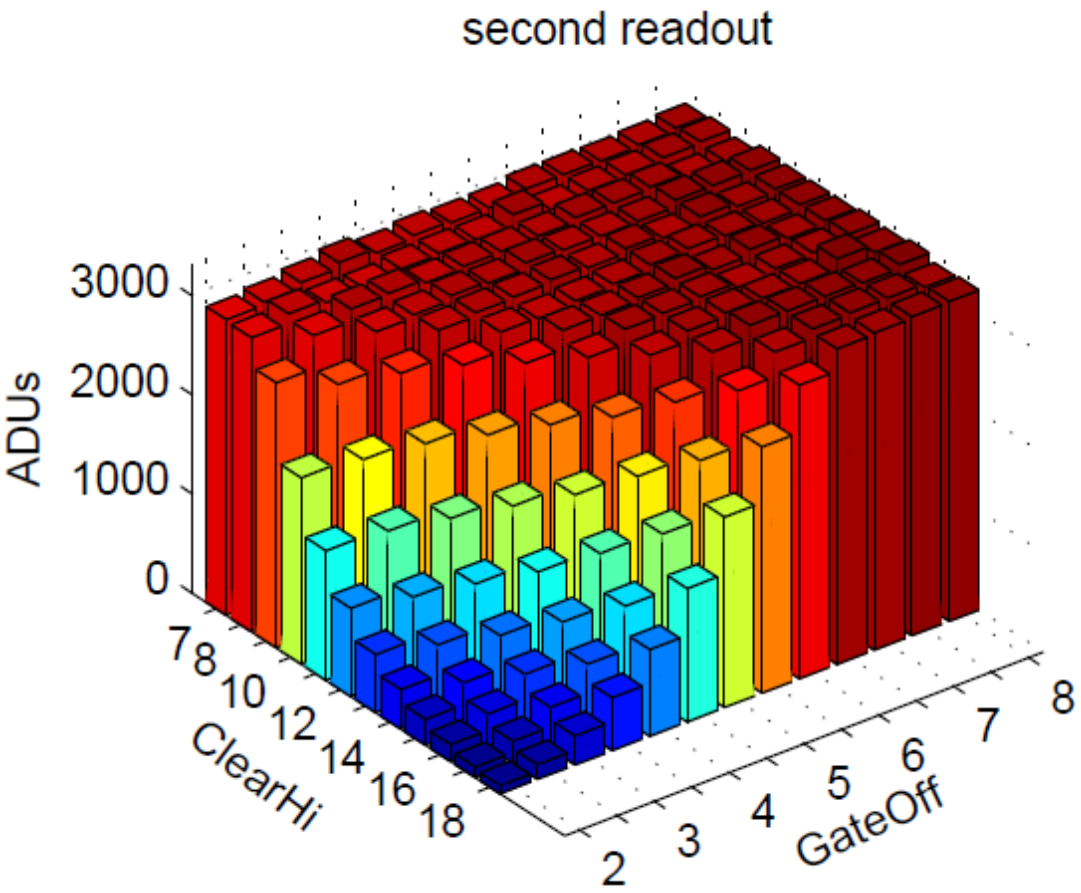
Gated mode without read-out: Switcher output



Gated mode with read-out: Switcher output



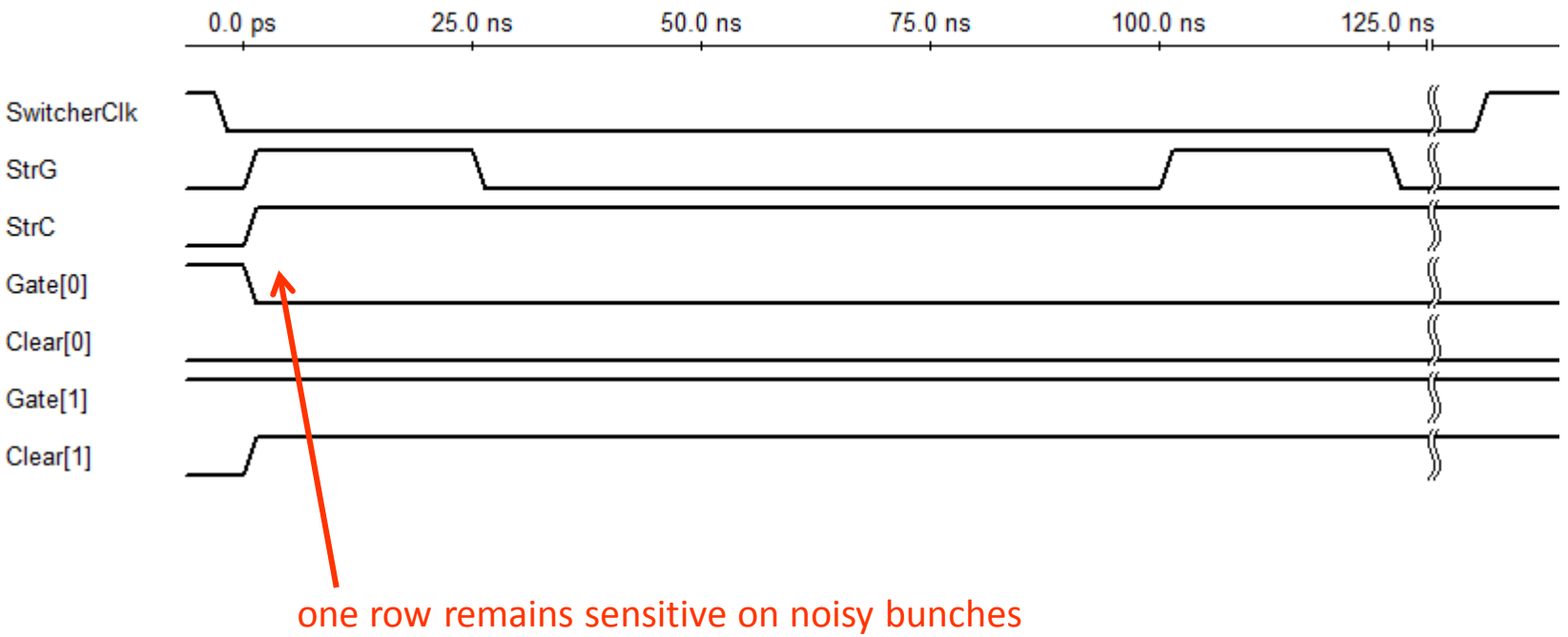
Signal Loss during Gated Mode



- Charge loss depends on the Clear On and Gate Off voltage
- For Gate Off > 5V there is no charge loss

Measurements by Felix Müller / Master Thesis

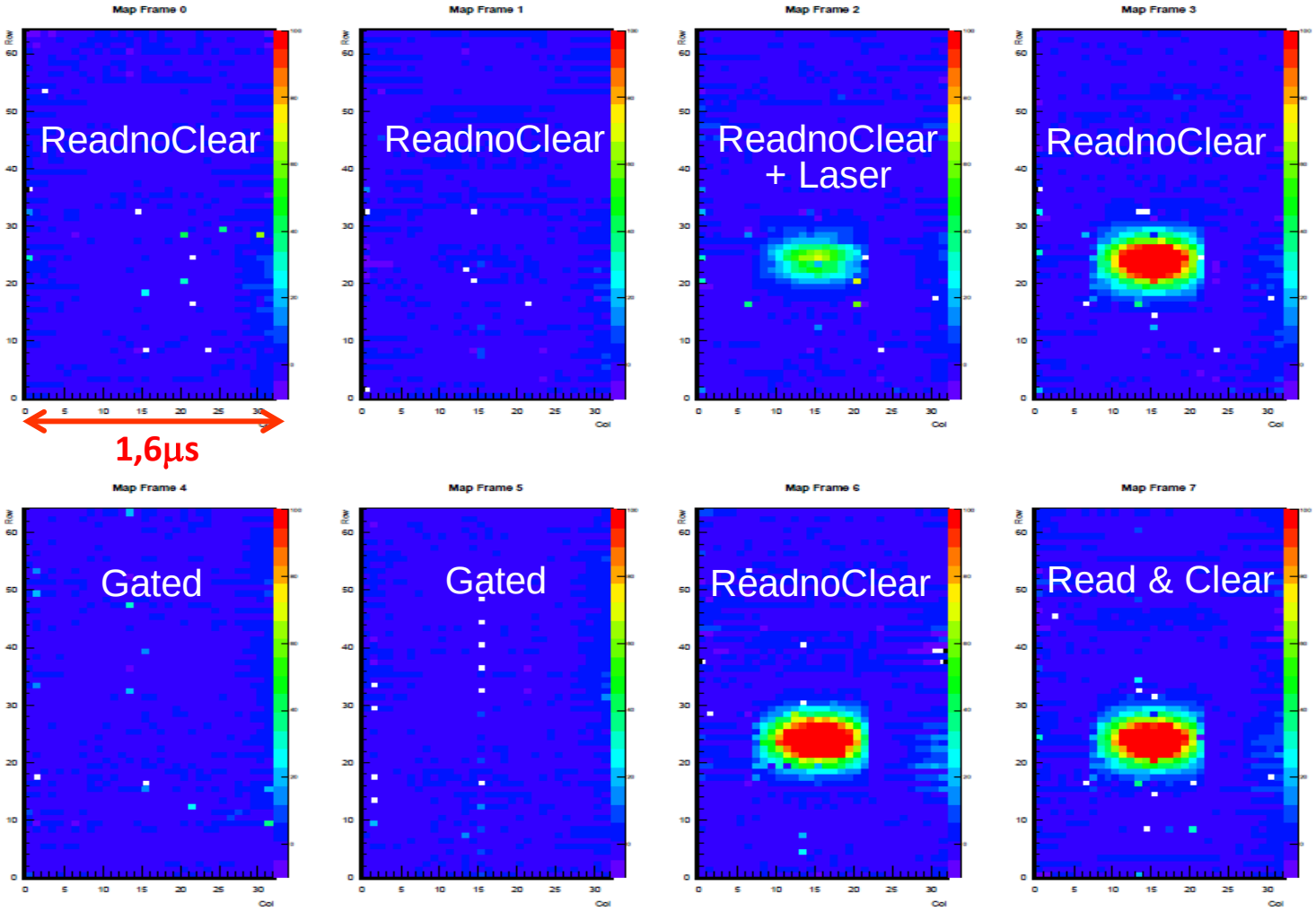
Gated mode without read-out



Enabling Gated Mode:

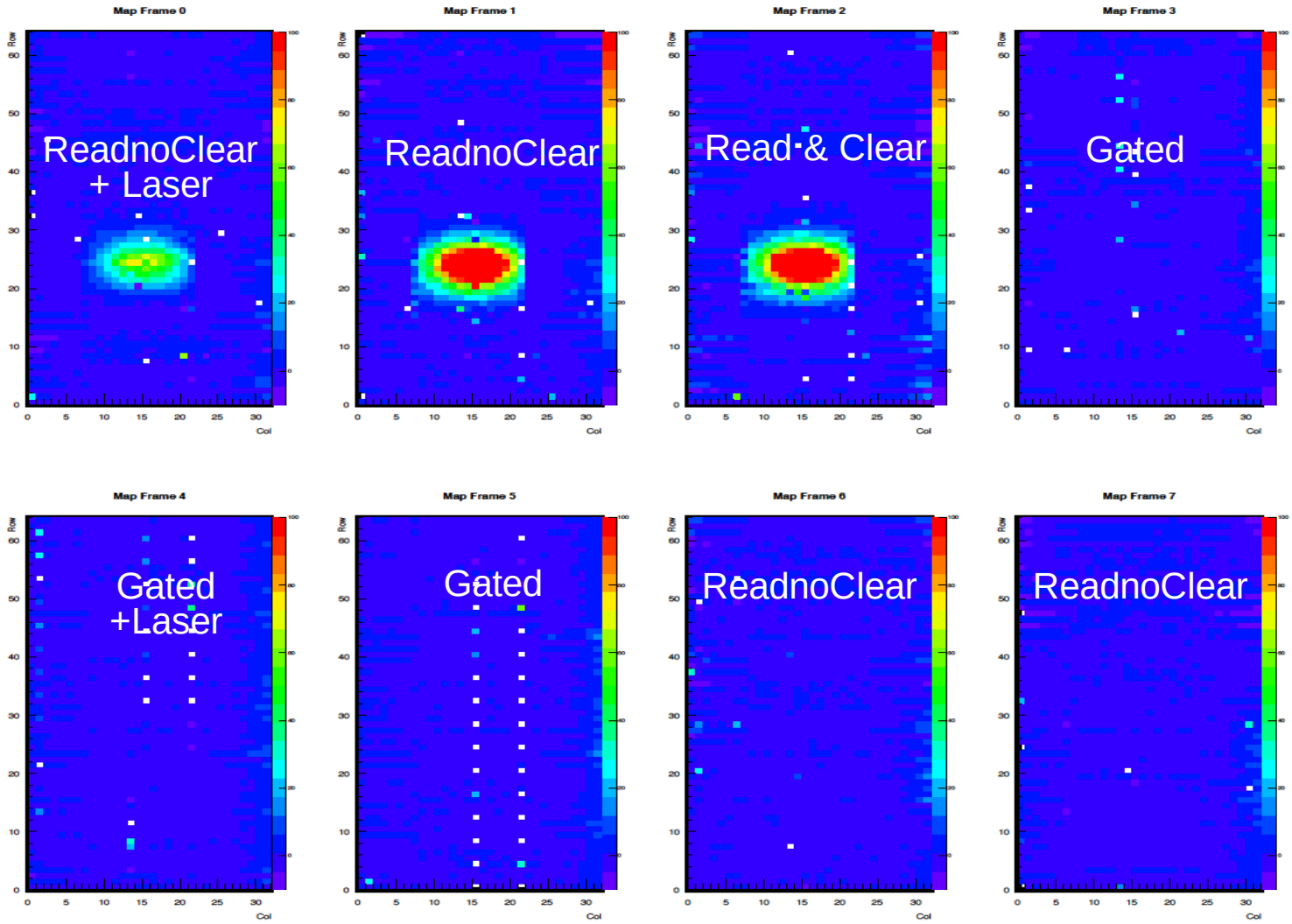
- SwitcherClk off, switch StrC to high, StrG continues running
- Minimum length of 8 falling StrG

Gated Mode w/o RO – *Signal Charge Storage*



- Laser 1µs, 800mV

Gated Mode w/o RO – *Junk Charge generation*



- Laser 1µs, 800mV