Boundary Scan Test of Belle II Pixel Detector Electronics

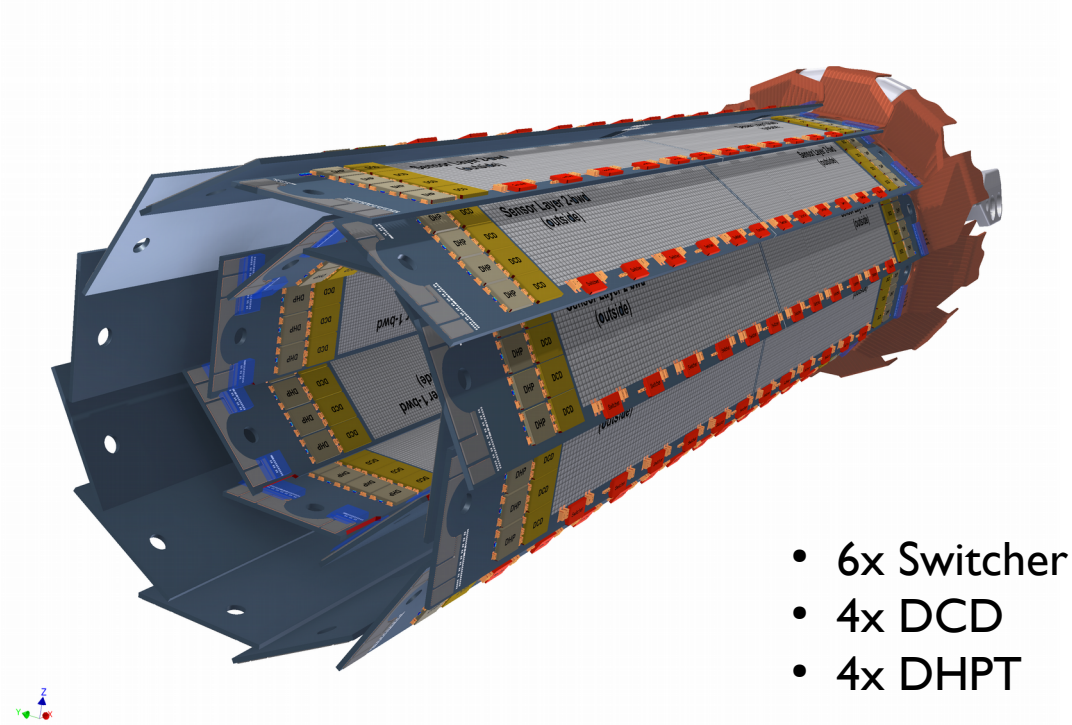
Seeon 12.05.2015

19th International Workshop on

DEPFET Detectors and Applications

Philipp Leitl

PXD bump bonds



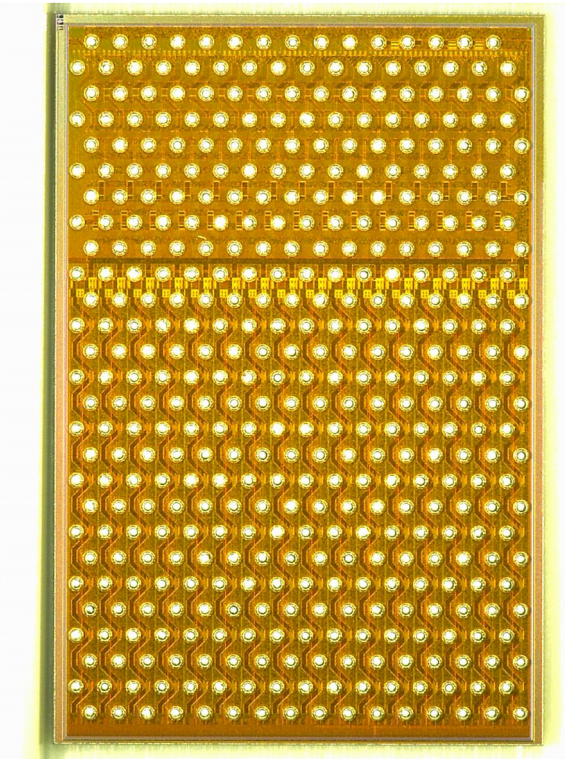
ASIC	Pins
Switcher	96
DCD	431
DHPT	255

- 6x Switcher
- 4x DCD
- 4x DHPT

} 3320 for each half ladder

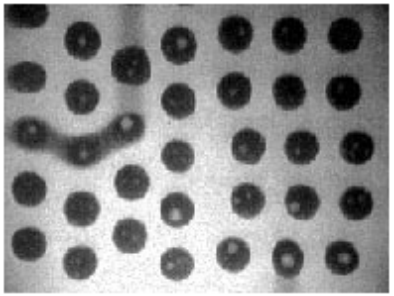
→ 132.800 bump bonded ASIC pins

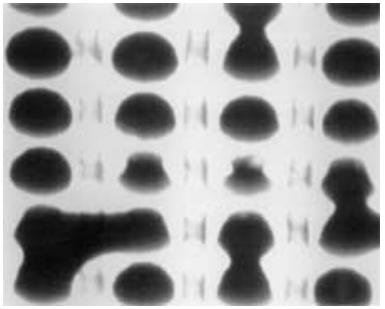
PXD bump bonds

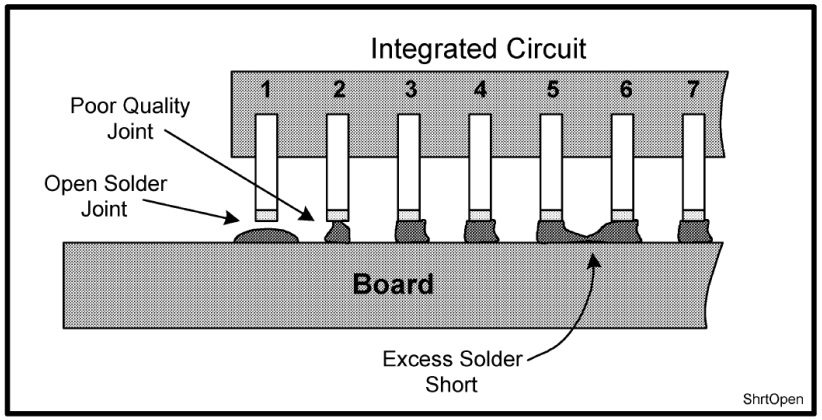


photograph of DCD chip
bump pitch:
200µm in x and 180µm in y

X-ray inspection

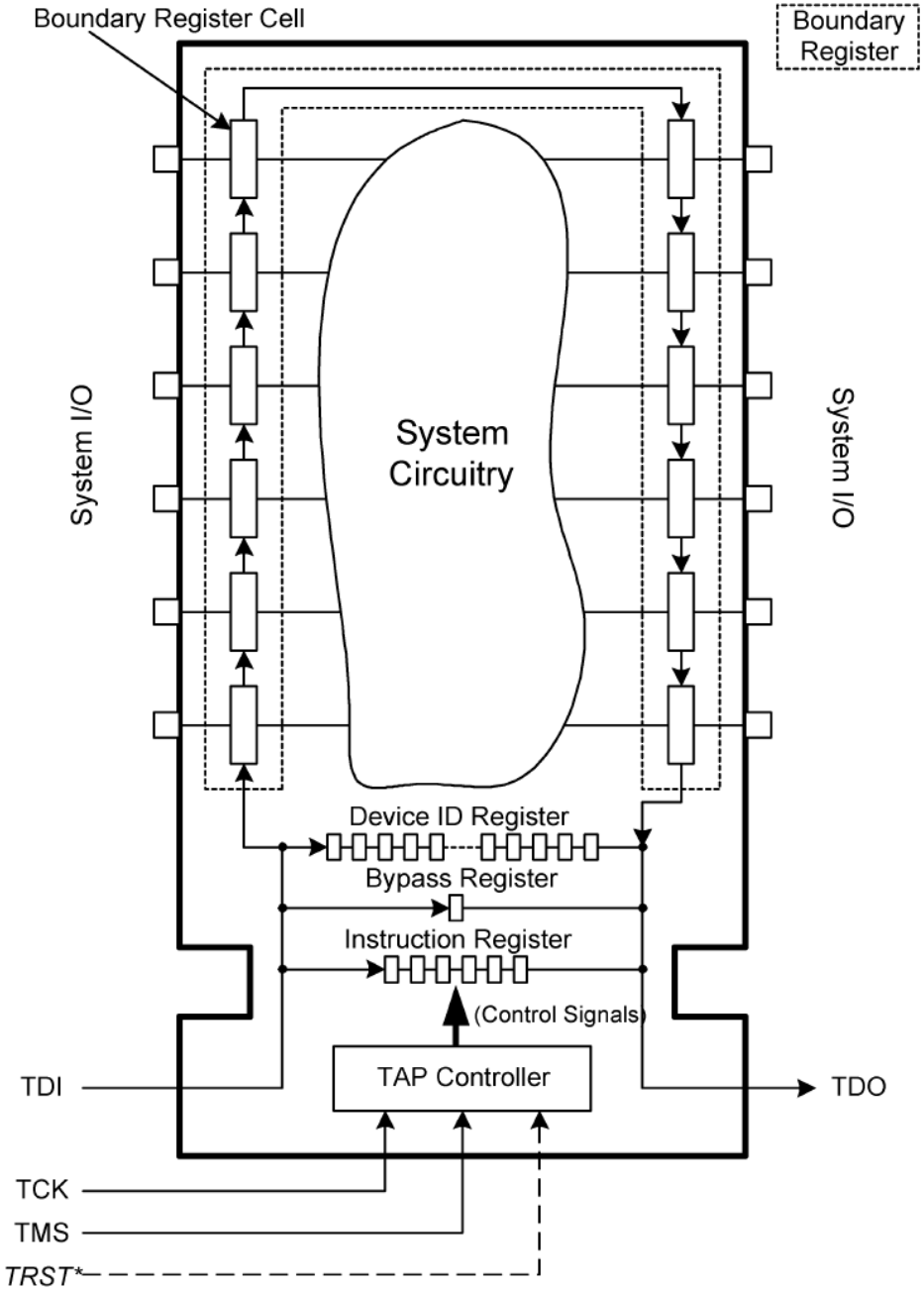






not accessible for a probe station with needles

JTAG



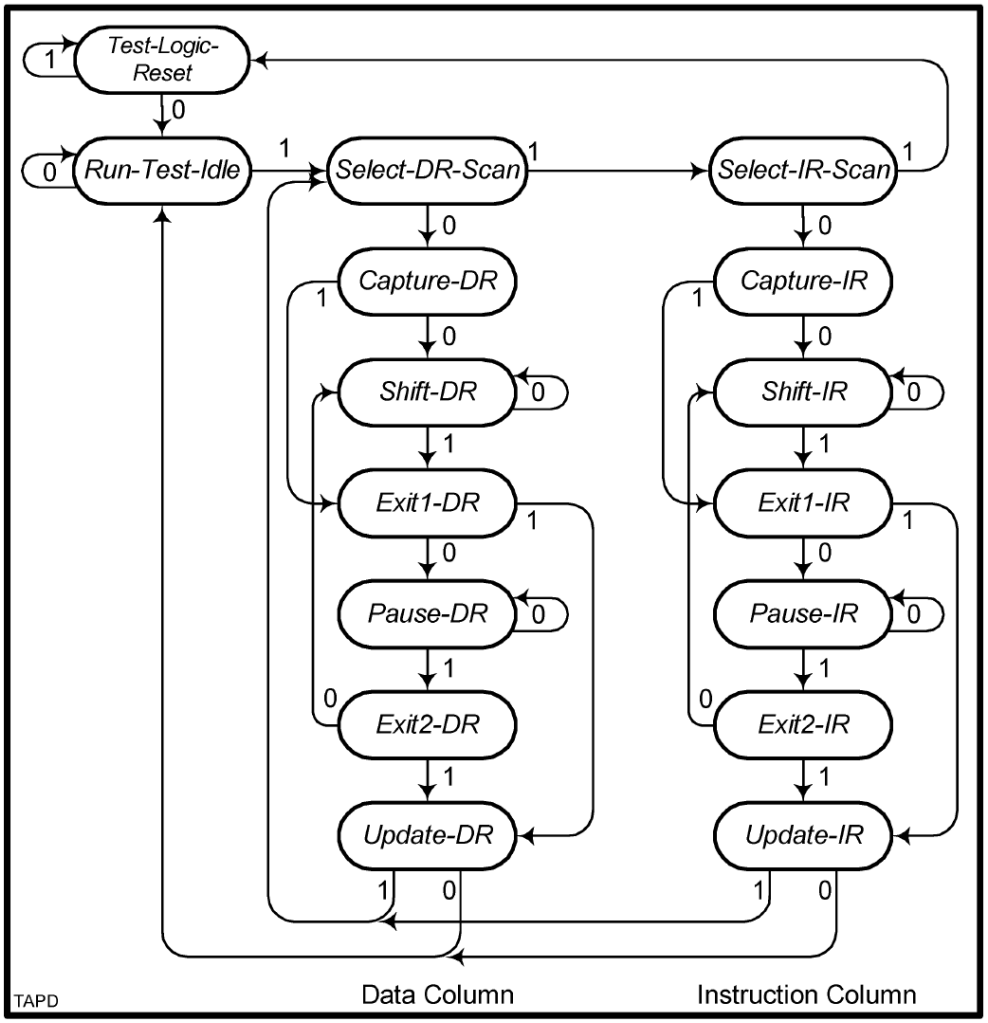
IEEE Std. 1149.1
Joint Test Action Group (JTAG)

additional boundary-scan cells at the I/Os of an IC

four additional I/O ports
Test Access Port (TAP)

TCK	test clock
TMS	test mode select
TDI	test data input
TDO	test data output
(TRST	test reset)

TAP controller

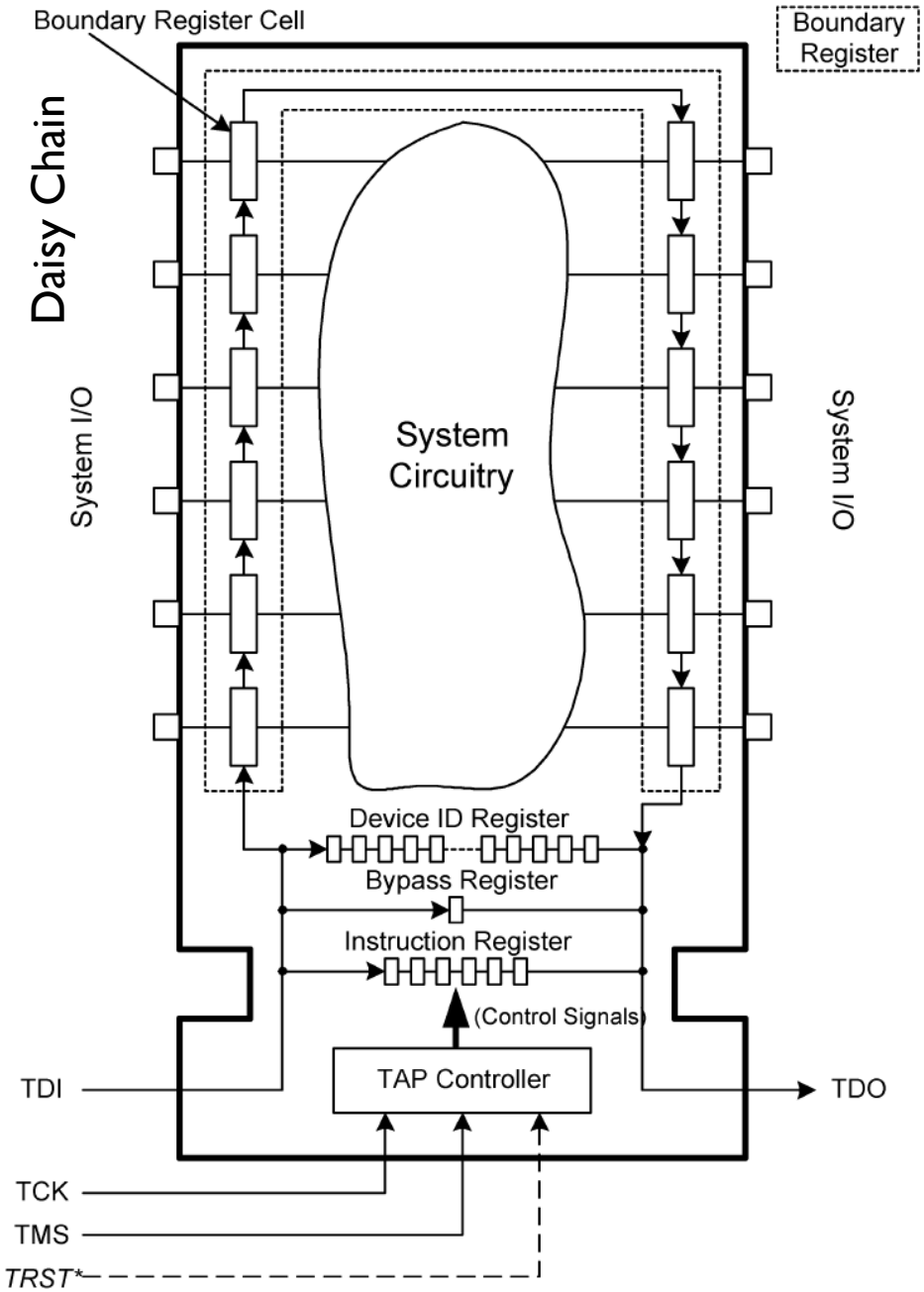


State transition diagram of the TAP controller (Test Access Port)

16 state machine

controlled by TCK and TMS

JTAG



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four additional I/O ports
Test Access Port (TAP)

TCK	test clock
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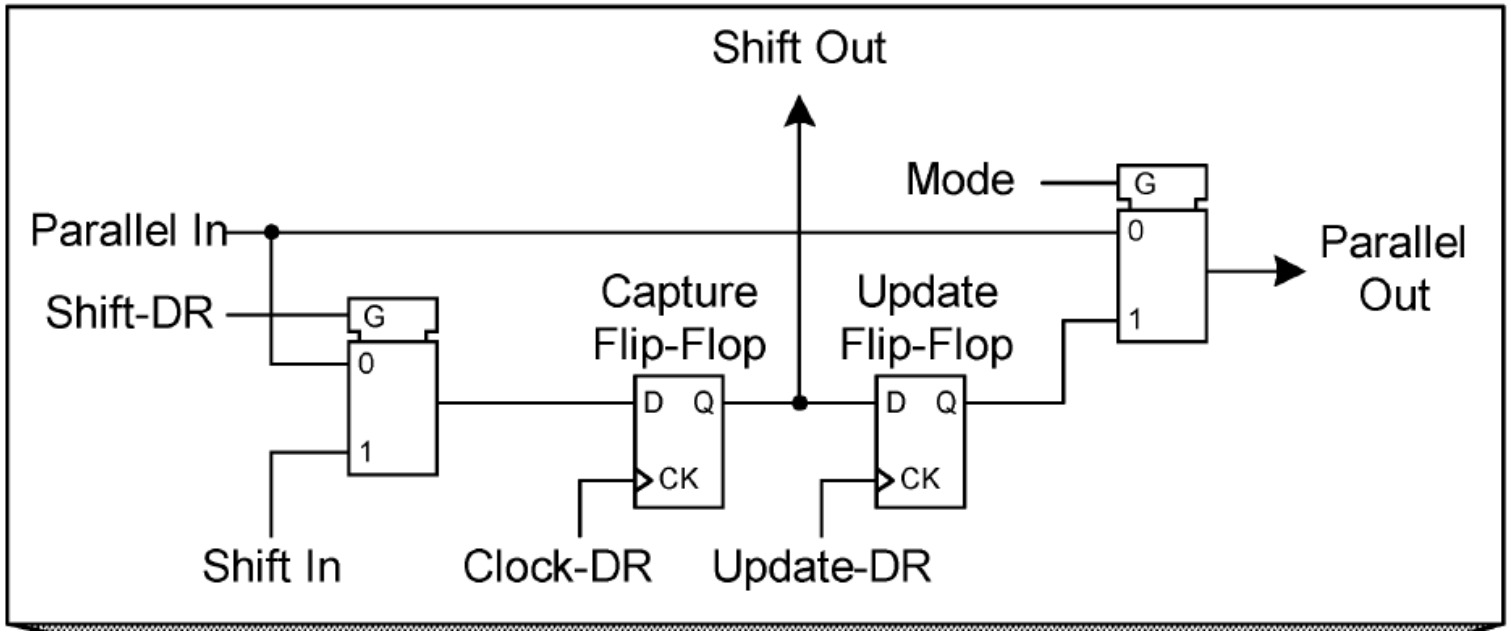
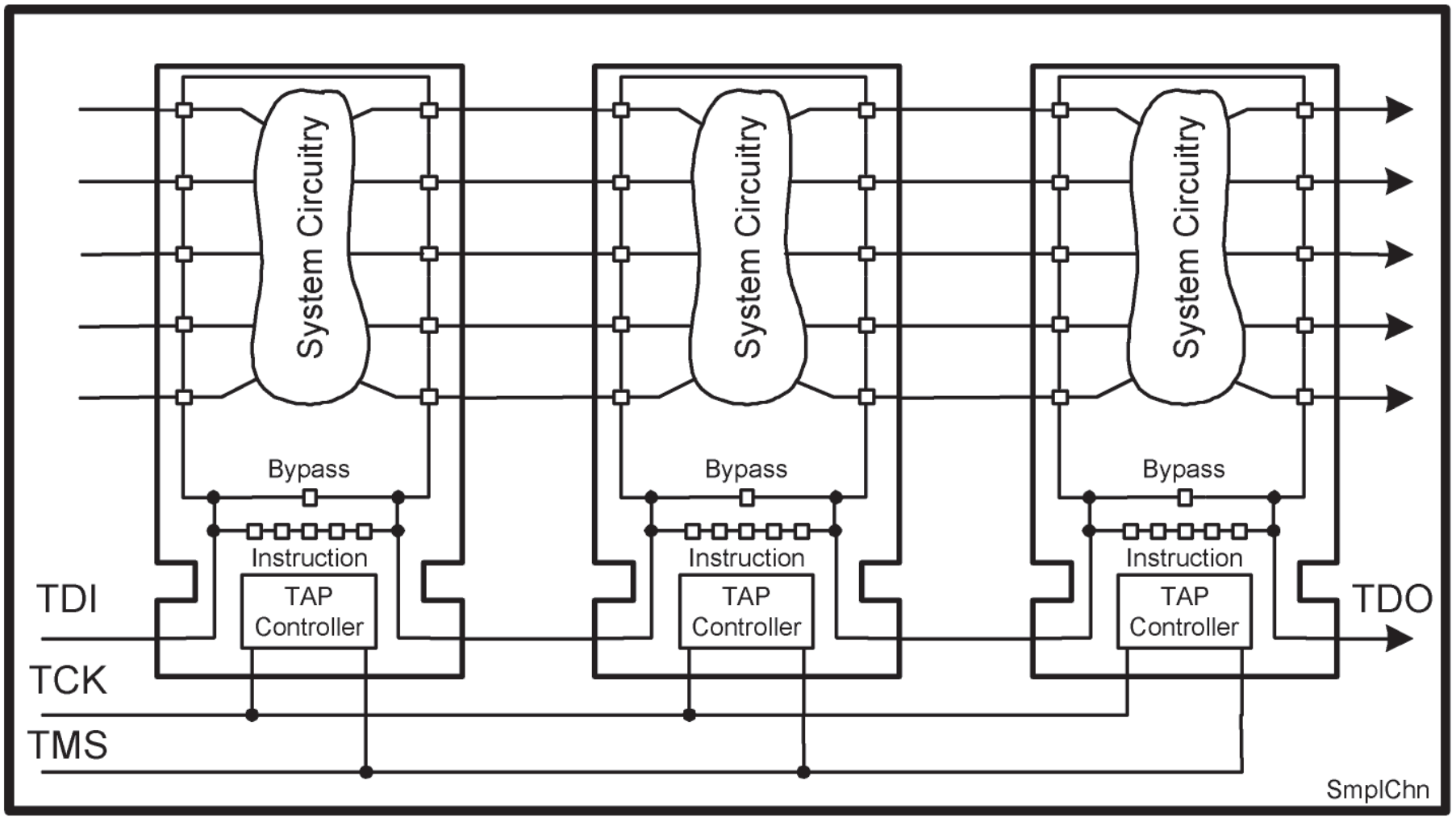
Boundary Register Cell

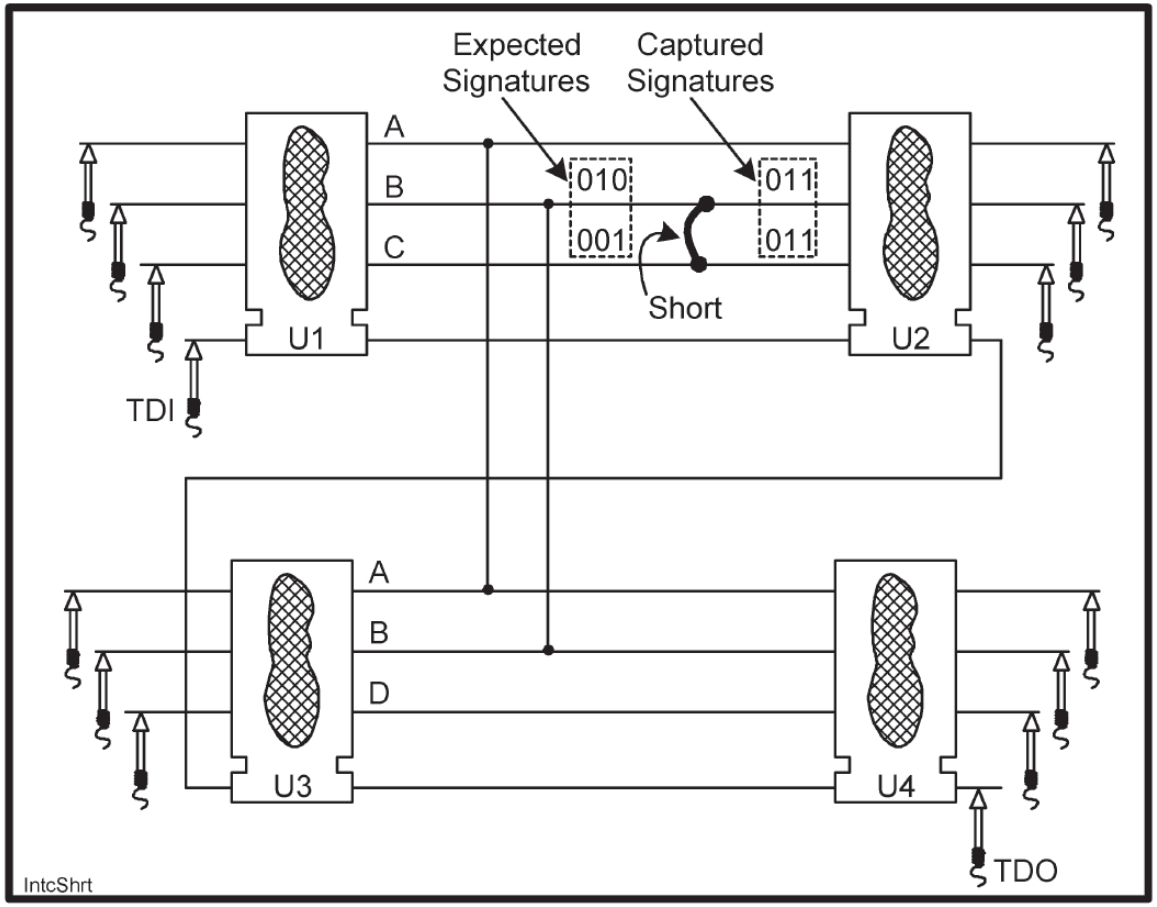


two multiplexer
two flip-flops

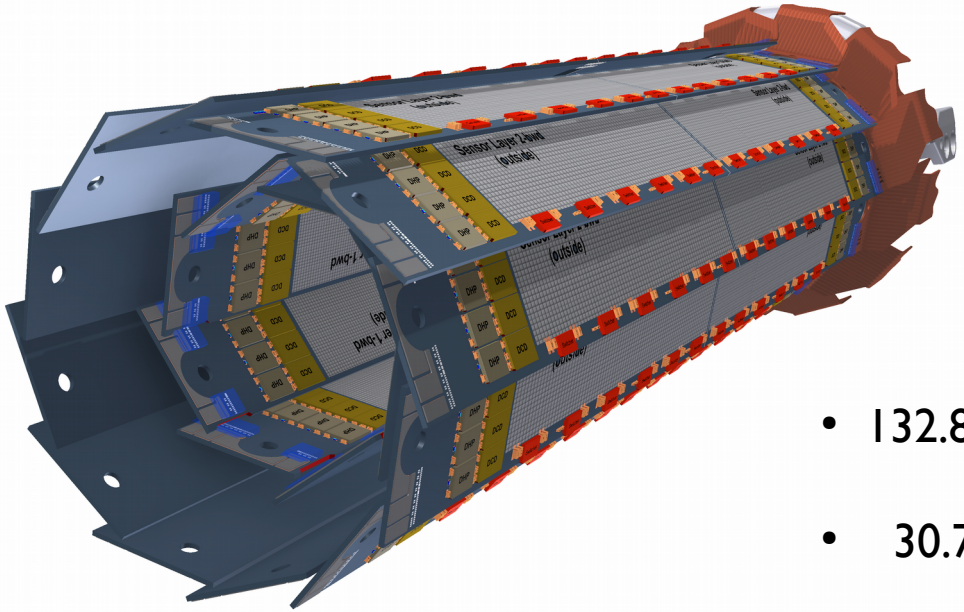
Chain of Boundary Scan ICs



Interconnect Test



PXD bump bonds

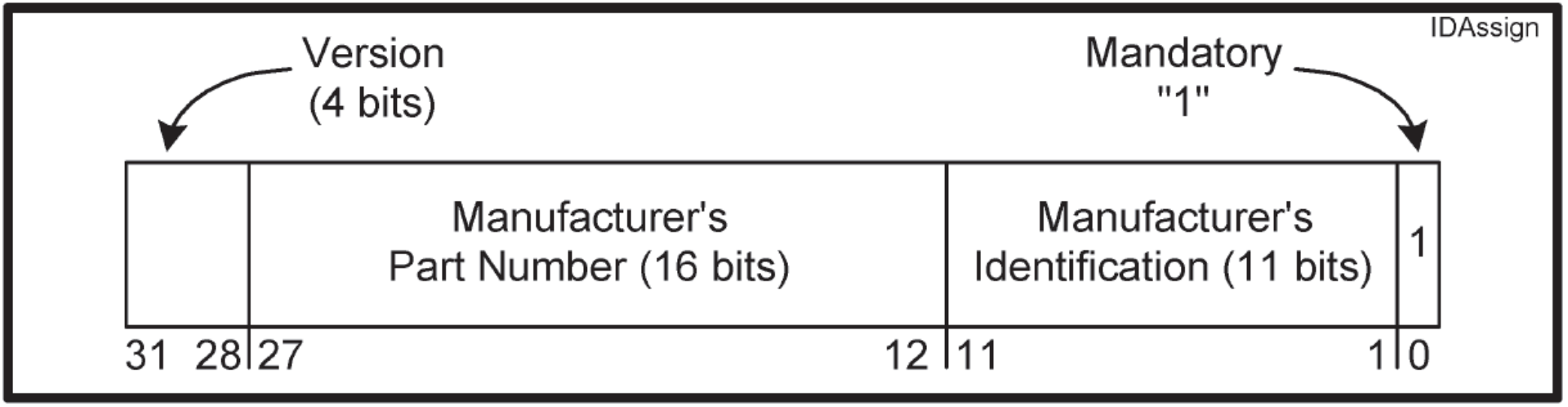


ASIC	Pins	BSC (Pins)
Switcher	96	10
DCD	431	80
DHPT	255	97

- 132.800 bump bonded ASIC pins
- 30.720 accessible through BS

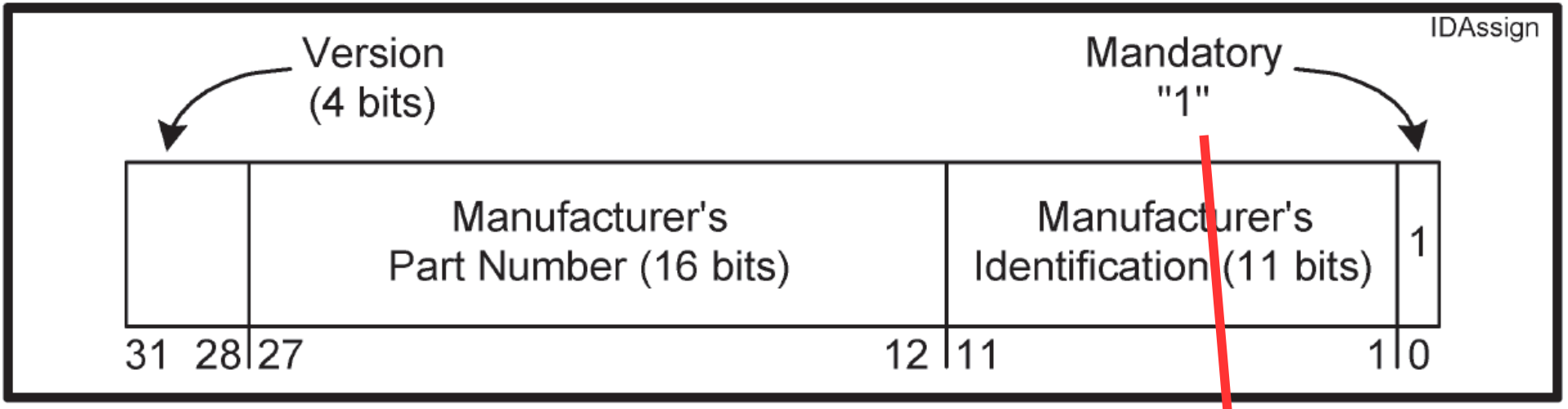
→ ~ 23% direct test coverage
(additional functional tests:
power pins, JTAG pins, CLK, ...)

ID Code



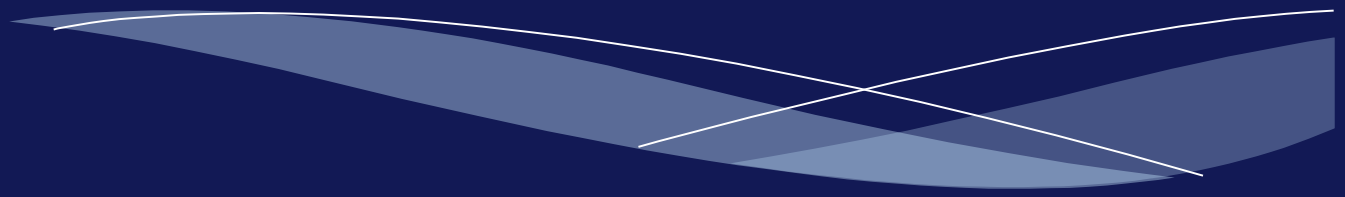
	hex	binary
Switcher18v2	23456789	0010 0011010001010110 011111000100 1
DCD	12345678	0001 0010001101000101 011001111100 0
DHPT1.0	44485011	0100 0100010010000101 00000001000 1

ID Code

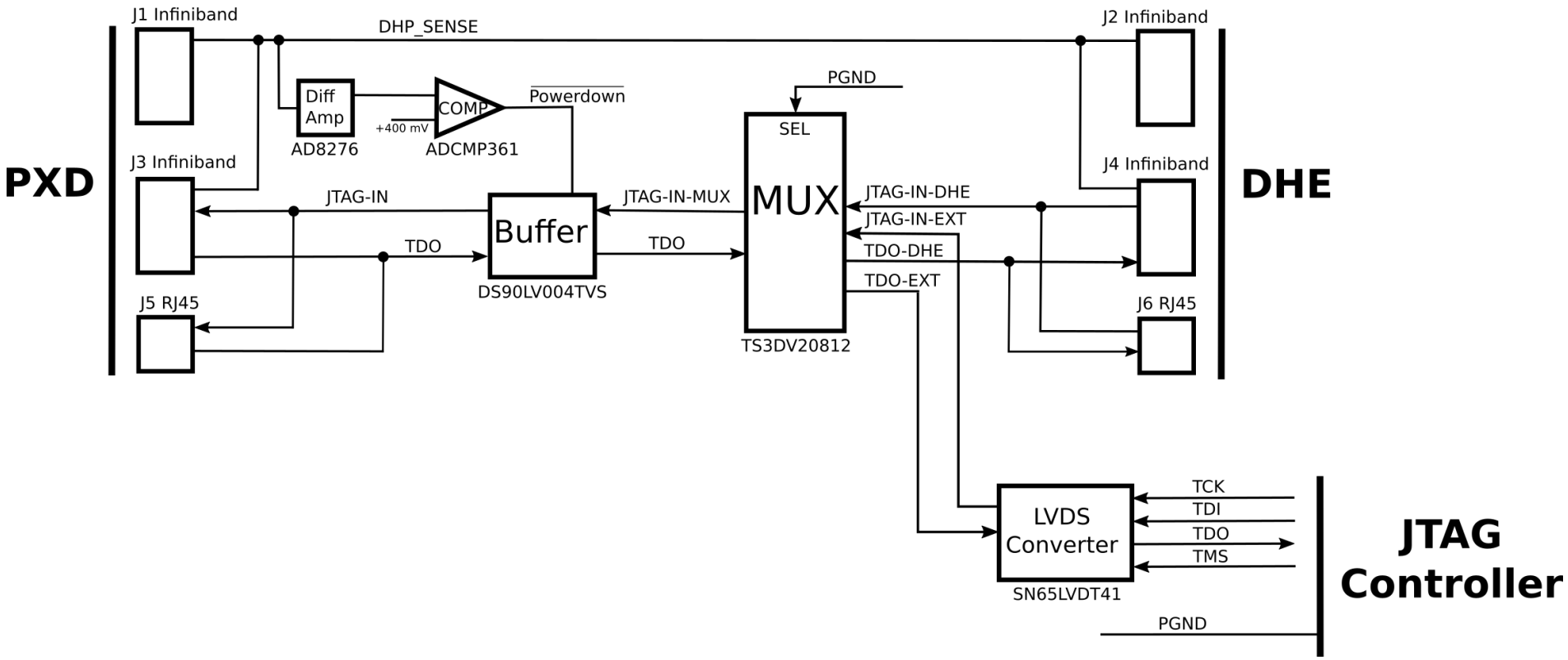


	hex	binary
Switcher18v2	23456789	0010 0011010001010110 011110001001
DCD	12345678	0001 0010001101000101 0110011110 0
DHPT1.0	44485011	0100 0100010010000101 00000001000 1

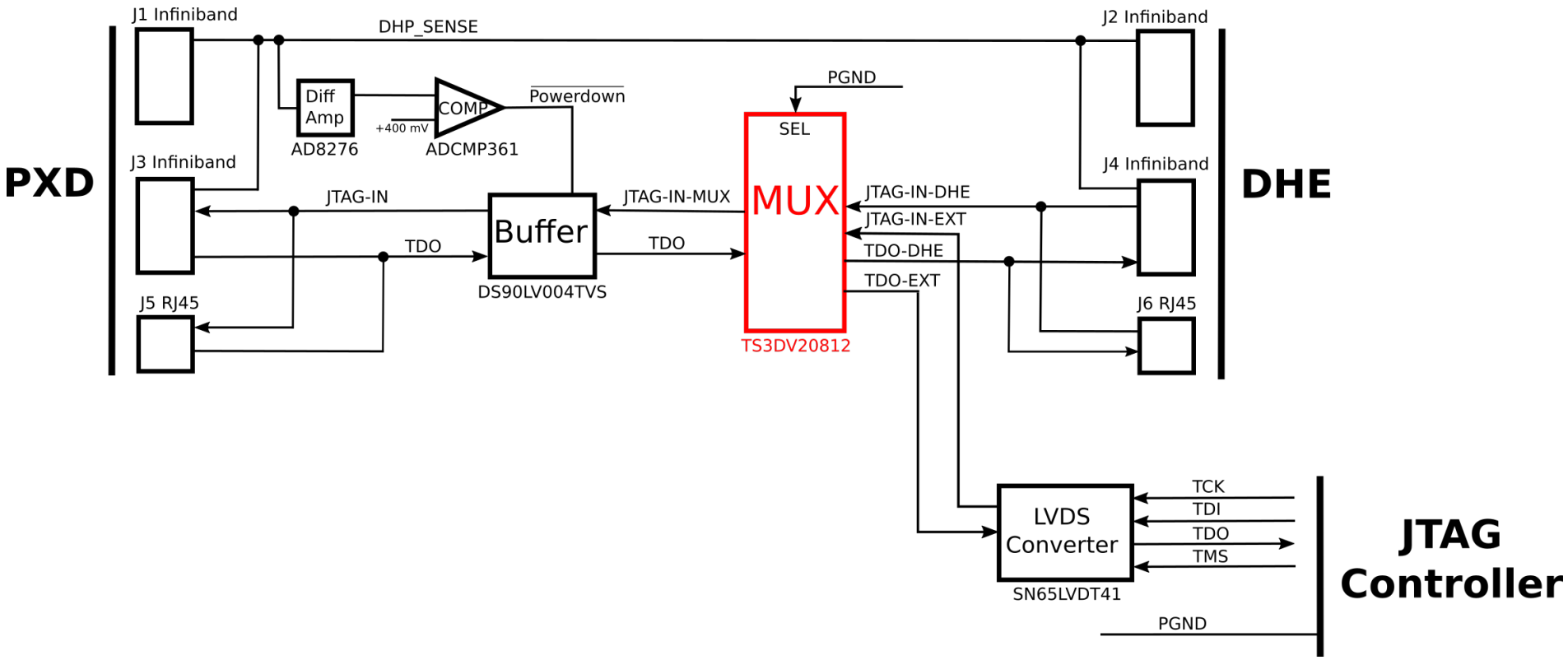
HARDWARE



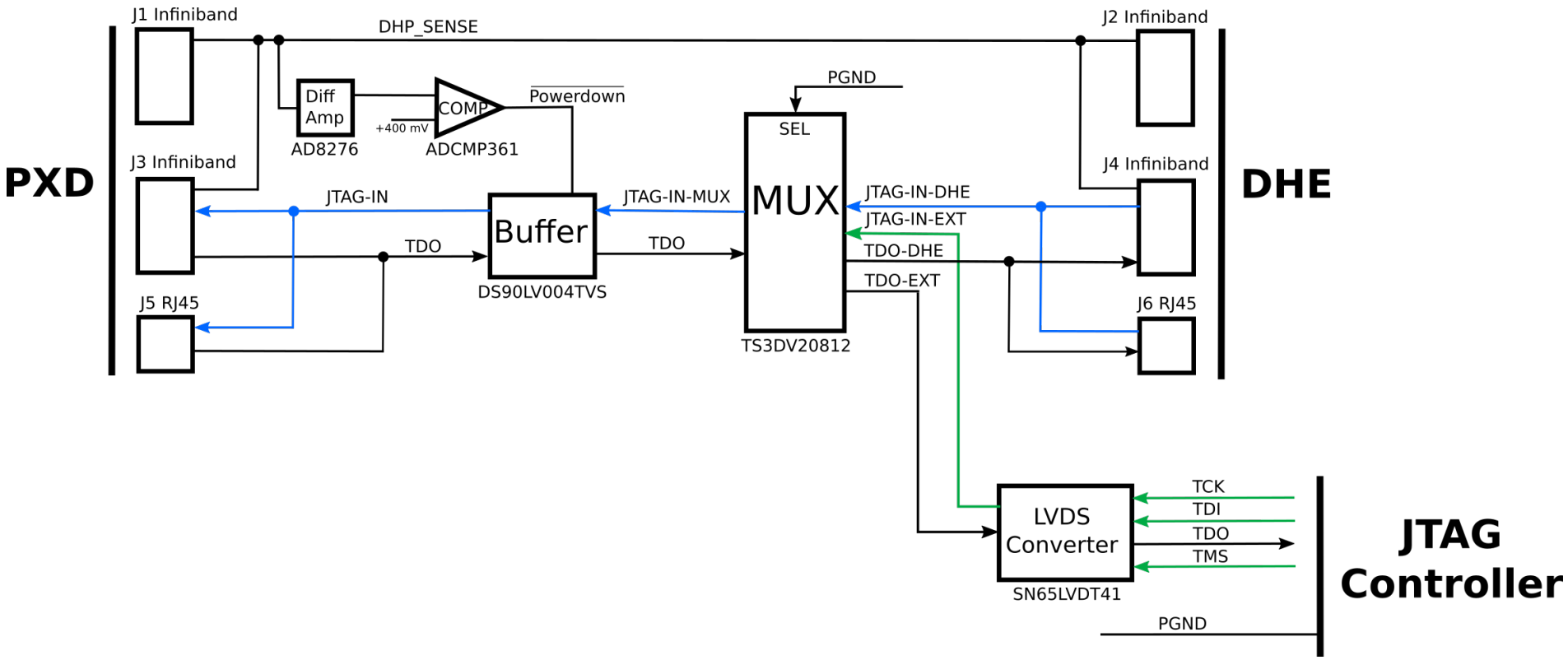
JTAG Breakout Board



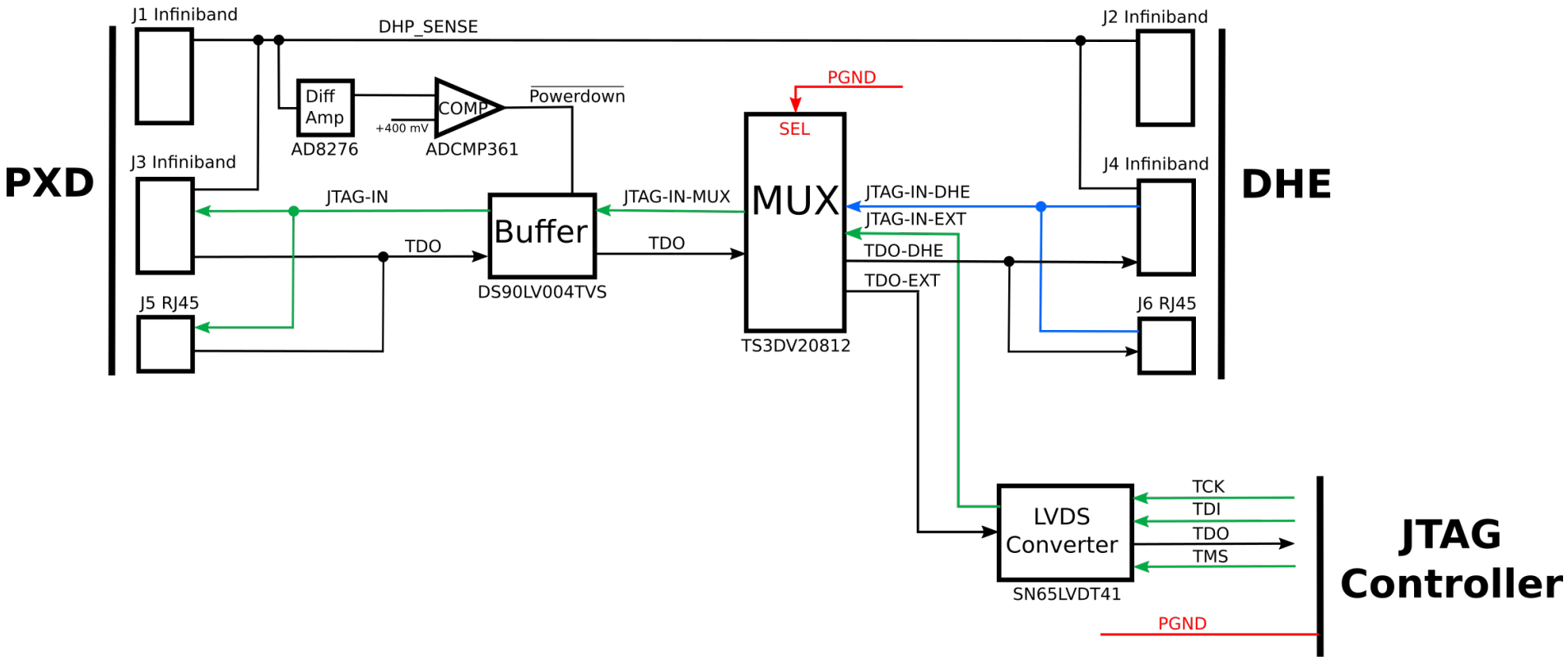
JTAG Breakout Board



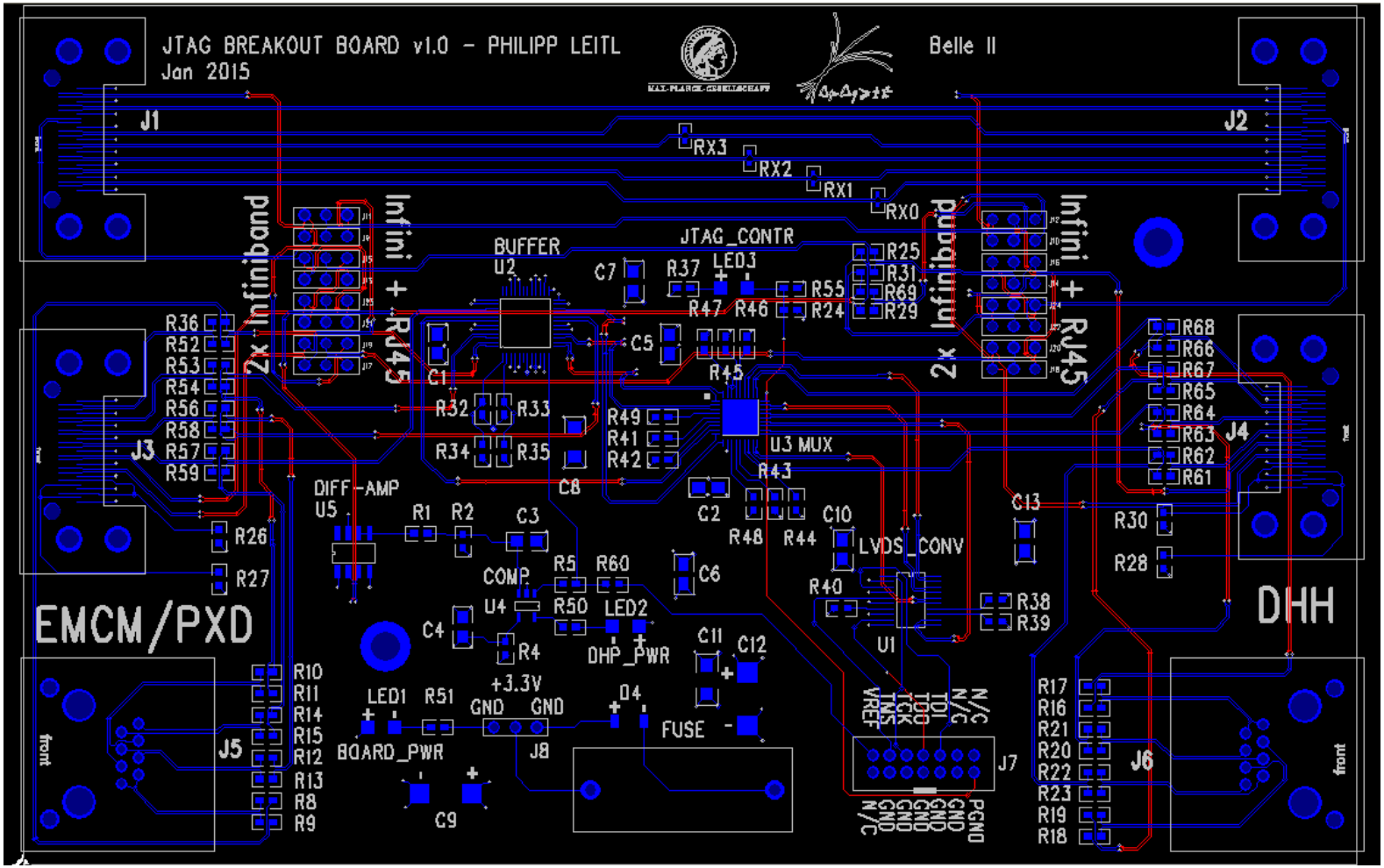
JTAG Breakout Board



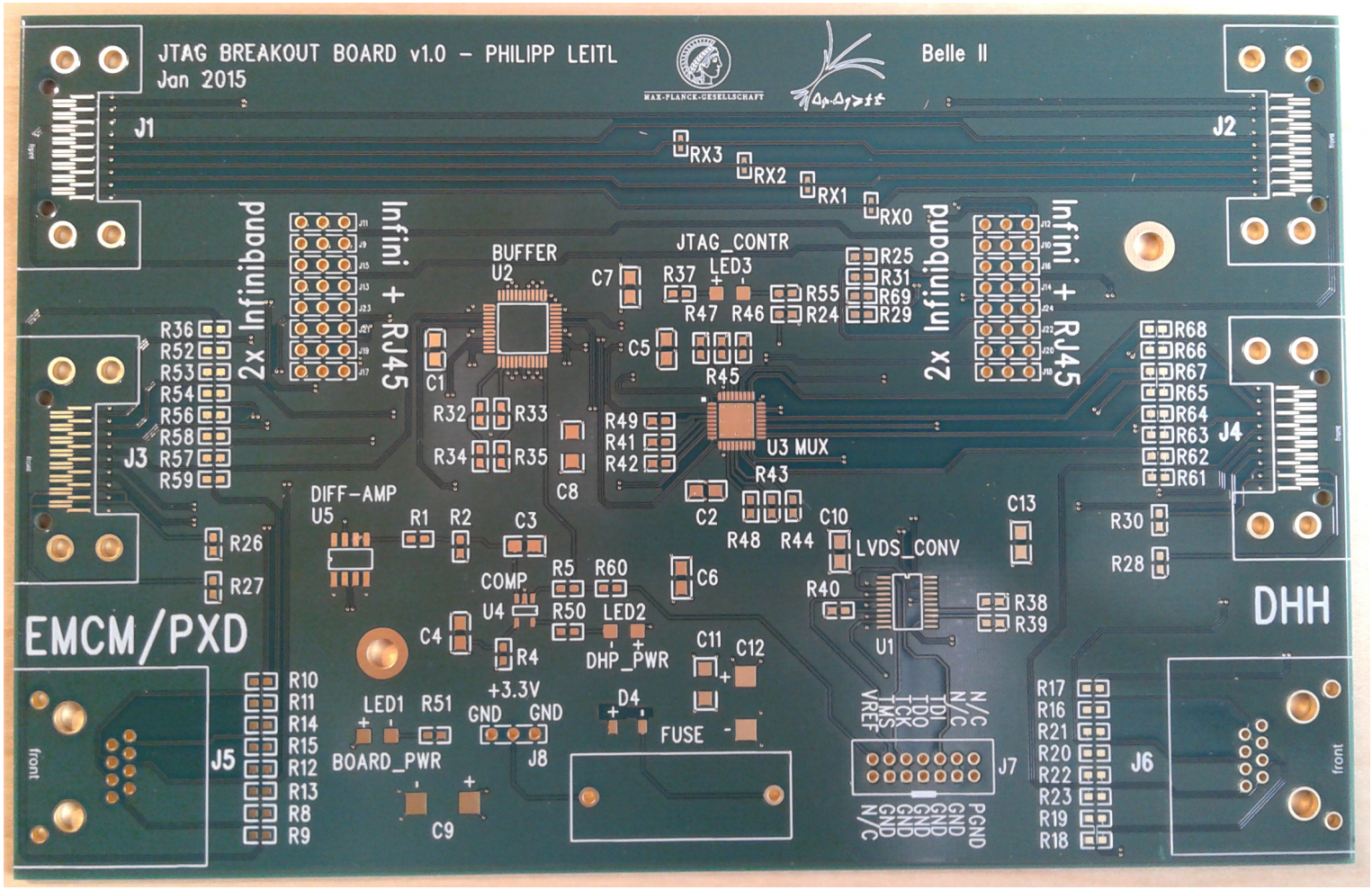
JTAG Breakout Board



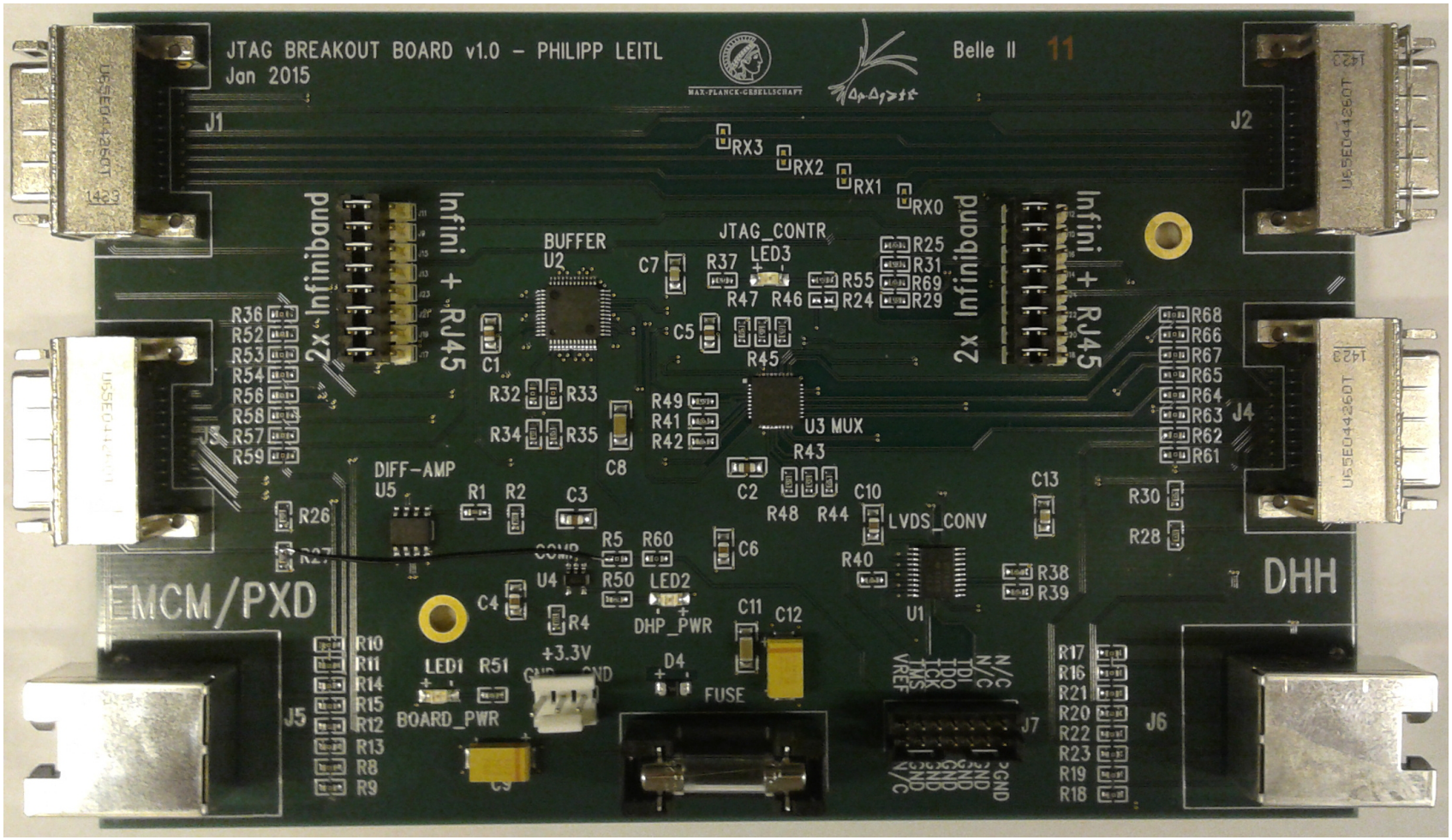
JTAG Breakout Board



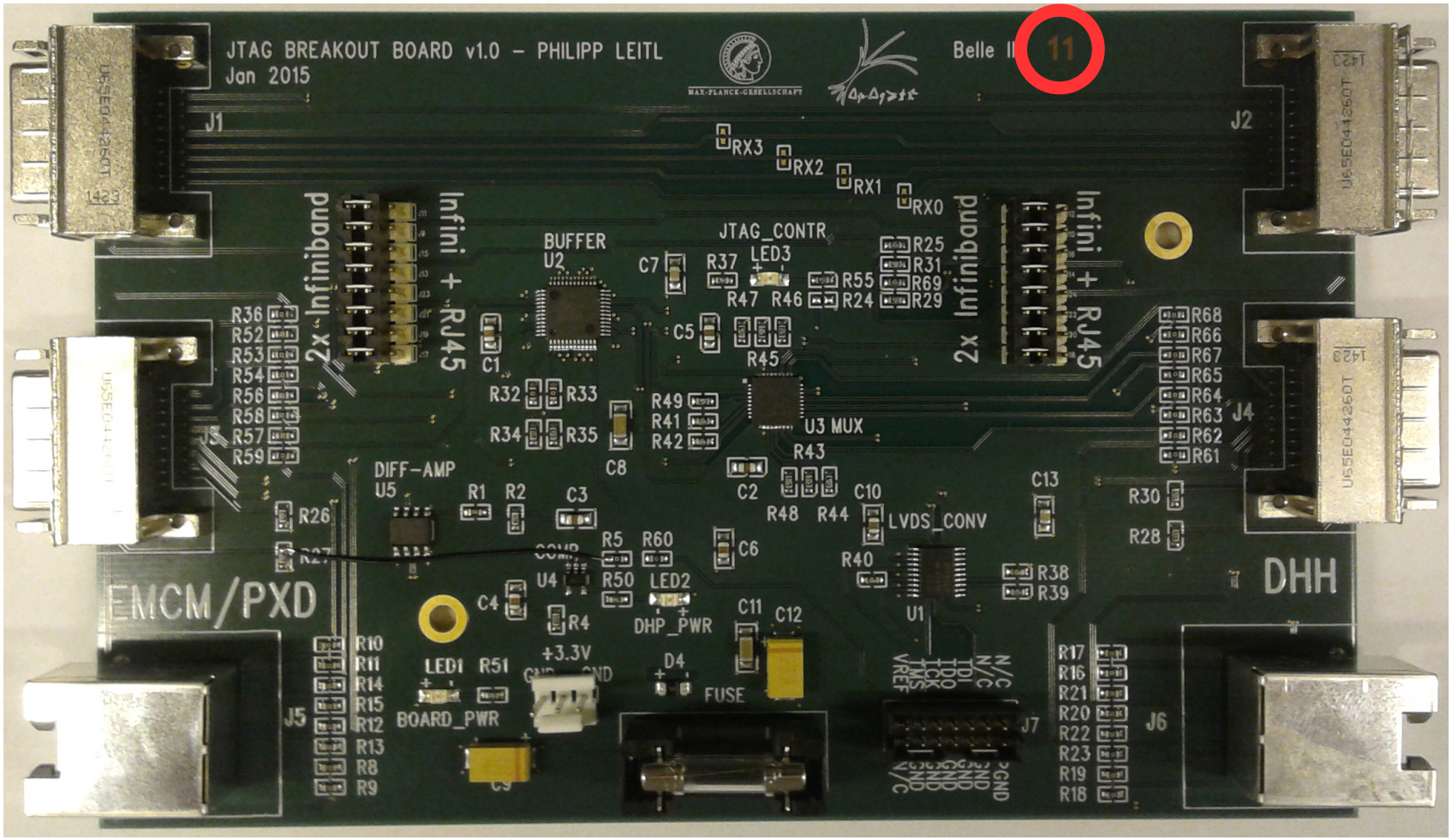
JTAG Breakout Board



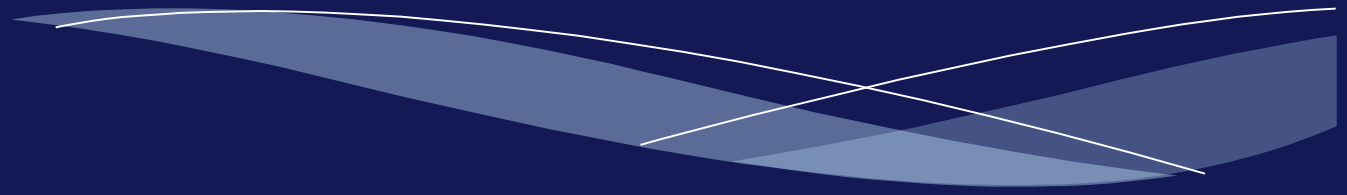
JTAG Breakout Board



JTAG Breakout Board



SOFTWARE



Boundary Scan Software

- New commercial system needed → offers from different vendors
  - demo-version in the meantime
  - different JTAG controller → adapter needed

- Requirement: Boundary Scan Description Language (BSDL) files
  - DHP and DHPT: software generated
  - SwitcherB18 v1 and v2: manually written by Christian Kreidl
  - DCD: manually written by me

BSDL File DCD

Verilog file (jtag.v):

```
105  //wire to connect the boundary scan chain
106  wire     [82:0]          bs_chain;
107  wire                     bs_chain_tdo;
```

80 BSCs (8 columns with 8x DO and 2x DI each)
+ 4 additional BSCs

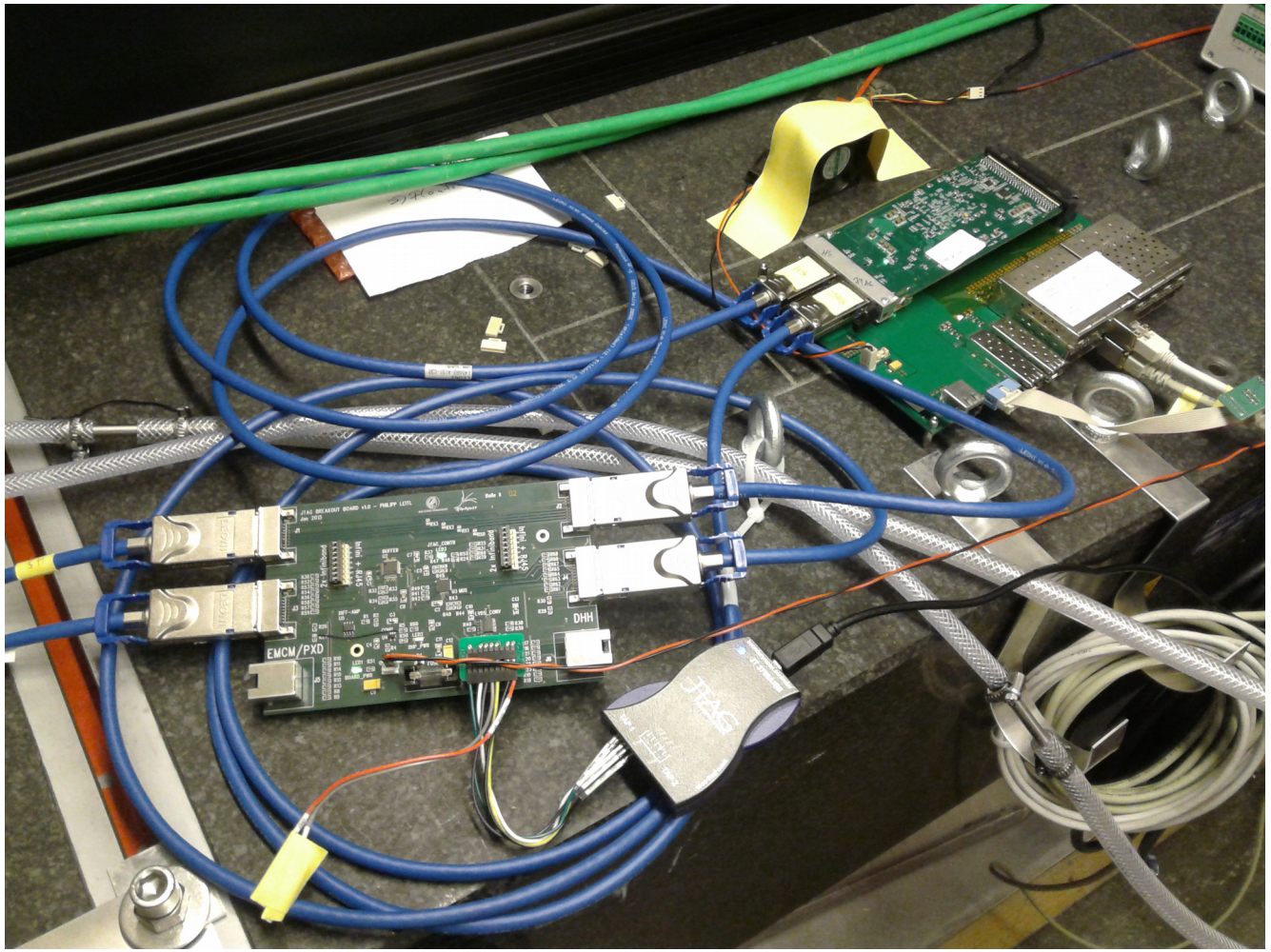
BS_input_cell_sync_reset_I
BS_input_cell_clk_I
BS_output_cell_return_clk
BS_input_cell_test_injection_en_I

84 BSC in total

BSDL file:

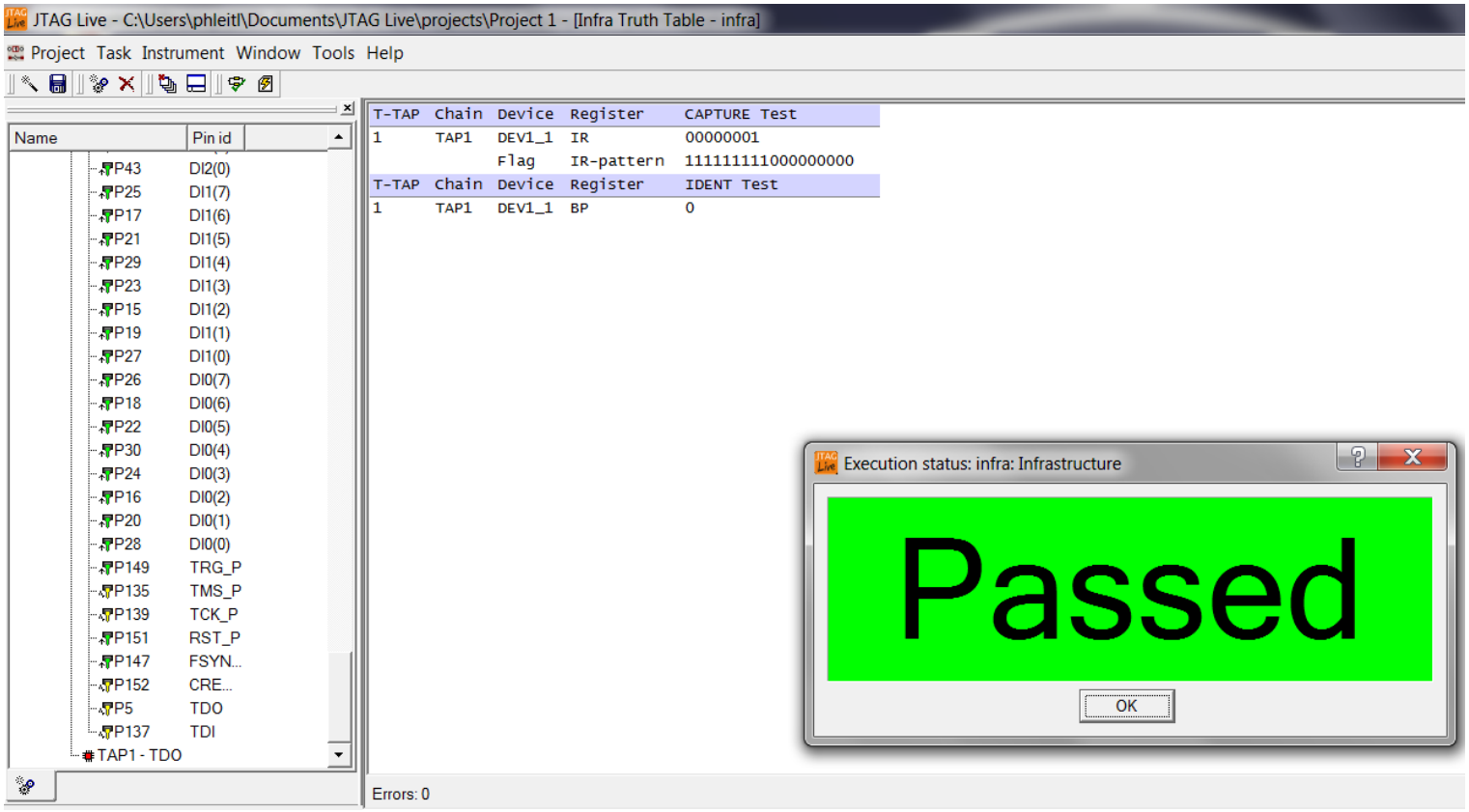
```
178 -- Specifies the length of the boundary scan register.
179
180    attribute BOUNDARY_LENGTH of DCD_top: entity is 84;
```

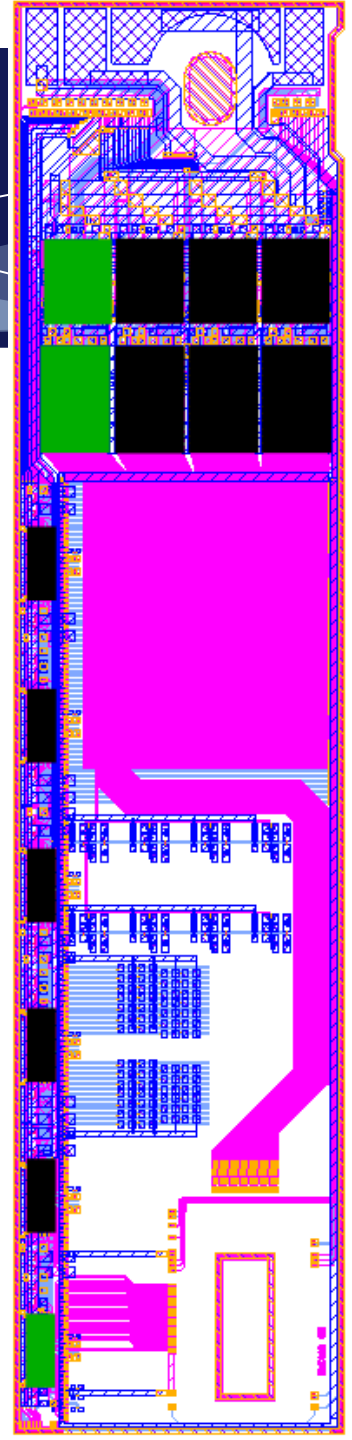
First Boundary Scan Tests



EMCM P6-1

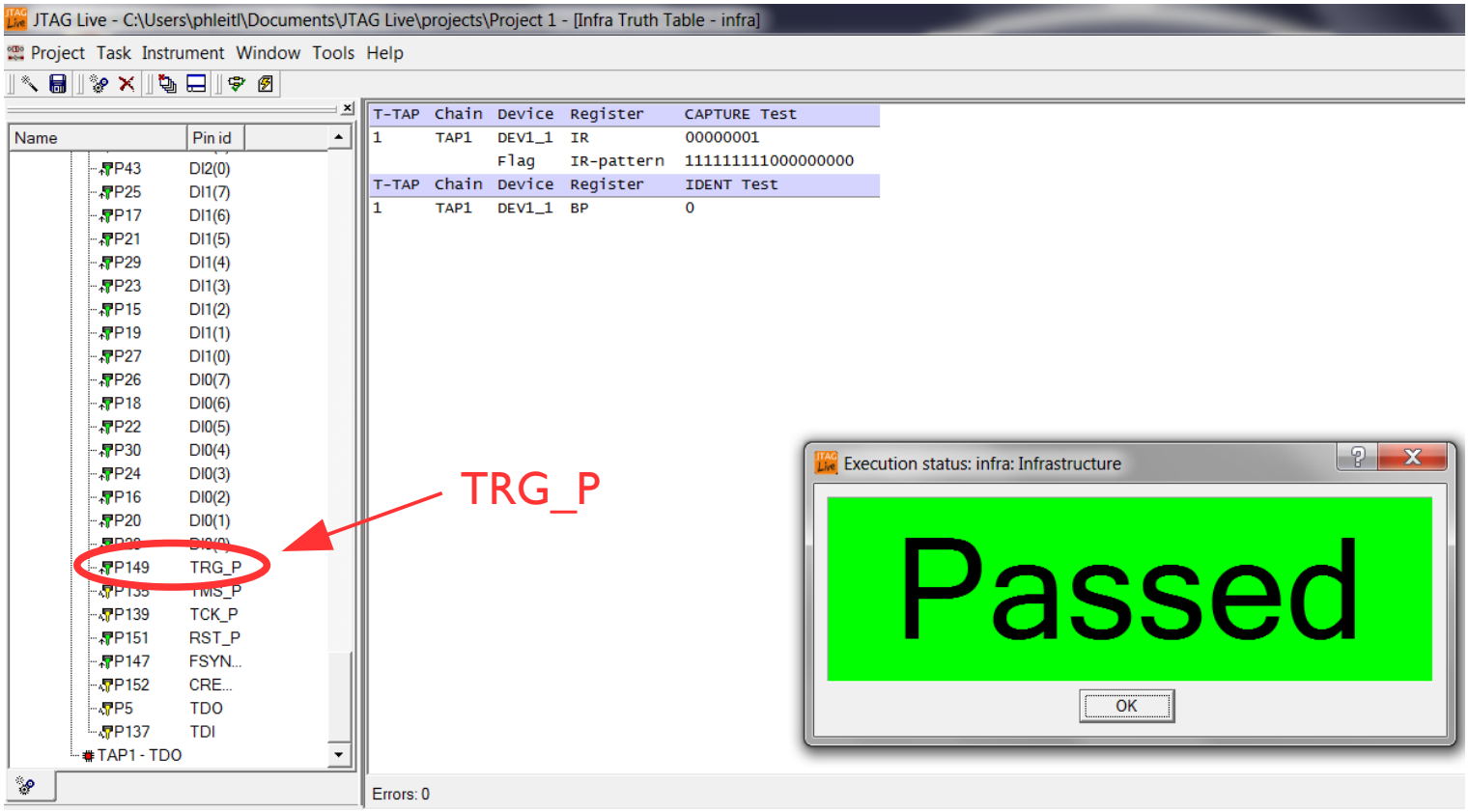
old ASICs: 1x DHP0.2, 1x DCD and 1x SwitcherB18v1

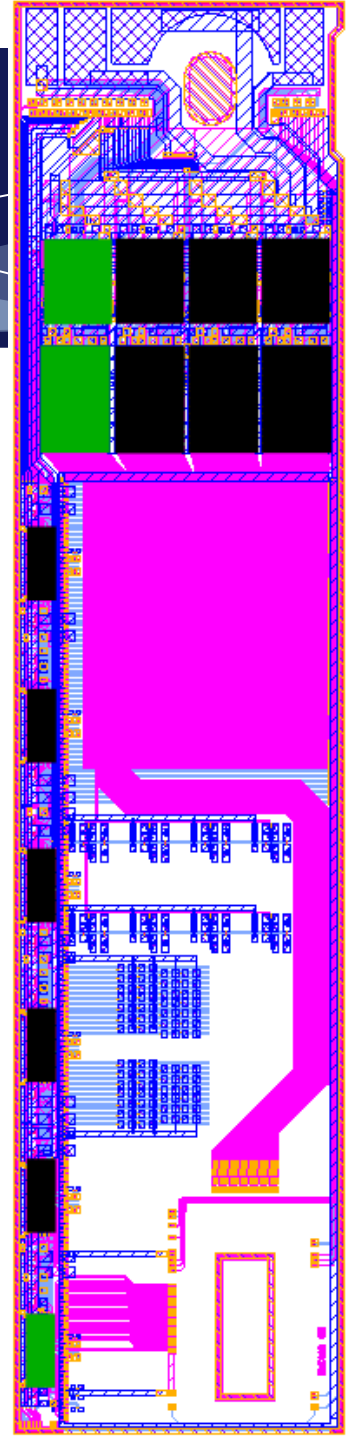




EMCM P6-1

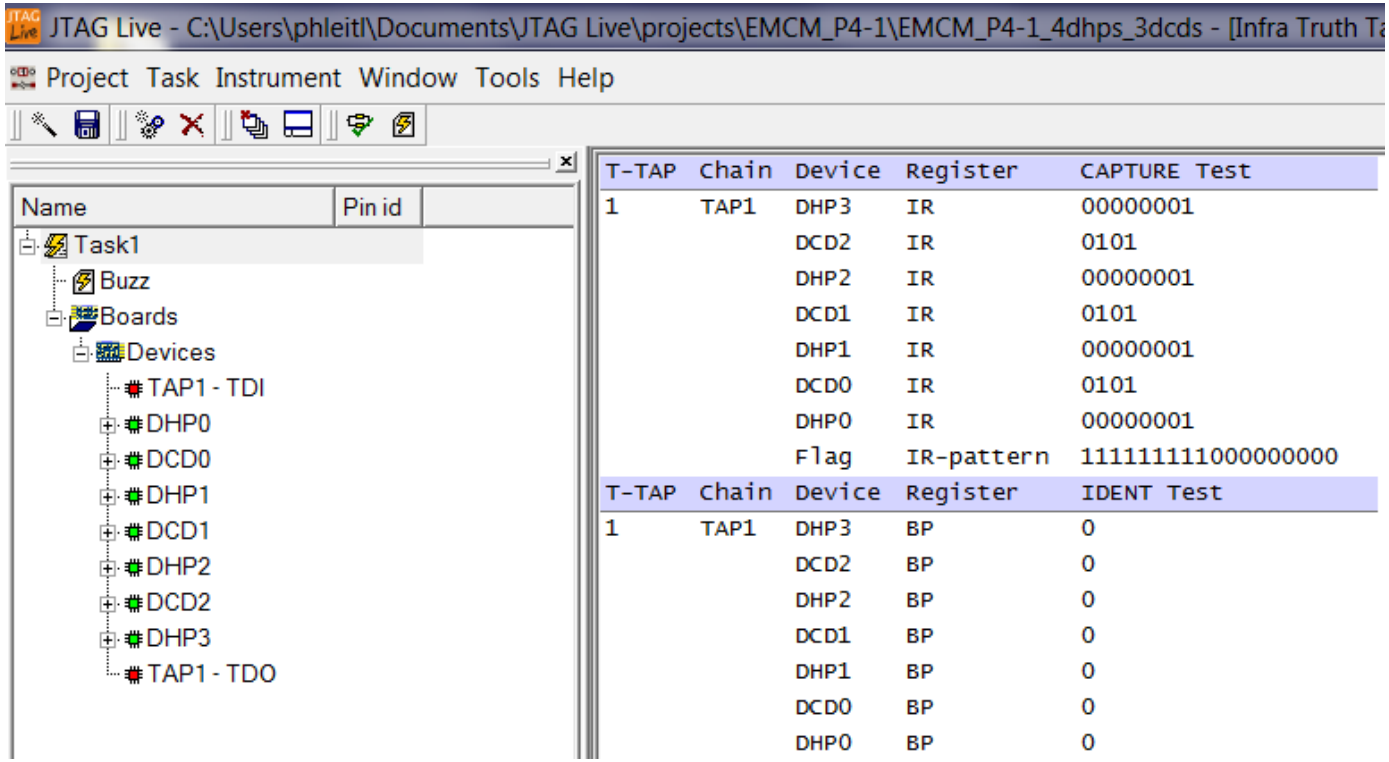
old ASICs: 1x DHP0.2, 1x DCD and 1x SwitcherB18v1

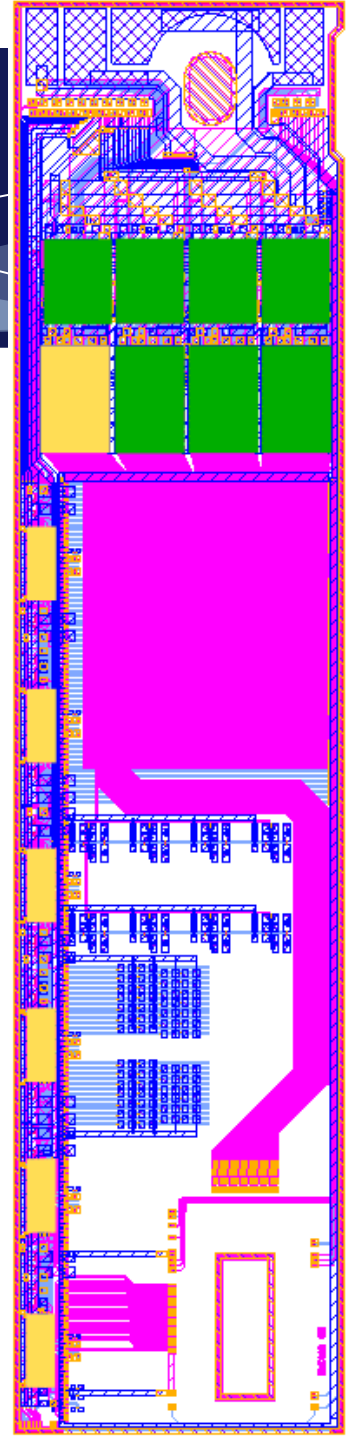




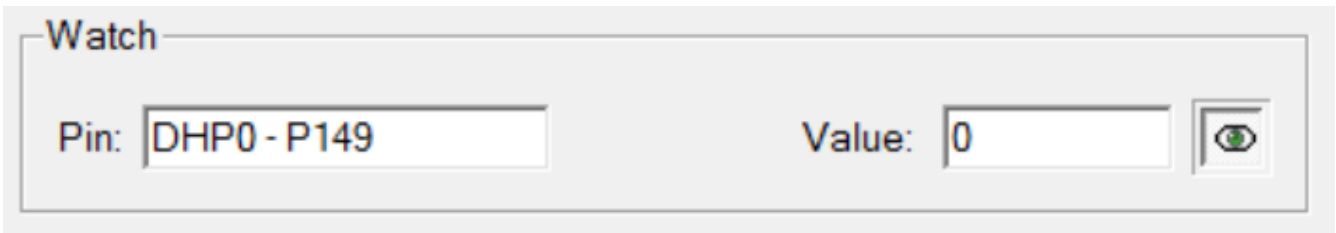
EMCM P4-1

old ASICs: 4x DHP0.2, 4x DCD and 6x SwitcherB18v1
(JTAG chain through Switchers not working)

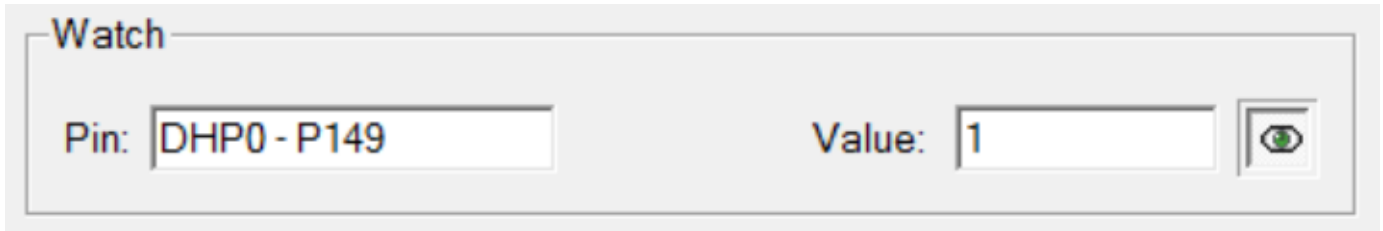


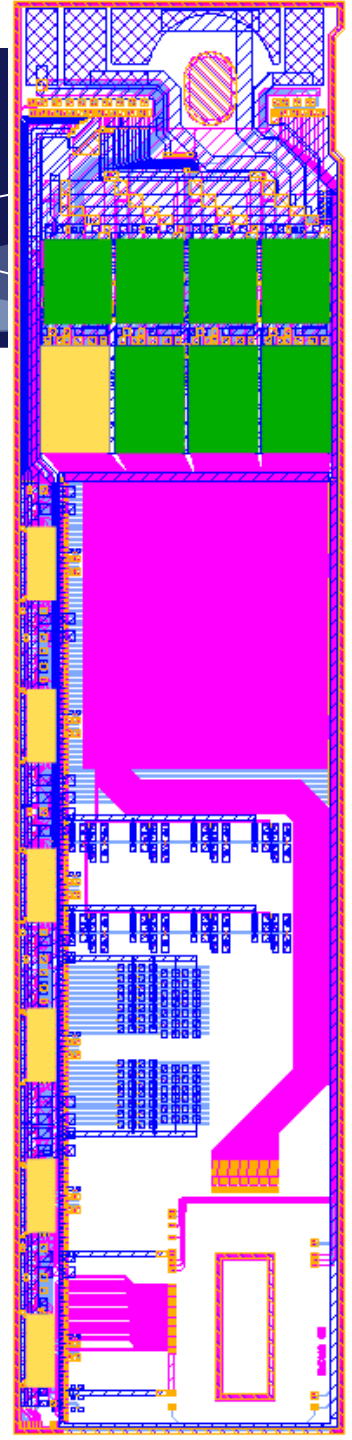


EMCM P4-1



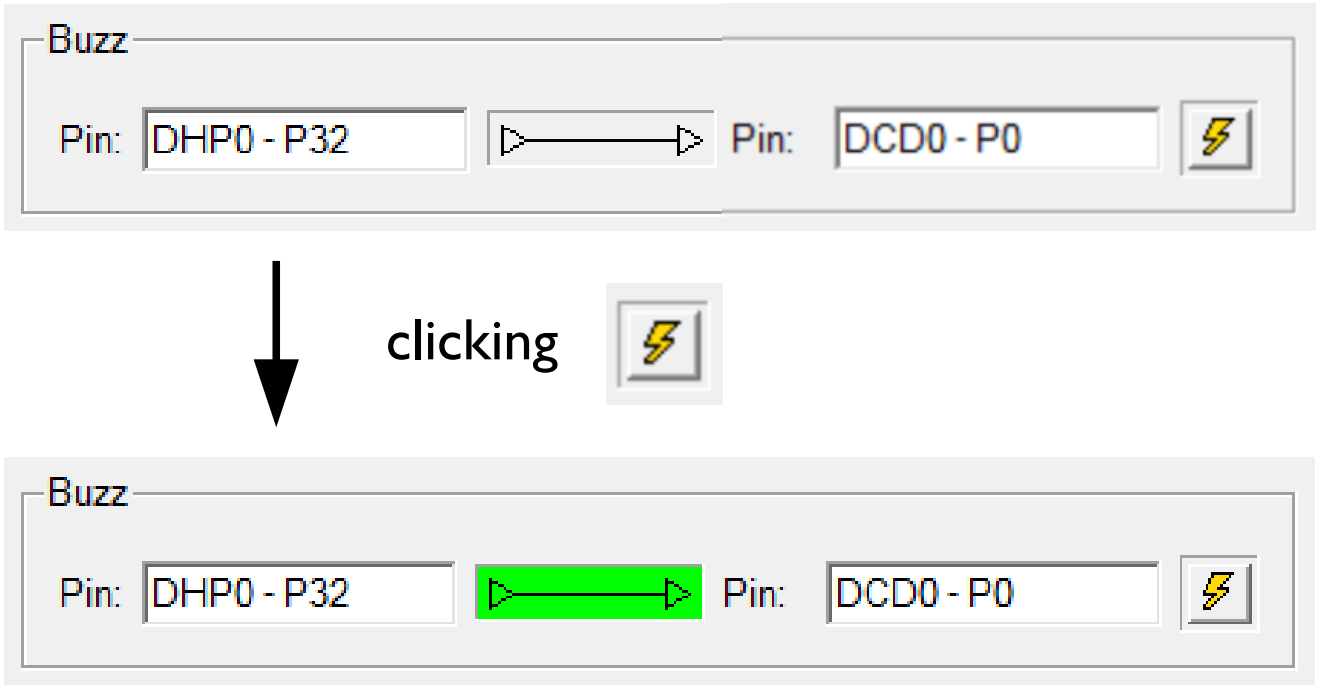
Toggle TRG signal

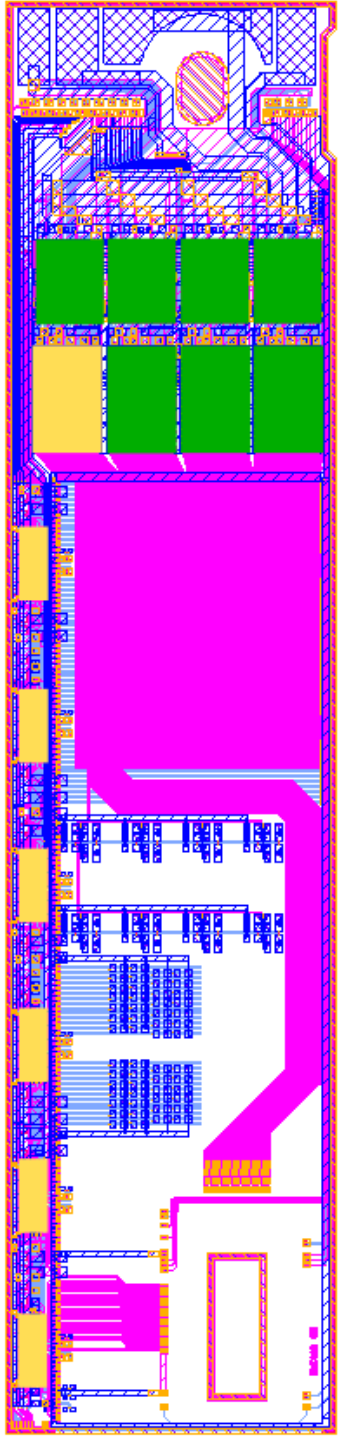




EMCM P4-1

Interconnect test between DHP: DO0(0) and DCD: DI0(0)

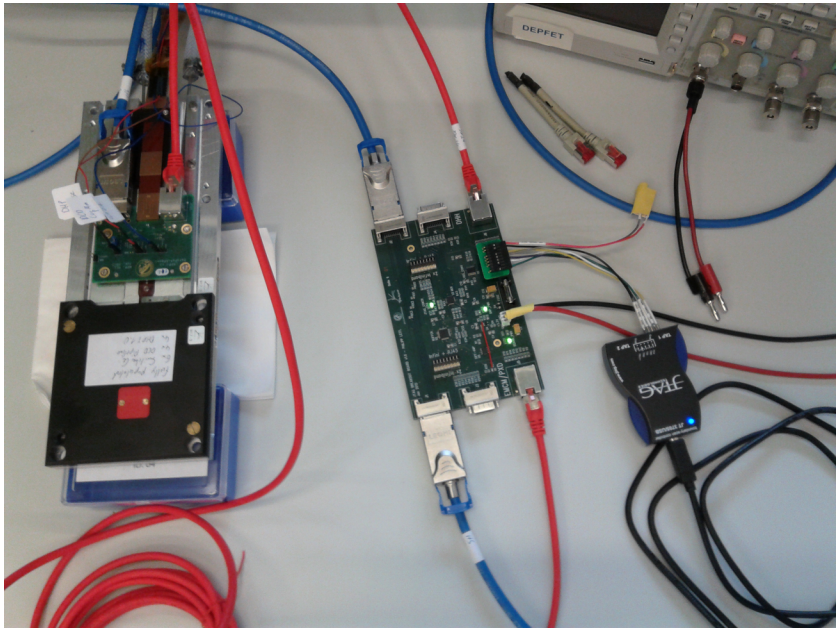


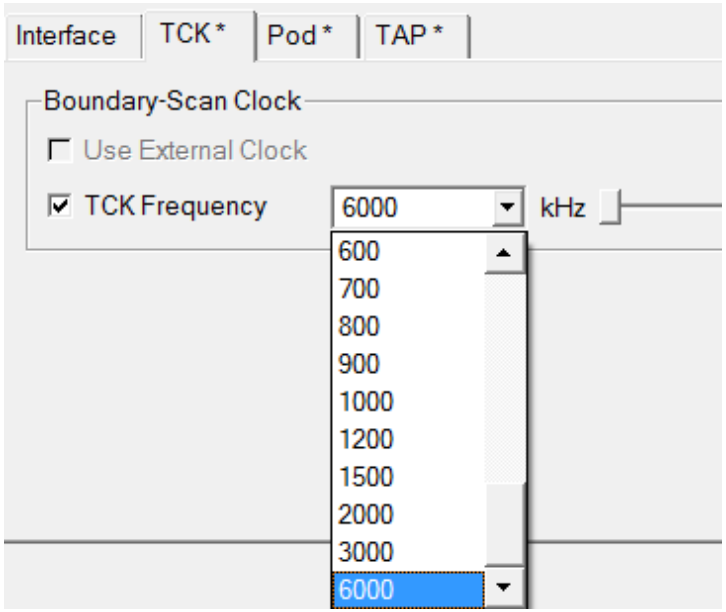


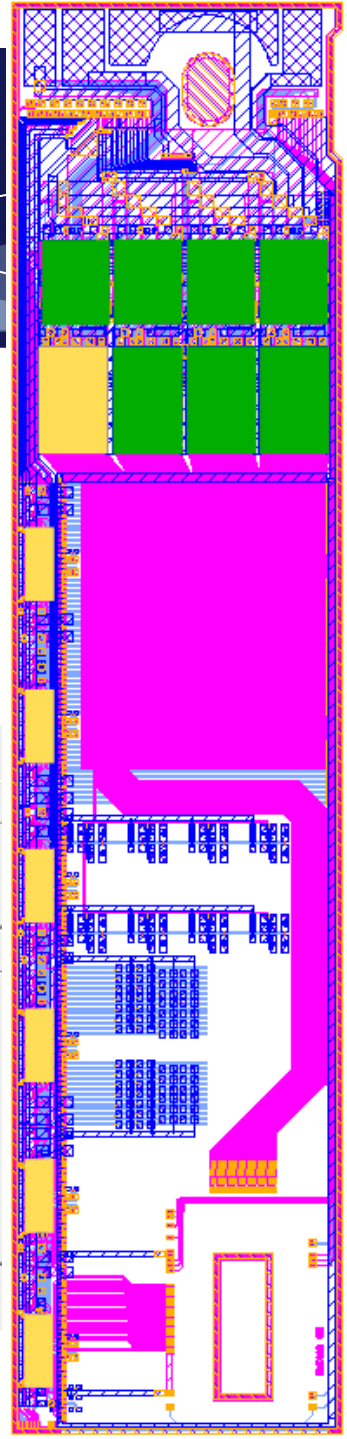
EMCM W17-3

new DHE
new ASICs →

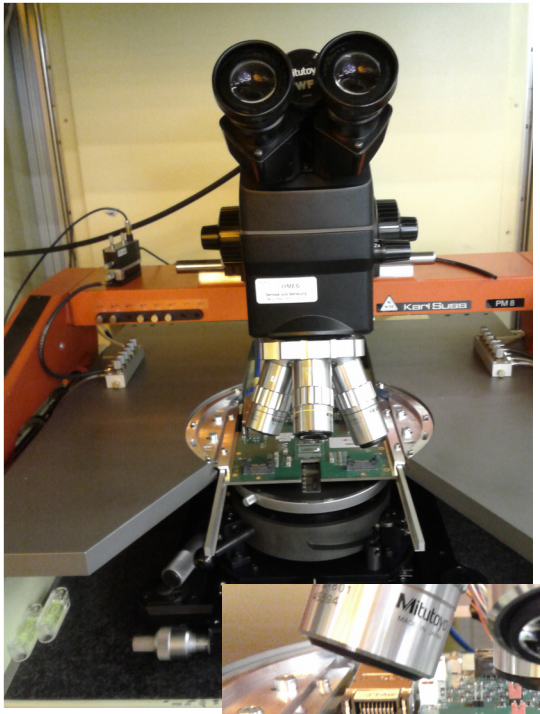
change in connectors (Infiniband → RJ45)
changes in the BSDL files (not for the DCD)
change in the TRG signal (not static any more)
change in maximal speed (≤ 3 MHz, best 1 MHz)

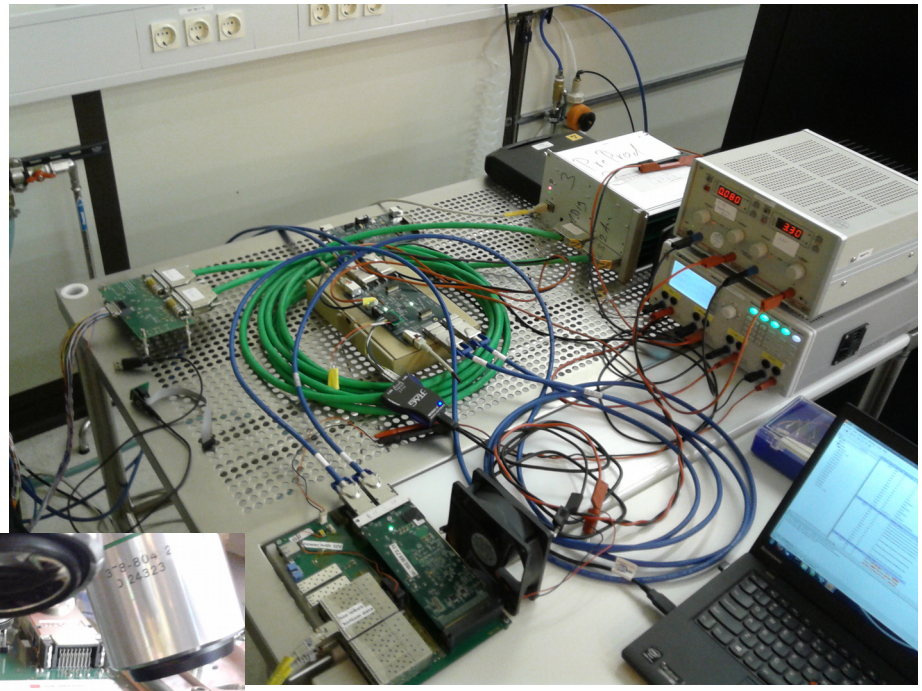


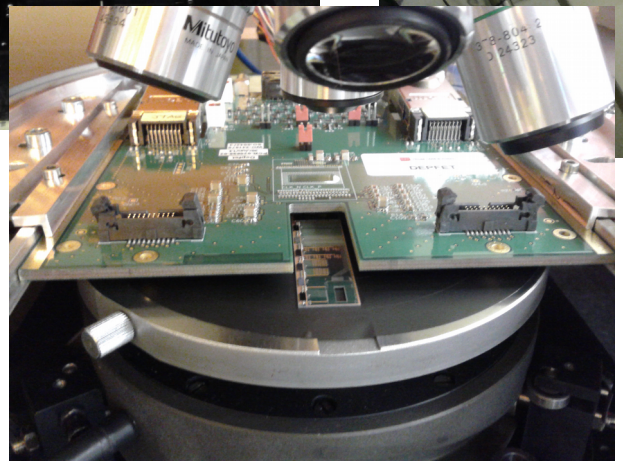


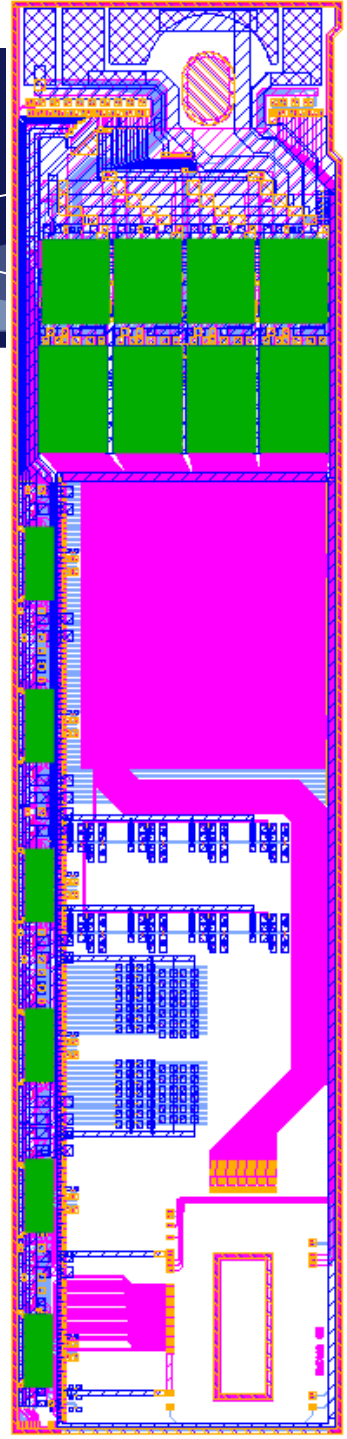


EMCM ProveCard









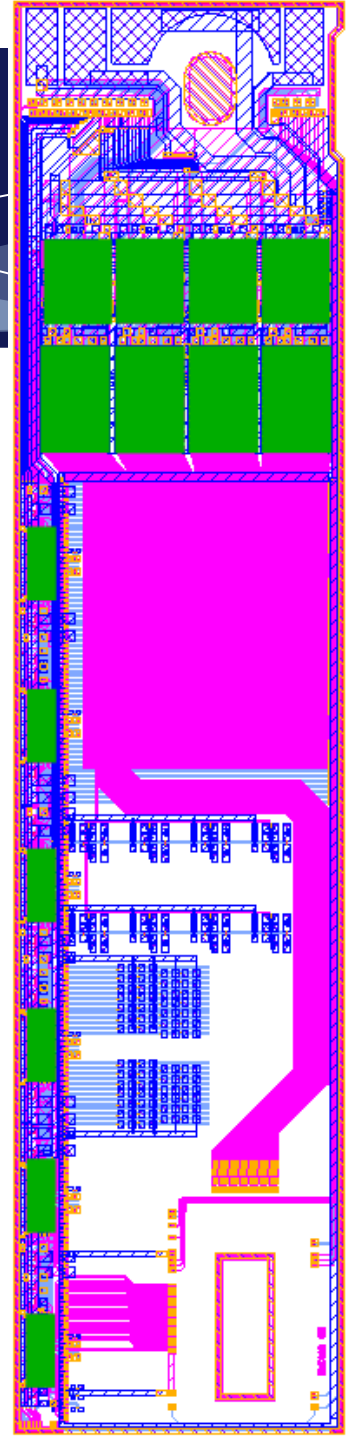
EMCM ProveCard

JTAG Live - C:\Users\phleitl\Documents\JTAG Live\projects\Prove-Card-full - [Infra Truth Table - infra]

Project Task Instrument Window Tools Help

Name	Pin id
Task1	
Buzz	
Boards	
Devices	
TAP1 - TDI	
DHP1	
DCD1	
DHP2	
DCD2	
DHP3	
DCD3	
DHP4	
DCD4	
SW1	
SW2	
SW3	
SW4	
SW5	
SW6	
TAP1 - TDO	

T-TAP	Chain	Device	Register	CAPTURE Test
1	TAP1	SW6	IR	101
		SW5	IR	101
		SW4	IR	101
		SW3	IR	101
		SW2	IR	101
		SW1	IR	101
		DCD4	IR	0101
		DHP4	IR	00000001
		DCD3	IR	0101
		DHP3	IR	00000001
		DCD2	IR	0101
		DHP2	IR	00000001
		DCD1	IR	0101
		DHP1	IR	00000001
		Flag	IR-pattern	111111111000000000
T-TAP	Chain	Device	Register	IDENT Test
1	TAP1	SW6	ID	00100011010001010110011110001001
		SW5	ID	00100011010001010110011110001001
		SW4	ID	00100011010001010110011110001001
		SW3	ID	00100011010001010110011110001001
		SW2	ID	00100011010001010110011110001001
		SW1	ID	00100011010001010110011110001001
		DCD4	BP	0
		DHP4	ID	01000100010010000101000000010001
		DCD3	BP	0
		DHP3	ID	01000100010010000101000000010001
		DCD2	BP	0
		DHP2	ID	01000100010010000101000000010001
		DCD1	BP	0
		DHP1	ID	01000100010010000101000000010001



Summary and Outlook

- Overview of Boundary Scan method
- Introduction of JTAG Breakout Board (JBB) successfully tested and assembly finished
- System of hardware (incl. probe station) and software (incl. BSDL files) working

- Getting familiar with the chosen JTAG software
- Development of a standardized procedure for testing the new PXD9 modules