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SI LAB Silizium Labor Bonn

DHPT delay and pilot run production tests

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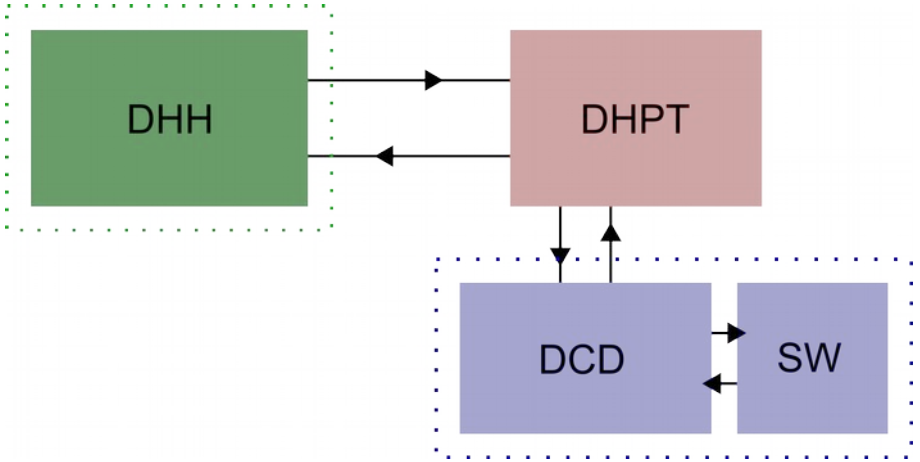
- System in use
- Delay measurements
  - FPGA based system
- DCD communication
  - Hybrid 5
- Pilot run production tests

- Three different setups used for the investigations of the communication of the DHPT
- DHPT only setups used to disentangle phenomena that are observed in multi chip setups (EMCM, Hybrids, etc)
- Test initially performed on single chip system and then transfered to multi chip systems



System in use

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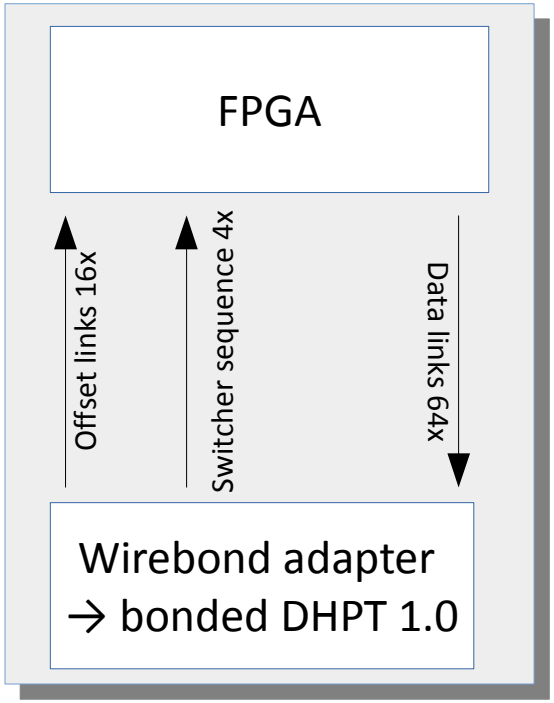
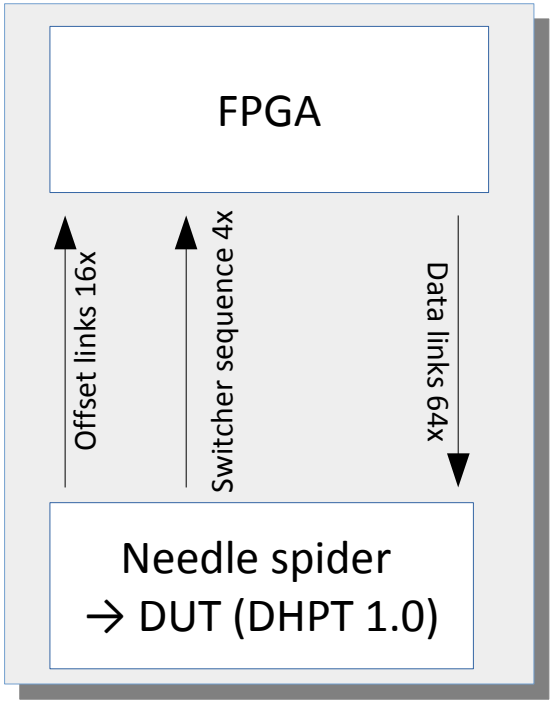
Debug Card



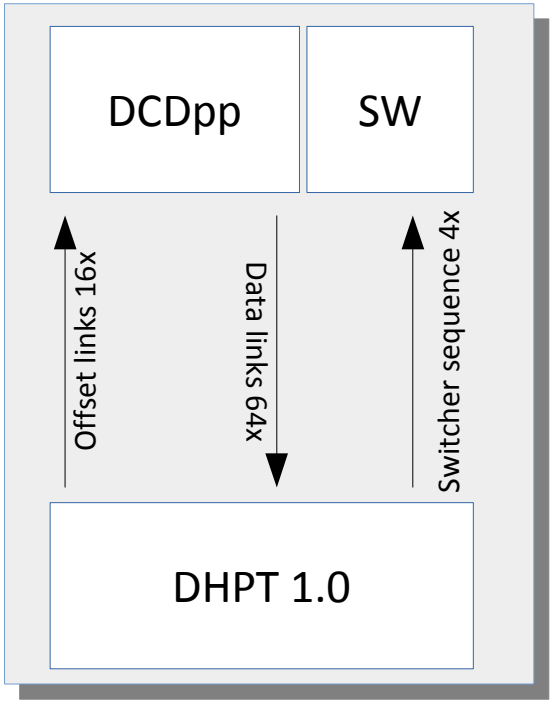
For software development and debugging (electrically identical to needle card)

Needle Card



For DUT testing

Hybrid 5



For system relevant aspects, i.e. communication DCD<->DHP, gated mode, etc.

Delay Measurements

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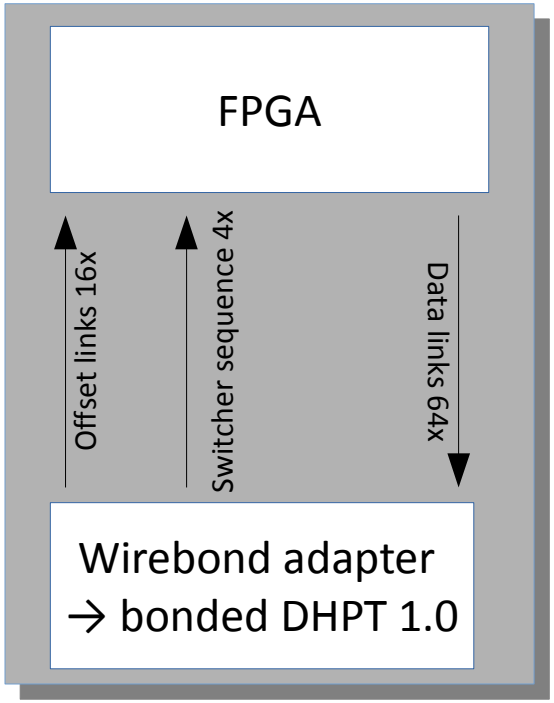
Debug Card



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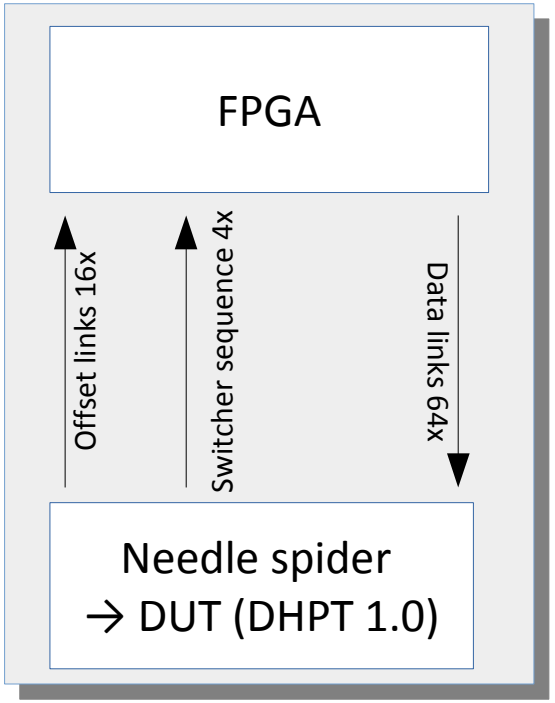

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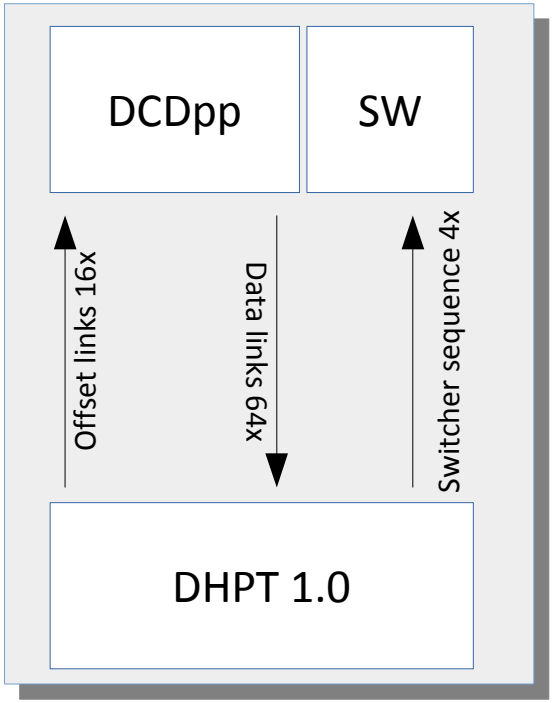

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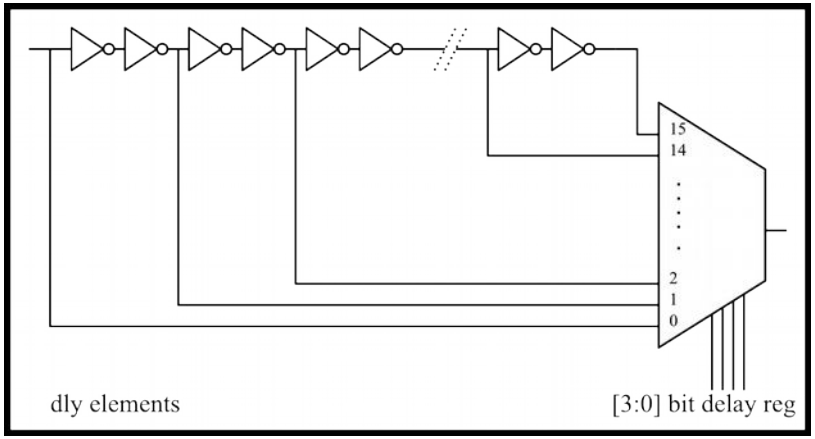
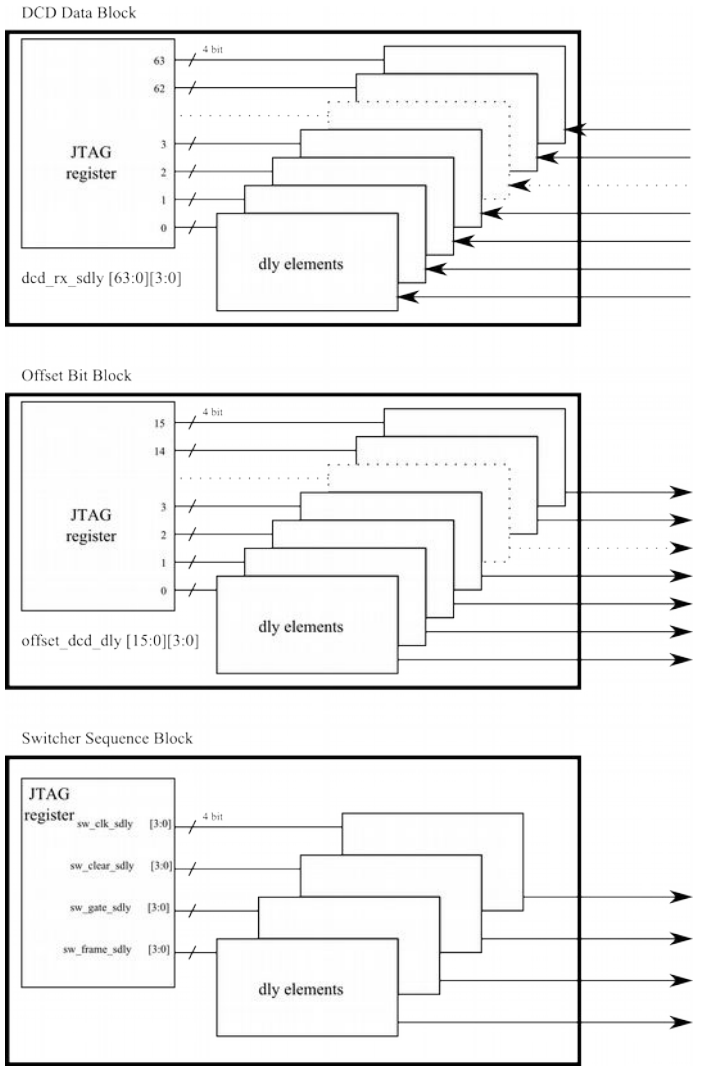
Delay Measurements

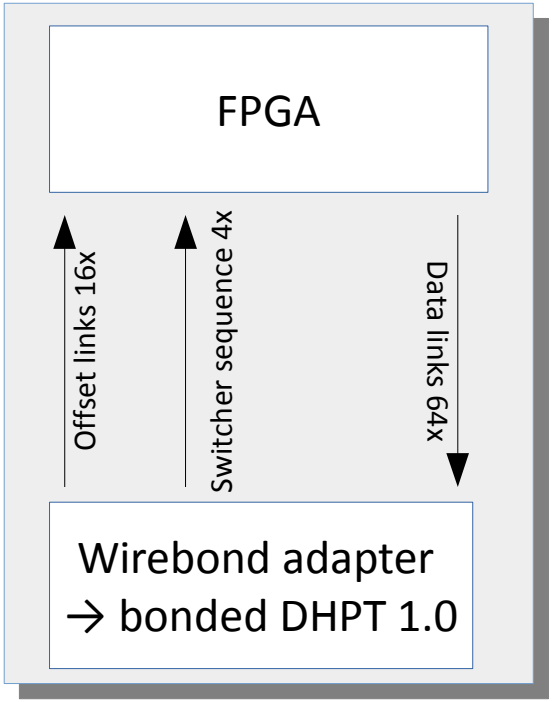
- Each I/O link has an **adjustable delay** set by JTAG registers
- Value 0 corresponds to no delay with respect to the driving clock of the signal
- Maximum 15 elements (inverter pairs) can be switched on



Simplified concept of implementation



- Debug Card used to investigate the effect of delays on signals, i.e. switcher sequence signal to FPGA
- Switcher sequences recorded on oscilloscope and read by the FPGA for relative bit error tests



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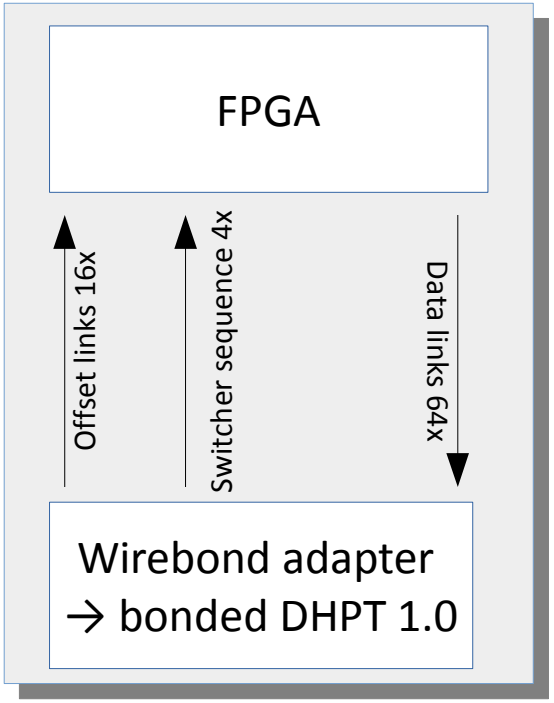


Delay Measurements

- Recorded waveforms (oscilloscope) of switcher sequence signal (clear) with an alternating pattern
- Nominal core voltage of 1.2V and reference clock of GCK = 77.7MHz

Duty Cycle 55% @ DLY 0

Duty Cycle 62% @ DLY 8

Duty Cycle 59% @ DLY 4

Duty Cycle 68% @ DLY 15

- Recorded waveforms (oscilloscope) of switcher sequence signal (clear) with an alternating pattern
- Nominal core voltage of 1.2V and reference clock of GCK = 77.7MHz

Duty Cycle 55% @ DLY 0

Sampling point

Duty Cycle 59% @ DLY 4

Duty cycle distortion due to non symmetric delay elements (standard cell) → replaced by custom design

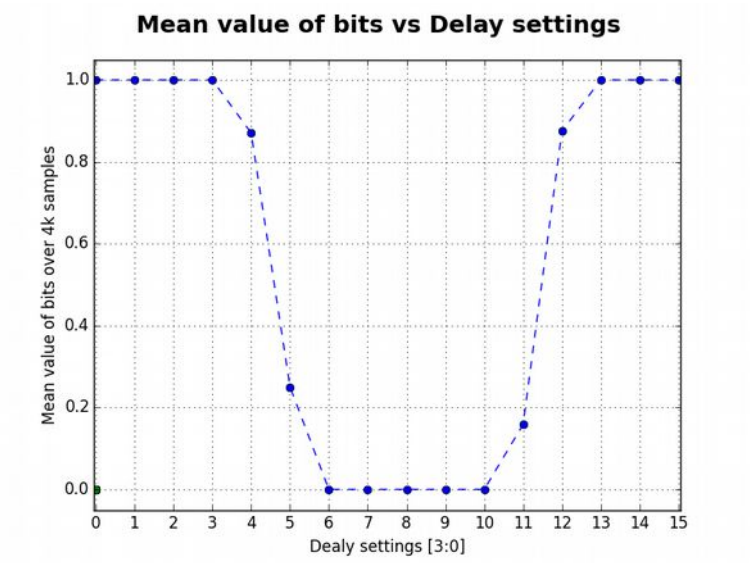
Duty Cycle 62% @ DLY 8

Sampling point

Duty Cycle 68% @ DLY 15

Delay Measurements

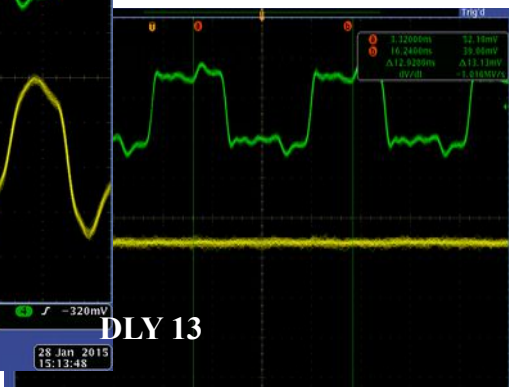
- The signals are sampled by the FPGA and analysed by the software to detect bit errors
- S-Curve → information about the absolute value of a single delay element (averaged over all 15)
- TDLY = 355+/-20 ps → Ttotal ~ 5.3 ns (covers 1.65x period of dcd_clk)



FPGA output

DLY 0

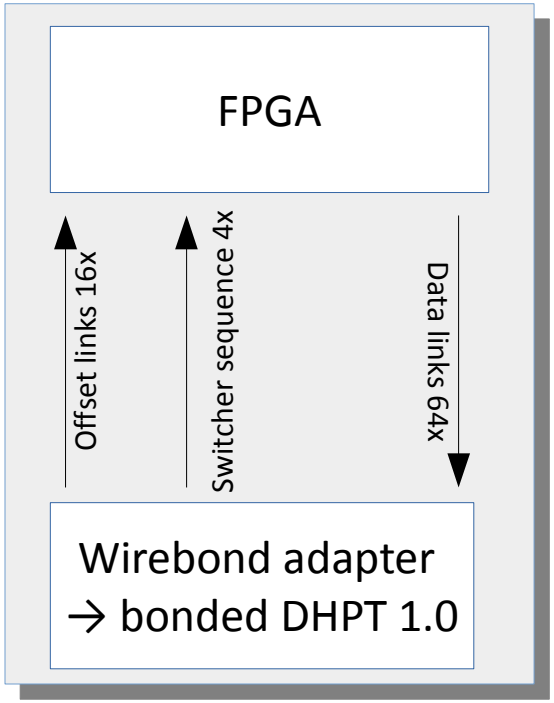
FPGA output



Sampling of bit

DCD communication

Debug Card



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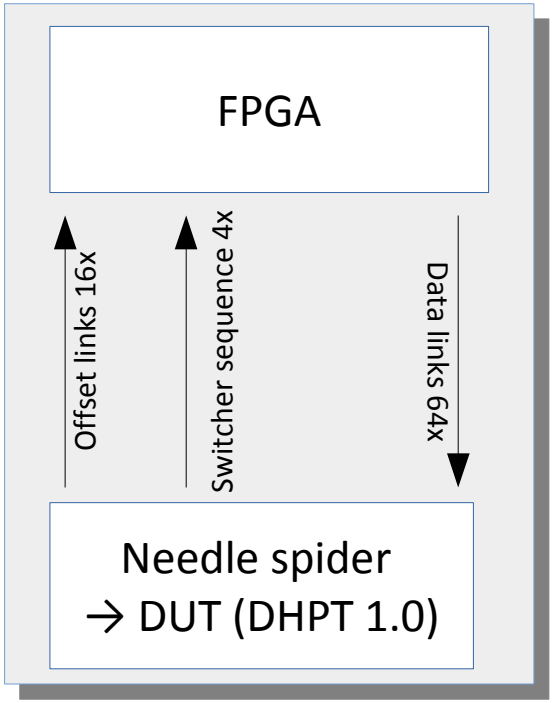
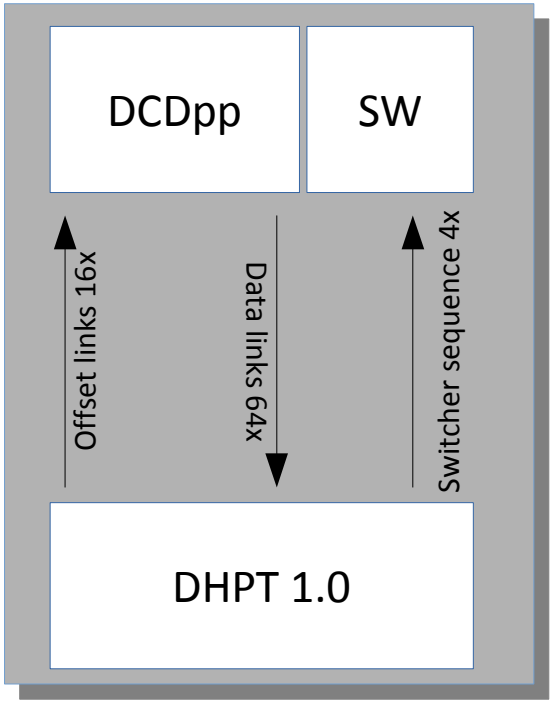


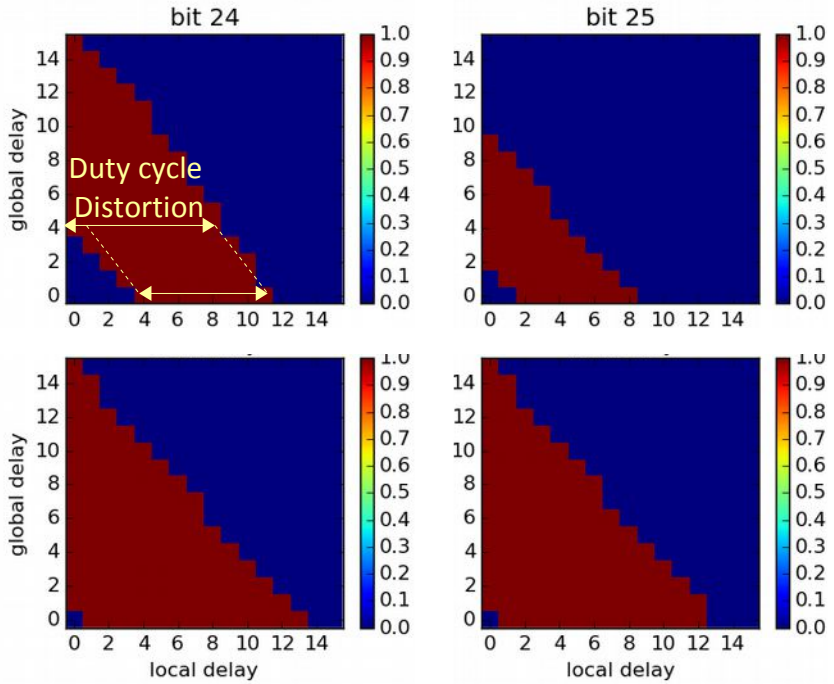
For DUT testing

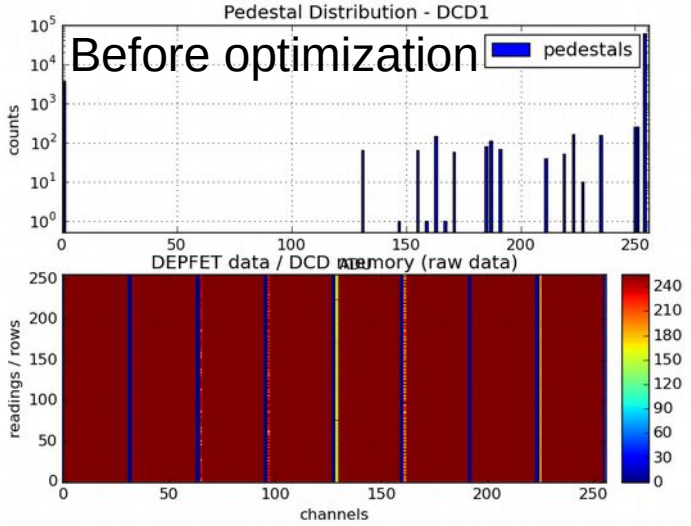
Hybrid 5

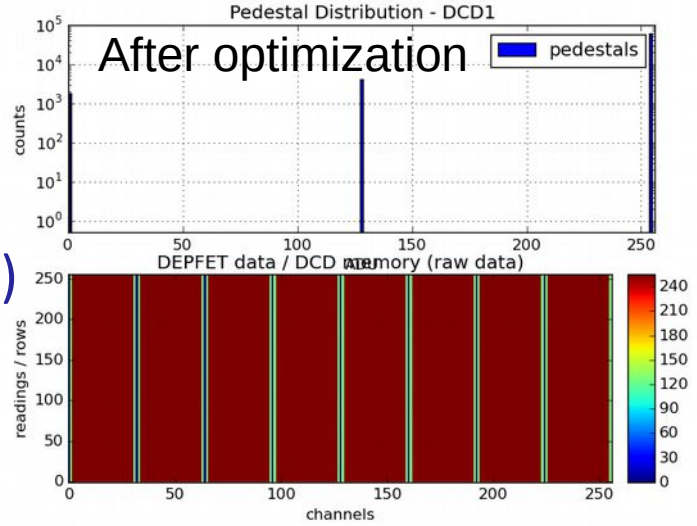


For system relevant aspects, i.e. communication DCD<->DHP, gated mode, etc.

DCD communication





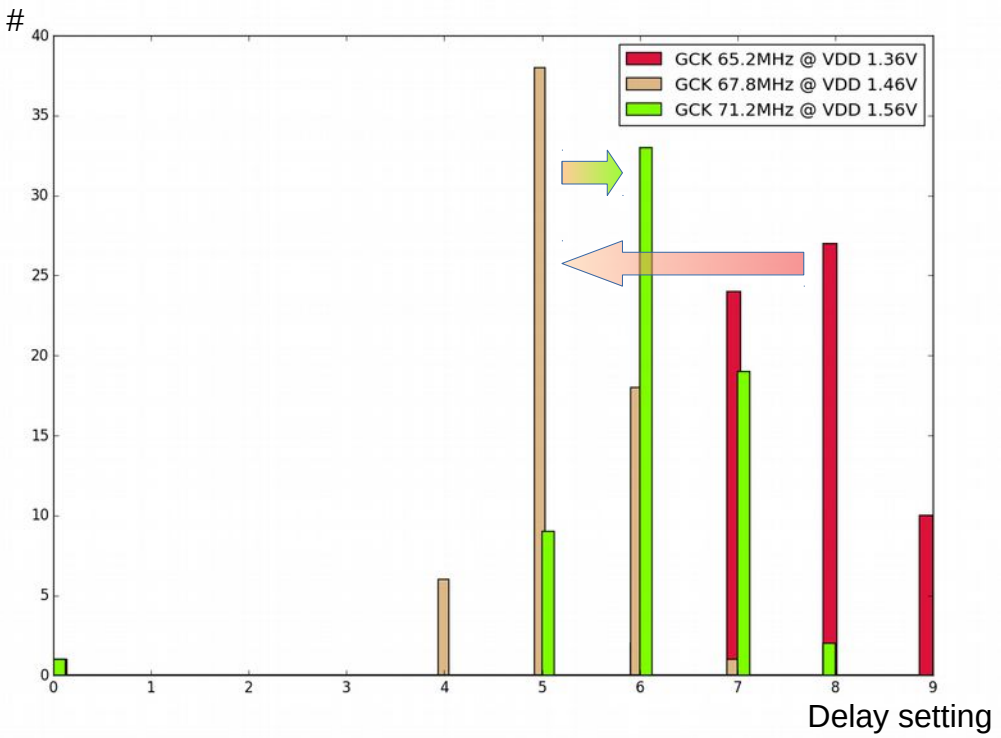


- Region of right delay settings (red,upper picture) @ GCK = 71.2MHz and VDD = 1.52V (core voltage)
- A bit shift is expected at a width of ~ 13.5

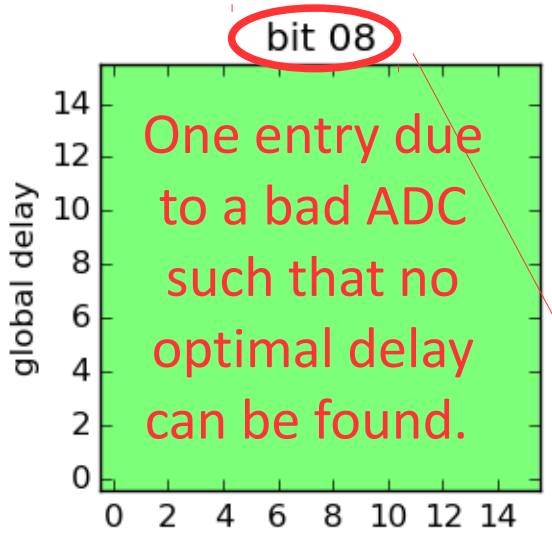
Distribution of optimized delay settings at different frequencies GCK and voltages VDD

Two concurrent effects:

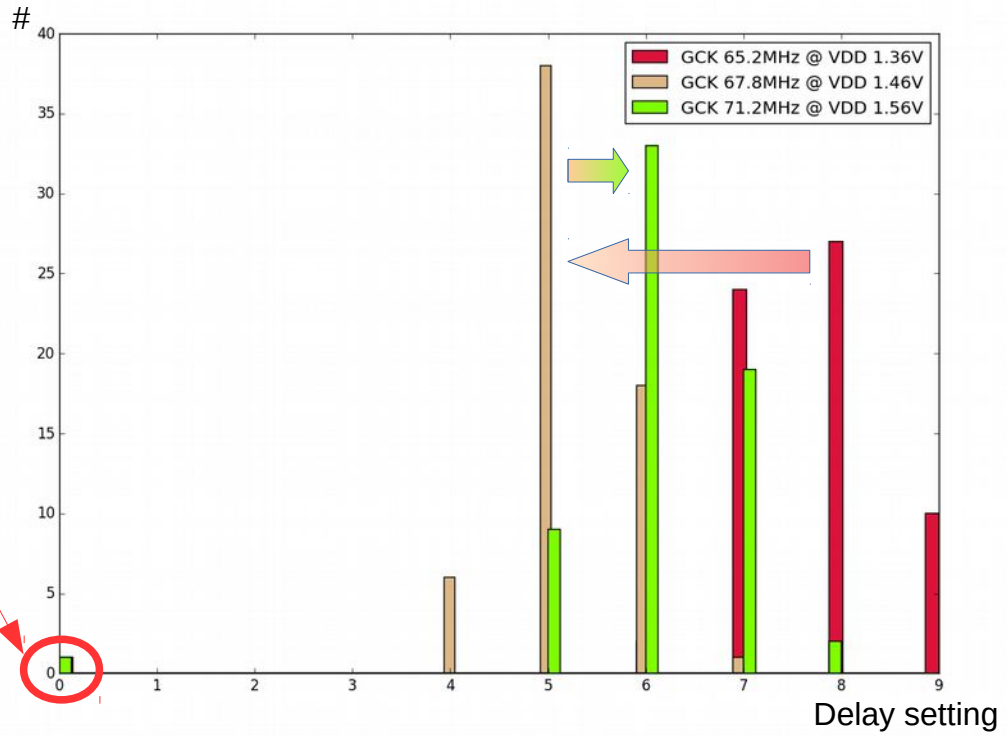
- Higher core voltages decrease the propagation time of a delay element → more elements needed for the same time delay
- Higher frequencies decrease the width of a bit → less elements needed for shifting the sampling point



Distribution of optimized delay settings
at different frequencies GCK and voltages VDD



Confirmed by further analysis of Philipp Wieduwilt, Göttingen



Pilot Run Production Test

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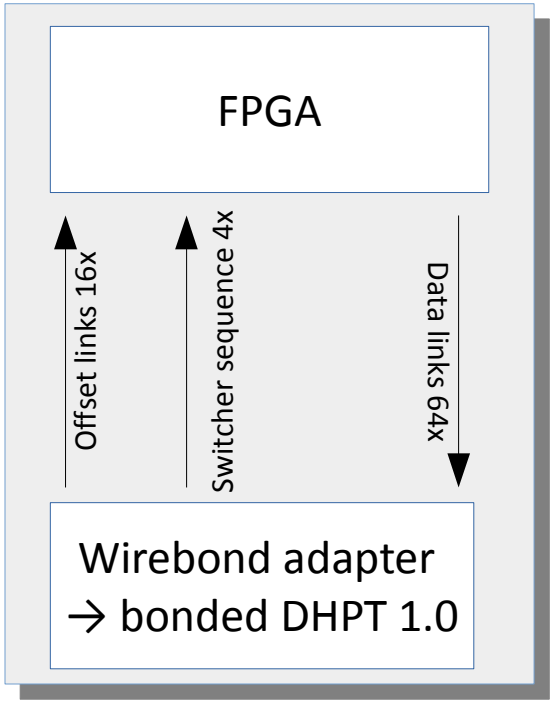
Debug Card



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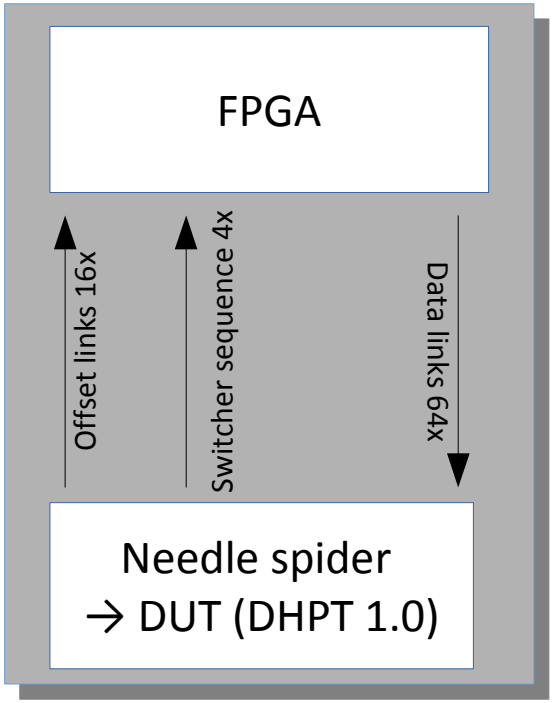
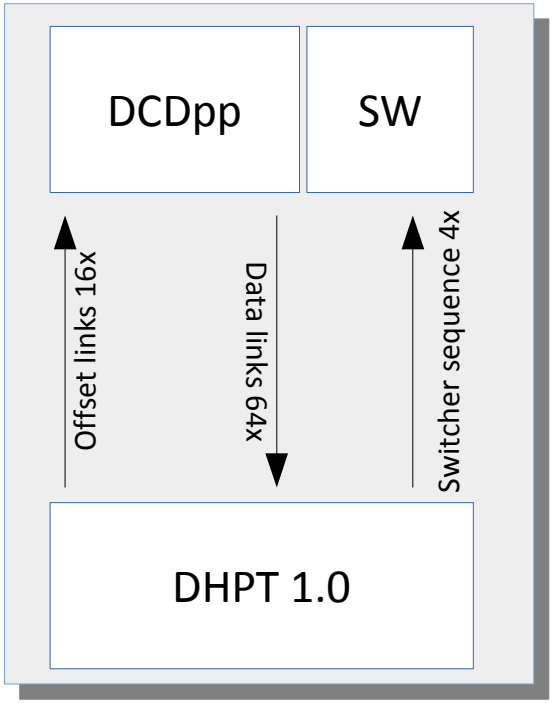


For DUT testing

Hybrid 5



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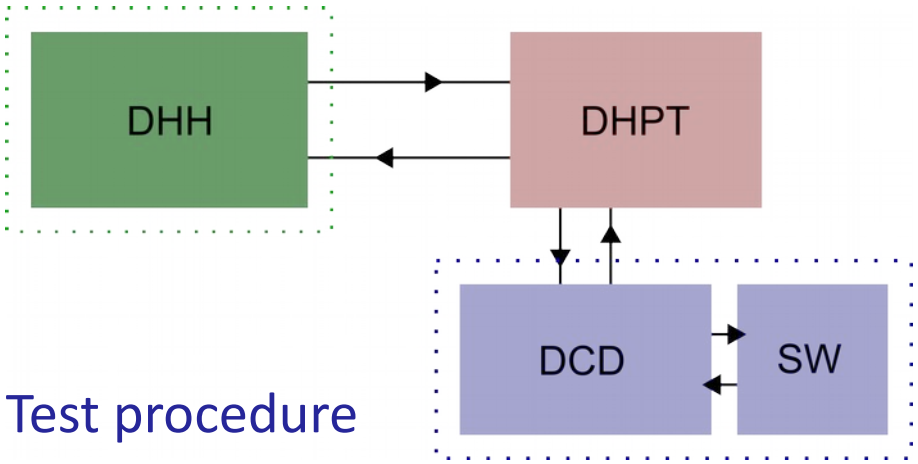


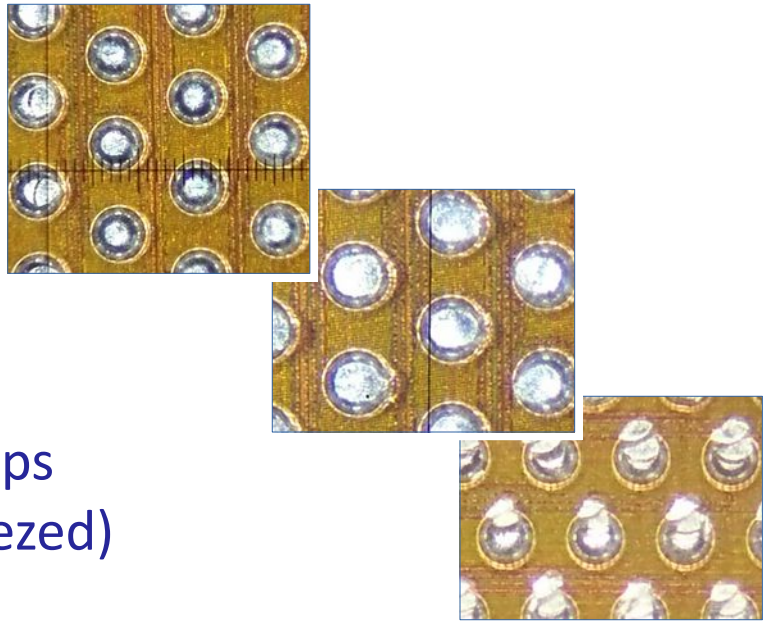
Test procedure

1. DHPT power consumption
2. JTAG register sanity check
3. DCD programming via JTAG
4. DHPT internal memory error counter
5. Memory sanity check
   - data, pedestal, offset and sw sequence
6. Switcher sequence test
   - Switching Normal ↔ gated mode
7. Offset bit check
8. Link stability and stress test
9. Data read in
   - DCDpp test pattern generation
10. Data processing
    - Rnd data generation with pre set pedestals, CM, threshold and occupancy
11. Temperature sensor read out

Test issues and bump categorization

- Contacting to bumps via the needles becoming worse with time, due to residues and oxide on the needle tips
- Higher forces needed to achieve sufficient contact to the bumps
  → stronger deformations of the bumps

- 3 Categories introduces of the DHPT tested for the pilot run
  - Cat1 : nicely touched bumps
    (~5 um flattened)
  - Cat2: strongly touched bumps
    (~20 um flattened)
  - Cat3: Sliced or strongly deformed bumps
    (e.g. contact from side and squeezed)



Results

- 31 DHPT1.0 ready for pilot run modules
  - #Cat1 10 chips, #Cat2 12 chips and #Cat3 9 chips
- Yield of 94%
- Bad chips have broken JTAG registers, or/and do not consume any power
- Chips suffured from 'hard' contact by the needles, not good planarity
- Needles have to be cleaned regularly (Ceramics)

row in picture does not correspond to the bump categories

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Generic DHPT tests

- Delay optimization is understood and controlled
- Duty cycle distortion will be corrected with the revision of the chip DHPT 1.1
- DCD communication needs more attention → more statistics to exclude link problems on the DHPT side

DHPT needle tests

- 2 Needle card will be used (cycling → one for probing while the other is cleaned)
- More attention on the bump connections. QC & QA needed.

Outlook

- Offset bits have to be investigated and understood (see Florians talk on Tuesday)
- Switcher sequencing on a Hybrid 5 has to be performed with final ASICs
- High occupancy tests on Hybrid 5 has to be performed

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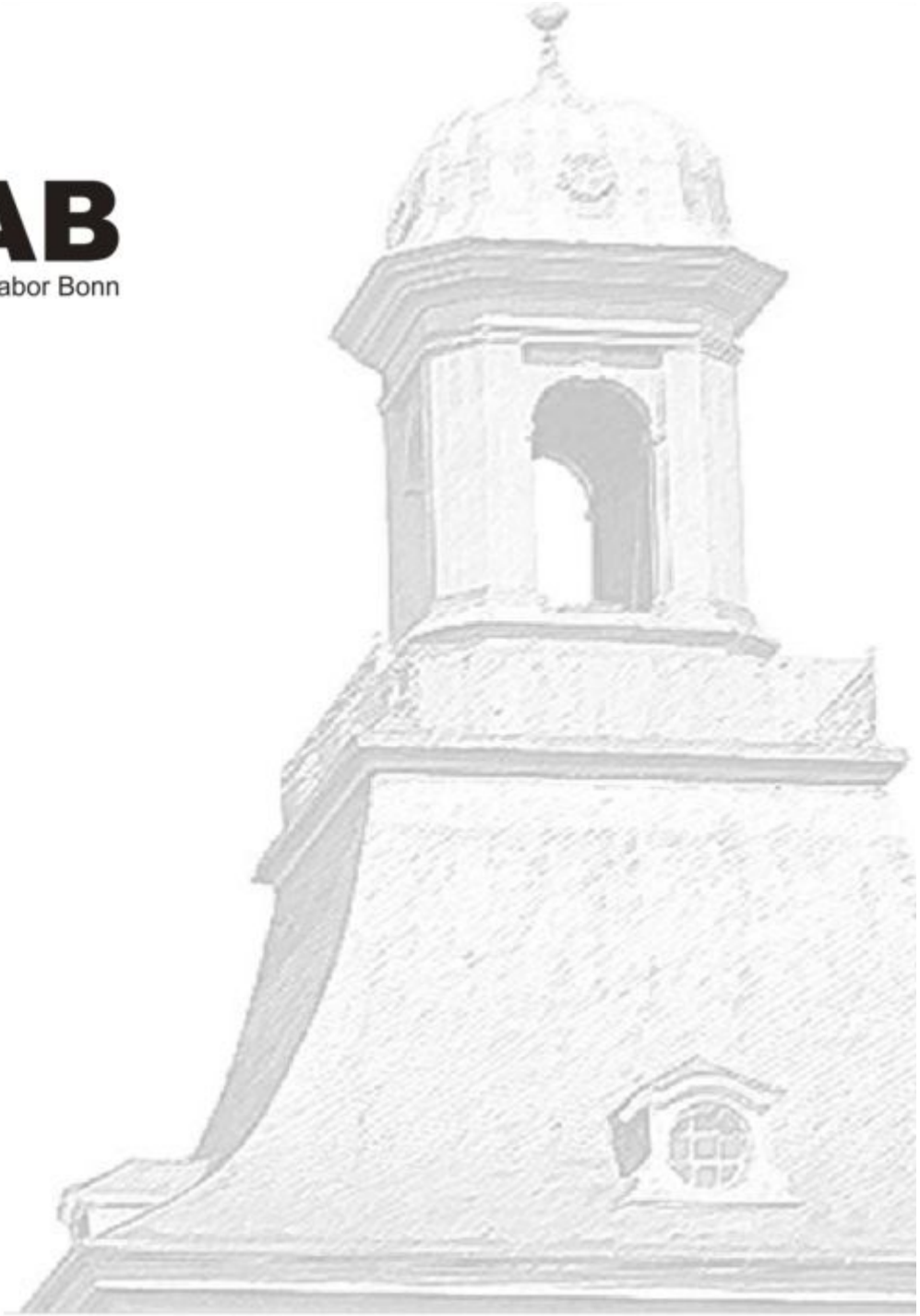

Thank you

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